DS38464
3.3V 64K x 40 NV SRAM SIMM

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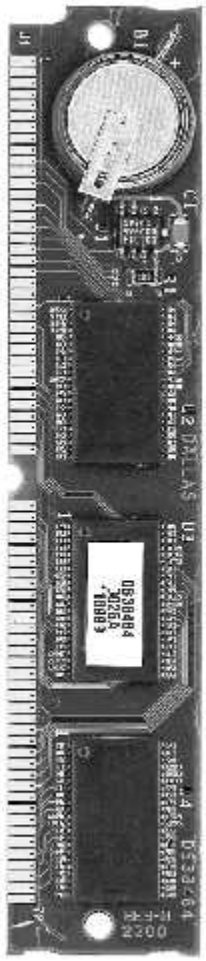
FEATURES

- 2Mbits organized as a 64K x 40 memory
- 6 years minimum data retention in the absence of external power
- Nonvolatile circuitry transparent to and independent of host system
- Automatic write protection circuitry safeguards against data loss
- Battery monitor checks remaining capacity daily
- Fast access time of 70ns
- Operating V_{CC} range of 3.0V to 3.6V
- Employs popular JEDEC standard 72-position SIMM connector
- Operating temperature: $0^{o}C$ to $+70^{o}C$

PIN DESCRIPTION

A0 - A15	-	Address Inputs
DQ0 – DQ39	-	Data Inputs/Outputs
CEA\	-	Chip Enable Inputs
WE\	-	Write Enable Inputs
OE\	-	Output Enable Inputs
VCC	-	3.3V Power Supply
GND	-	Ground

PIN ASSIGNMENT



DS38464 72-PIN SIMM

DESCRIPTION

The DS38464 is a self-contained 2,621,440-bit, nonvolatile static RAM, which is organized as a 64K x 40 memory. Built using three 64K x 16 SRAMs, one nonvolatile control IC, and one lithium battery, this nonvolatile memory contains all the necessary control circuitry and lithium energy source to maintain data integrity in the absence of power for more than 6 years. The DS38464 employs the popular JEDEC standard 72-position SIMM connection scheme and requires no additional circuitry.

READ MODE

The DS38464 executes a read cycle whenever WE\ is inactive (high) and CE\ and OE\ are active (low). The unique address specified by the 16 address inputs (A_0 - A_{15}) defines which byte of data is to be accessed from the selected SRAMs. Valid data will be available to the data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that CE\ and OE\ access times are also satisfied. If OE\ and CE\ access times are not satisfied, then data access must be measured from the later occurring signal (CE\ or OE\) and the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\ rather than t_{ACC}.

WRITE MODE

The DS38464 executes a write cycle whenever both WE\ and CE\ signals are in the active (low) state after address inputs are stable. The later occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\. All address inputs must be kept valid throughout the write cycle. WE\ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The OE\ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled (CE\ and OE\ active) then WE\ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS38464 provides full functional capability for V_{CC} greater than 3.0 volts and write protects by 2.8 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. Should the supply voltage decay, the NV SRAM automatically write protects itself, all inputs become “don’t care,” and all outputs become high impedance. As V_{CC} falls below approximately 2.5 volts, power switching circuits connect the lithium energy sources to the RAMs to retain data. During power-up, when V_{CC} rises above approximately 2.5 volts, the power switching circuits connect external V_{CC} to the RAMs and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 3.0 volts.

BATTERY MONITORING

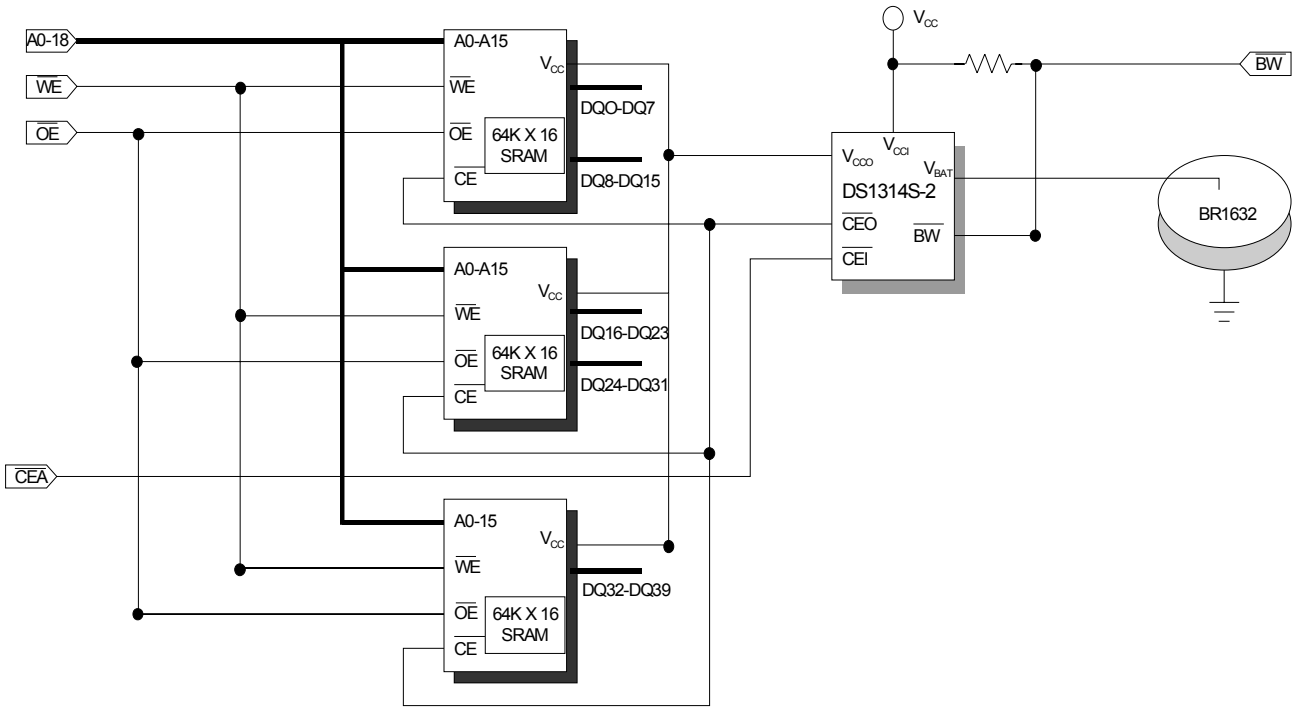
The DS38464 automatically performs periodic battery voltage monitoring on a 24 hour time interval. Such monitoring begins within t_{REC} after V_{CC} rises about V_{TP} and is suspended when power failure occurs.

After each 24 hour period has elapsed, the battery is connected to an internal 1MΩ test resistor for one second. During this one second, if battery voltage falls below the battery voltage trip point (2.6V), the battery warning output BW\ is asserted. Once asserted, BW\ remains active until the SIMM is replaced. The battery is still retested after each V_{CC} power-up, even if BW\ is active. If the battery voltage is found to be higher than 2.6V during such testing, BW\ is de-asserted and regular 24-hour testing resumes. BW\ has an open drain output driver.

PIN ASSIGNMENT

PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	NC	25	A15	49	A11
2	DQ0	26	A1	50	V_{SS}
3	DQ1	27	A2	51	NC
4	DQ2	28	A3	52	A12
5	DQ3	29	A4	53	A13
6	DQ4	30	A5	54	A14
7	DQ5	31	A6	55	DQ24
8	DQ6	32	A7	56	DQ25
9	DQ7	33	DQ16	57	DQ26
10	BW\	34	V_{CC}	58	DQ27
11	CEA\	35	DQ17	59	DQ28
12	OE\	36	DQ18	60	DQ29
13	WE\	37	V_{SS}	61	DQ30
14	DQ8	38	DQ19	62	DQ31
15	DQ9	39	DQ20	63	DQ32
16	DQ10	40	DQ21	64	DQ33
17	DQ11	41	DQ22	65	DQ34
18	DQ12	42	DQ23	66	DQ35
19	DQ13	43	NC	67	V_{CC}
20	DQ14	44	A8	68	DQ36
21	DQ15	45	A9	69	DQ37
22	V_{CC}	46	V_{CC}	70	DQ38
23	A0	47	V_{SS}	71	DQ39
24	V_{SS}	48	A10	72	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to ground -0.3 to +4.6V
Operating temperature 0°C to 70°C
Storage temperature -40°C to +85°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0 to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V	
Logic 1 Input Voltage	V_{IH}	2.2		V_{CC}	V	
Logic 0 Input Voltage	V_{IL}	0.0		+0.4	V	

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C; V_{CC} = 3.3V ± 0.3V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	$0V \le V_{IN} \le V_{CC}$	-4		+4	µA
Output Leakage Current	I_{LO}	$0V \le V_{OUT} \le V_{CC}$, all CE \ = V_{IH}	-1		+1	µA
Operating Current	I_{CCO}	duty=100% all CE\ = V_{IL}, $I_{I/O}$=0, V_{IN}=V_{IH} or V_{IL}			300	mA
Standby Current	I_{CCS}	all CE\ = V_{IH}			1	mA
Output High Current	I_{OH}	V_{OH} = 2.4V	-1.0			mA
Output Low Current	I_{OL}	V_{OL} = 0.4V	2.1			mA
Write Protection voltage	V_{TP}		2.8	2.9	3.0	V

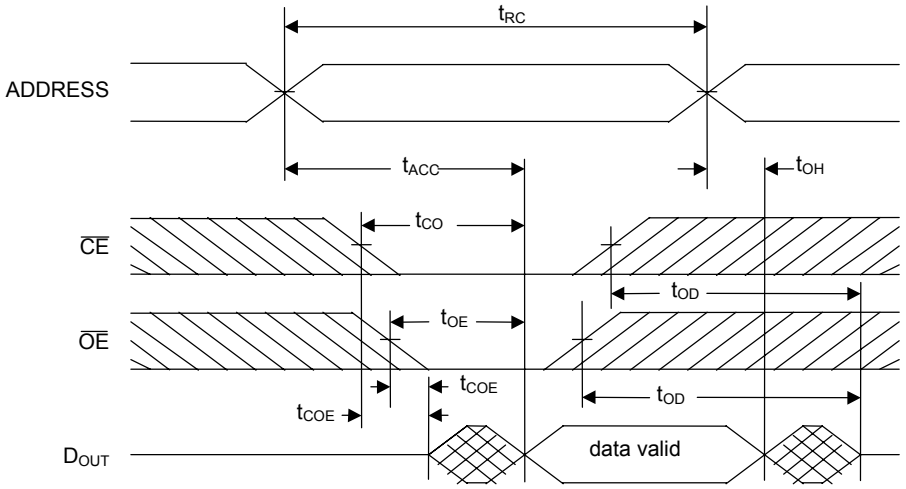
CAPACITANCE (T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			24	pF	
Output Capacitance	$C_{I/O}$			10	pF	

AC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C; V_{CC} = 3.3V ± 0.3V)

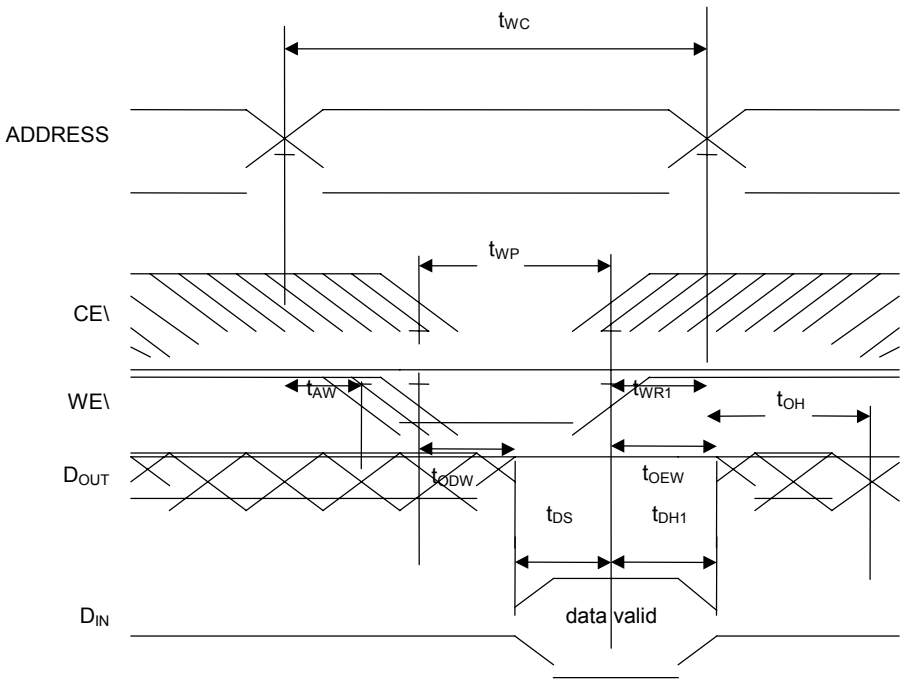
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read cycle time	t_{RC}	70			ns	
Access time	t_{ACC}			70	ns	
$\overline{OE}$ to output valid	t_{OE}			35	ns	
$\overline{CE}$ to output valid	t_{CO}			70	ns	
$\overline{OE}$ or $\overline{CE}$ to output active	t_{COE}	5			ns	5
Deselection to output high-z	t_{OD}			25	ns	5
Output hold after address change	t_{OH}	5			ns	
Write cycle time	t_{WC}	70			ns	
Write pulse width	t_{WP}	55			ns	3
Address setup time	t_{AW}	0			ns	
Write recovery time	t_{WR1}	5			ns	11
	t_{WR2}	20			ns	12
$\overline{WE}$ active to output high-z	t_{ODW}			25	ns	5
$\overline{WE}$ inactive to output active	t_{OEW}	5			ns	5
Data setup time	t_{DS}	30			ns	4
Data hold time	t_{DH1}	0			ns	11
	t_{DH2}	20			ns	12

TIMING DIAGRAM: READ CYCLE



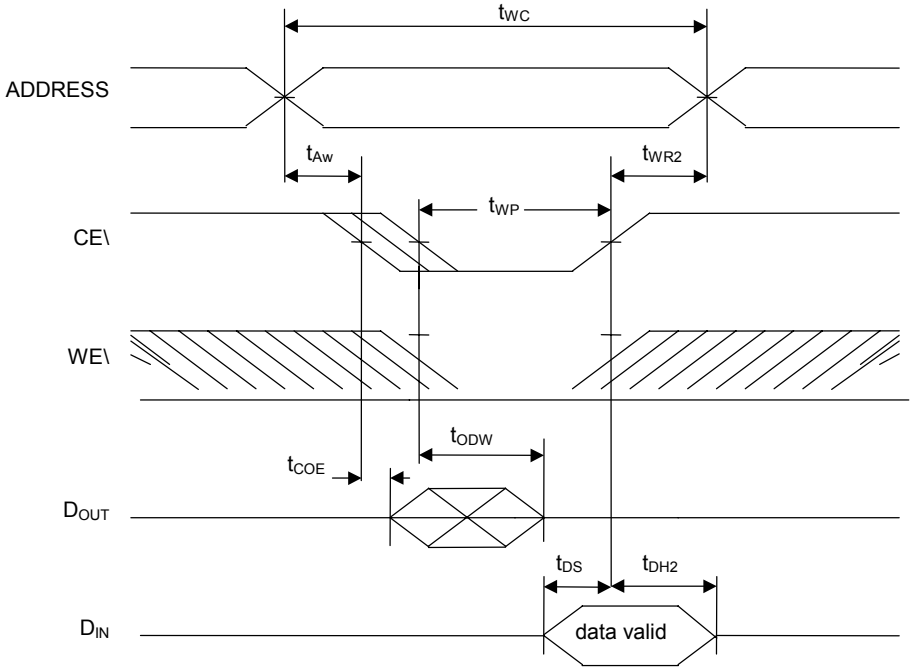
SEE NOTE 1

TIMING DIAGRAM: WRITE CYCLE 1 (WE\ Controlled)



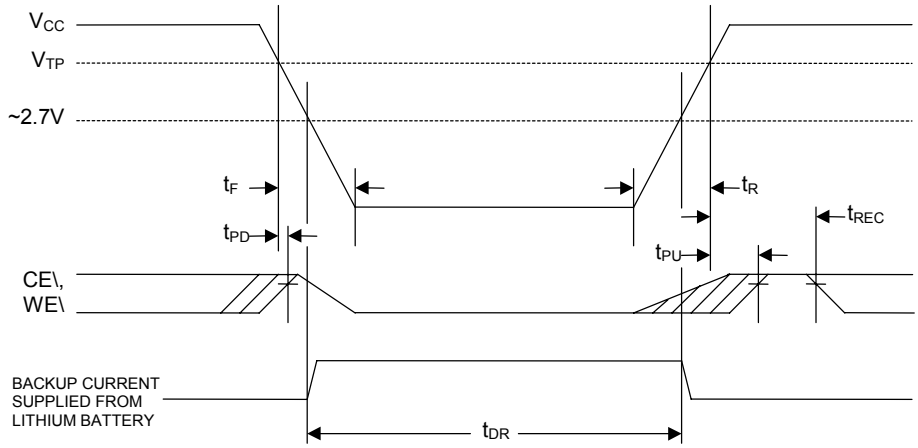
SEE NOTES 2, 3, 4, 6, 7, 8 AND 11

TIMING DIAGRAM: WRITE CYCLE 2 (CE\ Controlled)



SEE NOTES 2, 3, 4, 6, 7 8 AND 12

TIMING DIAGRAM: POWER-DOWN AND POWER-UP



SEE NOTE 10

POWER-DOWN/POWER-UP TIMING (T_A = 0 to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fail Detect to CE\ and WE\ Inactive	t_{PD}			1.5	µs	10
V_{CC} Slew from V_{TP} to 0V	t_F	150			µs	
V_{CC} Slew from 0V to V_{TP}	t_R	150			µs	
V_{CC} Valid to CE\ and WE\ Inactive	t_{PU}			2	ms	
V_{CC} Valid to End of Write Protection	t_{REC}			125	ms	

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	6			years	9

WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

1. WE\ is high throughout read cycle.
2. OE\ = V_{IH} or V_{IL}. If OE\ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of CE\ and WE\. t_{WP} is measured from the latter of CE\ or WE\ going low to the earlier of CE\ or WE\ going high.
4. t_{DS} is measured from the earlier of CE\ or WE\ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the CE\ low transition occurs simultaneously with or later than the WE\ low transition, the output buffers remain in a high impedance state during this period.
7. If the CE\ high transition occurs prior to or simultaneously with the WE\ high transition, the output buffers remain in a high impedance state during this period.
8. If WE\ is low or the WE\ low transition occurs prior to or simultaneously with the CE\ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS38464 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
11. t_{WR1}, t_{DH1} are measured from WE\ going high.
12. t_{WR2}, t_{DH2} are measured from CE\ going high.
13. BW\ is an open-drain output and cannot source current.

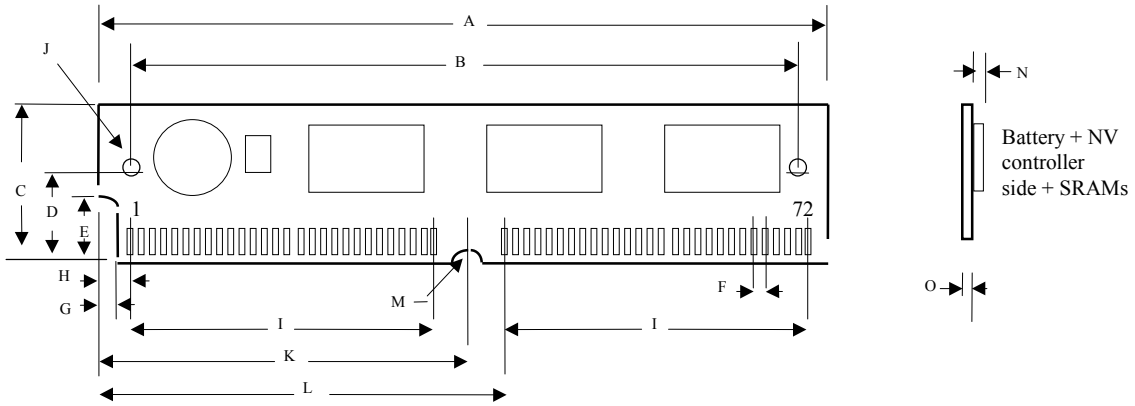
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns
All voltages are referenced to ground

AC TEST CONDITIONS

Output load: 50 pF + 1 TTL gate
Input pulse levels: 0 V to 2.7 V
Timing measurement reference levels
input: 1.5 V
output: 1.5 V
Input pulse rise and fall times: 5 ns

DS38464 72-PIN SIMM MODULE



PKG DIM	INCHES	
	MIN	MAX
A	4.245	4.255
B	3.979	3.989
C	0.845	0.855
D	0.395	0.405
E	0.245	0.255
F	0.050 BSC	
G	0.075	0.085
H	0.245	0.255
I	1.750 BSC	
J	0.120	0.130
K	2.120	2.130
L	2.245	2.255
M	0.057	0.067
N		0.130
O	0.047	0.054