National Semiconductor

ADVANCE INFORMATION

DS38C86A CMOS BTL 9-Bit Edge Latched/Registered Data Transceiver

General Description

The DS38C86A is one in a series of transceivers designed specifically for the proprietary bus interfaces implemented in CMOS technology, these transceivers deliver all of the performance of their Bi-CMOS counterparts with less then half of the power supply current. The DS38C86A is a CBTL 9-Bit Latching Data Transceiver designed to conform to IEEE 1194.1 (Backplane Transceiver Logic—BTL). The DS38C86A allows data transmission from A(port) TTL to B(port) BTL or from B(port) BTL to A(port) TTL depending on the logic level of T/$\overline{R}$ pin. Buffer, register and D-type latch configurations are available for the drive direction, while Buffer and D-type latch configurations are available for the receive direction.

The DS38C86A driver output configuration is an open drain which allows Wired-OR connection on the bus. A unique design reduces the bus loading to typically 3 pF. The driver also has high sink current capability to comply with the bus loading requirements defined within IEEE 1194.1 BTL specification.

Backplane Transceiver Logic (BTL) is a signaling standard that was invented and first introduced by National Semiconductor, then developed by the IEEE to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum

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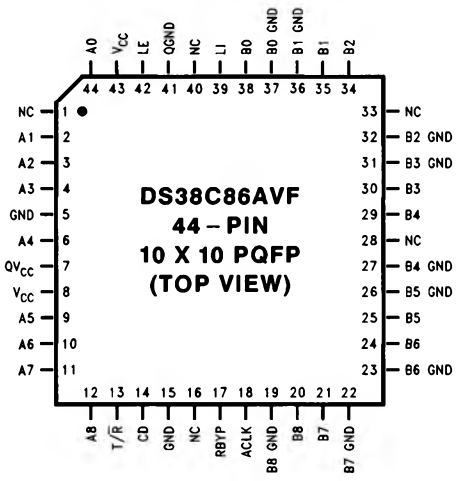
Features

- >50% less I_{CC} than BiCMOS DS3886A
- Fast propagation delay
- 9-Bit inverting BTL latched transceiver
- Driver incorporates edge triggered latches
- Receiver incorporates transparent latches
- Meets IEEE 1194.1 Standard on Backplane Transceiver Logic (BTL)
- Supports live insertion
- Glitch free power-up/down protection
- Typically 3 pF bus-port capacitance
- Low Bn bus-port voltage swing (typically 1V) at 80 mA
- Exceeds 2 kV ESD testing (Human Body Model)
- Open drain bus-port outputs allow Wired-OR connection
- Controlled rise and fall time to reduce noise coupling to adjacent lines
- TTL compatible driver and control inputs
- Built in bandgap reference with separate QV_{CC} and QGND pins for precise receiver thresholds
- Individual bus-port ground pins
- Product offered in PQFP 7 x 7, PQFP 10 x 10 and PLCC package style
- The 7 x 7 PQFP requires 50% less PCB space than 10 x 10
- Tight skew

Connection Diagrams



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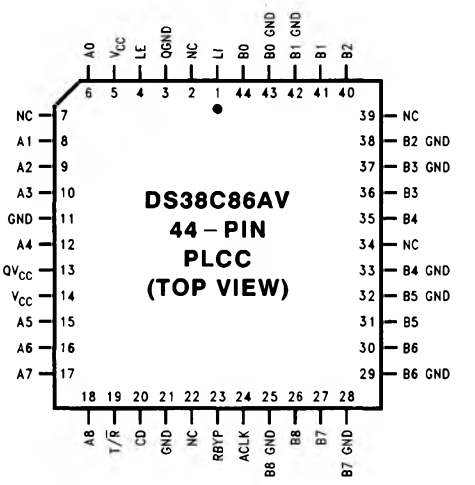

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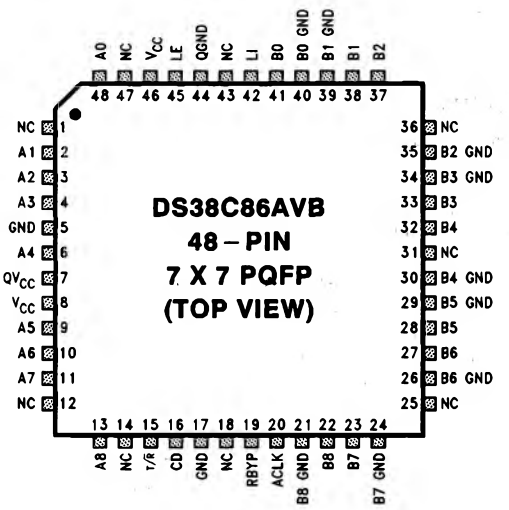
This datasheet contains the design specification for product development. Specifications may change in any manner without notice.

Connection Diagrams (Continued)



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Order Number DS38C86AV, DS38C86AVB or DS38C86AVF
See NS Package Number V44A, VBH48A or VF44B

General Description (Continued)

noise immunity. The BTL standard eliminates settling time delays that severely limit TTL bus performance, and thus provide significantly higher bus transfer rates. The backplane bus is intended to be operated with termination resistors (selected to match the bus impedance) connected to 2.1V at both ends. The low voltage is typically 1V.

Separate ground pins are provided for each BTL output to minimize induced ground noise during simultaneous switching.

The unique driver circuitry meets the maximum slew rate of 0.5V/ns which allows controlled rise and fall times to reduce noise coupling to adjacent lines.

The transceiver's high impedance control and driver inputs are fully TTL compatible.

The receiver is a high speed comparator that utilizes a Bandgap reference for precision threshold control, allowing maximum noise immunity to the BTL 1V signaling level. Separate QV_{CC} and QGND pins are provided to minimize the effects of high current switching noise. The output is TRI-STATE® and fully TTL compatible.

The DS38C86A supports live insertion as defined in IEEE 896.2 through the LI (Live Insertion) pin. To implement live insertion the LI pin should be connected to the live insertion power connector. If this function is not supported, the LI pin must be tied to the V_{CC} pin. The DS38C86A also provides glitch free power-up/down protection during power sequencing.

The DS38C86A has two types of power connections in addition to the LI pin. They are the Logic V_{CC} (V_{CC}) and the Quiet V_{CC} (QV_{CC}). There are three Logic V_{CC} pins on the DS38C86A that provide the supply voltage for the logic and control circuitry. Multiple connections are provided to reduce the effects of package inductance and thereby minimize switching noise. As these pins are common to the V_{CC} bus internal to the device, a voltage delta should never exist between these pins and the voltage difference between V_{CC} and QV_{CC} should never exceed ±0.5V because of ESD circuitry.

When CD (Chip Disable) is high, An is in high impedance state and Bn is high. To transmit data (An to Bn) the $T/\overline{R}$ signal is high.

When RBYP is high, the positive edge triggered flip-flop is in the transparent mode. When RBYP is low, the positive edge of the ACLK signal clocks the data.

In addition, the ESD circuitry between the V_{CC} pins and all other pins except for BTL I/O's and LI pins requires that any voltage on these pins should not exceed the voltage on V_{CC} + 0.5V.

There are three different types of ground pins on the DS38C86A; the logic ground (GND), BTL grounds (B0GND–B7GND) and the Bandgap reference ground (QGND). All of these ground reference pins are isolated within the chip to minimize the effects of high current switching transients. For optimum performance the QGND should be returned to the connector through a quiet channel that does not carry transient switching current. The GND and B0GND–B7GND should be connected to the nearest backplane ground pin with the shortest possible path.

Since many different grounding schemes could be implemented and ESD circuitry exists on the DS38C86A, it is important to note that any voltage difference between ground pins, QGND, GND or B0GND–B7GND should not exceed ±0.5V including power-up/down sequencing.