National Semiconductor

June 1992

DS8187 Vacuum Fluorescent Display Driver

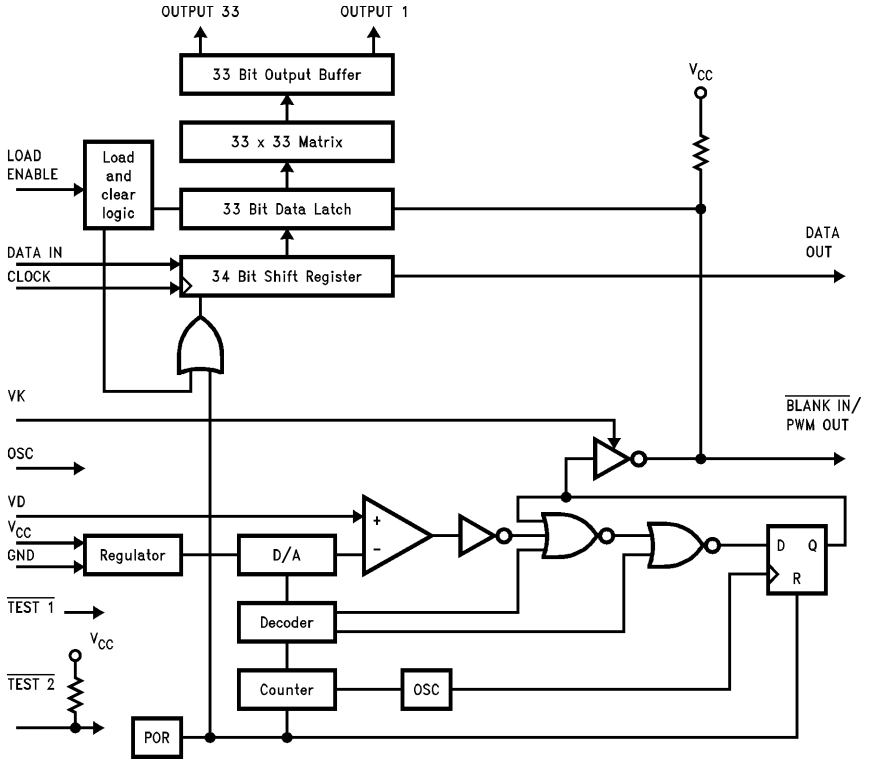
General Description

The DS8187 is a vacuum fluorescent display tube driver. This device is implemented in CMOS technology, to provide high voltage output drivers and low power. Dimming may be accomplished by either analog or digital input. Autoload capability is accomplished by connecting the DATA OUT pin to the LOAD ENABLE input pin, with the addition of a start bit to the input data stream.

Features

- 33 Segment Direct Drive 25 − 0.8 mA and 8 − 2 mA output drivers
- 49 steps of dimming, mask programmable
- Analog or digital input dimming control
- DATA OUT pin for cascading
- Mask options allow reconfiguring of outputs with respect to shift register bit position
- Autoload or external load capability

Block Diagram



TL/F/11220–4

FIGURE 1.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Volltage (V_{CC})	−0.3 to +20V
DC Input Voltage (V_{IN})	−0.3 to VCC+0.3V
DC Output Voltage (V_{OUT})	
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Power Dissipation (PD) at 25°C	
DIP Board Mount	TBD
DIP Socket Mount	TBD
Typical Values	
θJA DIP Board Mount	TBD °C/W
θJA DIP Socket Mount	TBD °C/W

Operating Conditions

	Min	Max	Unit
Supply Voltage (V_{CC})	8	18	V
DC Input or Output Voltage	0	V_{CC}	V
Temperature Range	−40	+85	°C
Electro-Static Discharge (ESD)		2K	V

DC Electrical Characteristics

V_{CC} = 8V to 18V, All voltages referenced to GND, unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage		3.8	6	V
V_{IL}	Low Level Input Voltage		0	0.8	V
I_{IH1}	High Level Input Current (Clock, Data In, Load, VK)	V_{IH1} = 5.0V	−5	5	μA
I_{IH2}	High Level Input Current (Blank)	V_{IH2} = 5.0V, T = 25°C	−20	10	μA
I_{IH3}	High Level Input Current ($\overline{TEST2}$)	V_{IH3} = %.0V, T = 25°C	−100	20	μA
I_{IL1}	Low Level Input Current (Clock, Data In, Load, VK)	V_{IL1} = 0V	−5	5	μA
I_{IL2}	Low Level Input Current ($\overline{BLANK\ IN}$)	V_{IL2} = 0V, T = 25°C	−125	−5	μA
I_{IL3}	Low Level Input Current ($\overline{TEST2}$)	V_{IL3} = 0V, T = 25°C	−700	−100	μA
I_{LI}	Input Leak Current (VD)	V_{IN} 0V to 6V	−5	5	μA
V_{OH1}	High Level Output Voltage (Low Current Driver)	V_{CC} = 9.5V, I_{OH1} = −0.8 mA	V_{CC}−0.8		V
V_{OH2}	High Level Output Voltage (High Current Drive)	V_{CC} = 9.5V, I_{OH2} = −2 mA	V_{CC}−0.8		V
V_{OH3}	High Level Output Voltage (DATA OUT, PWM OUT)	V_{CC} = 9.5V, I_{OH3} = −200 μA I_{OH3} = −20 μA	4 4.5	6 6	V V
V_{OL1}	Low Level Output Voltage (All Drivers)	V_{CC} = 9.5V, I_{OL1} = 500 μA I_{OL1} = 200 μA I_{OL1} = 2 μA		2 1 0.3	V V V
V_{OL2}	Low Level Output Voltage (DATA OUT,PWM OUT)	V_{CC} = 9.5V, I_{OL2} = 200 μA		0.8	V
I_{CC}	Supply Current	No Load		20	mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur.

AC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
f_C	Clock Frequency			250	kHz
PW_C	Clock Pulse Width		1.3		μs
t_S	Data Set-Up Time		1		μs
t_H	Data Hold Time		200		ns
PW_L	Load Pulse Width		1.3		μs
to_{DB}	Output Delay from Blank	C_L = 100 pF		7	μs
to_{DL}	Output Delay from Load	C_L = 100 pF		8	μs
t_r	Rise Time (All Driver Outputs)	C_L = 100 pF, t = 20% to 80% of V_{CC}		5	μs
t_f	Fall Time (All Driver Outputs)	CL = 100 pF, t = 80% to 20% of V_{CC}		5	μs

Dimming Characteristics

DC Characteristics

Parameter	Conditions	Min	Typ	Max	Units
V_D Offset Voltage (Note 2)	$\pm V_D$ (3% + 6%)			$\pm$10	mV

AC Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Pulse Width Error	No Load (Note 3)			$\pm$100	ns
PWM OUT Frequency		150	250	400	Hz
OSC Frequency		307.2	512	819.2	kHz

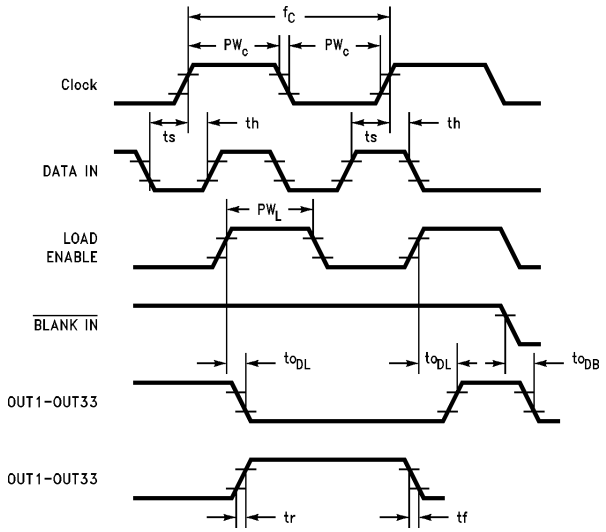
Note 2: Reference voltage is 6.1V typical.

Note 3: Under the ideal condition of DC parameters.

AC Test Conditions

Input Pulse Levels	0.5V to 3.5V
Input Rise and Fall Times	6 ns (10% to 90%)
Propagation Delays Measured at 20% and 80% points of respective waveforms	

Timing Waveforms



TL/F/11220–3

FIGURE 2.

Functional Description

SHIFT REGISTER OPERATION

Refer to block diagram *Figure 1* while LOAD ENABLE is low, data is entered into the shift register on the rising edge of the clock. The first data bit entered is stored in position #0, the last data bit entered is stored in position #33. A high voltage level applied to the LOAD ENABLE input transfers the data from the shift register to the data latch. The data is presented to the output drivers through a 33 x 33 matrix. This matrix determines shift register output designation. The DS8187 has 34 shift register positions, 33 data latches, and 33 output drivers.

AUTO LOAD MODE

In this mode, the DATA OUT pin is connected to the LOAD ENABLE pin. The data word consists of 34 bits including a leading start bit(logic 1). On the positive-going-edge of the 34th clock (LOAD ENABLE goes High), data is transferred to the data latches and the shift register is cleared.

DIRECT LOAD MODE

In this mode the DATA OUT pin is not connected to the LOAD ENABLE pin. The LOAD ENABLE pin is controlled directly by the user. When LOAD ENABLE goes High, the contents of the shift register are latched, presented to the output drivers through the 33 x 33 PLA matrix, and the shift register is cleared.

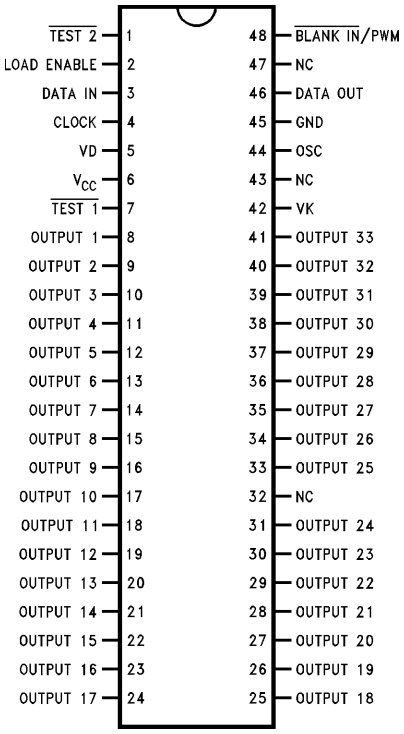
DIMMING FUNCTION

When VK is Low, the $\overline{\text{BLANK IN}}$/PWM OUT pin functions as an input blanking signal. When $\overline{\text{BLANK IN}}$/PWM is High, the output duty cycle is 100%. The duty cycle of a user supplied signal to this pin will determine the brightness of the output.

When VK is High, the duty cycle of the output drivers is controlled by an analog voltage applied to the VD pin. Table I indicates the duty cycle of the output drivers with respect to the analog voltage applied to VD pin.

Connection Diagram

Dual-In-Line Package



TL/F/11220–1

Top View
Order Number DS8187N
See NS Package Number N48A

Analog Dimming and V_D Offset Description

When using analog dimming, the brightness attainable is 10.2% of maximum brightness. The voltage (V_{REF}) is the external voltage from which V_D is developed (usually from a variable resistor). This voltage should be in the range of 5.7V to V_{CC} so that the maximum 10.2% PWM duty cycle is achieved easily.

The V_D offset error represents the difference between the actual analog input voltage when using analog dimming and the internal analog voltage created by the D/A converter. Table III indicates the PWM duty cycle with respect to voltage at the V_D pin over 49 steps of dimming. To determine the Min/Max PWM, V_D offset must be subtracted from/added to the threshold voltage of Table III. The Dimming Curves *(Figure 6)* are a graphical representation of Table III showing the V_D offset.

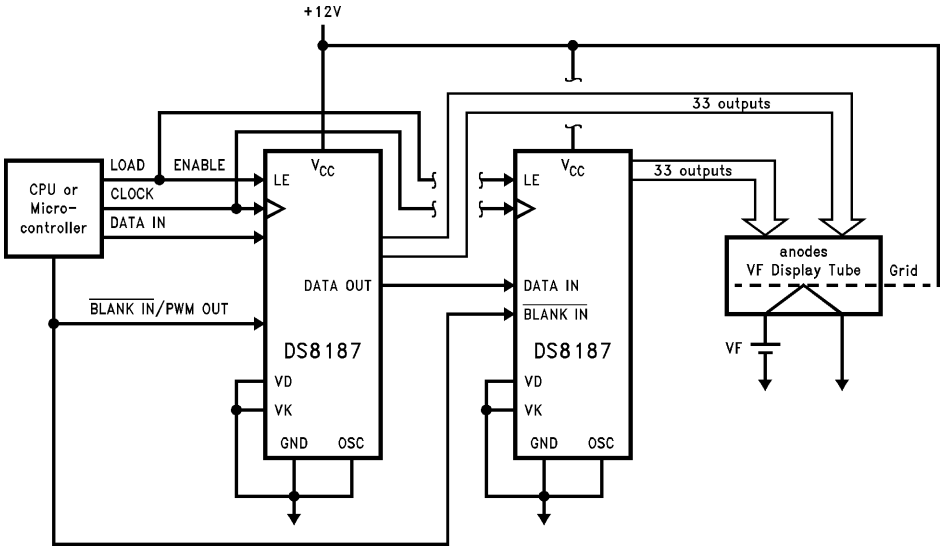
Load Enable Description

The positive going edge of the Load Enable input signal latches data from the shifter and resets the shifter. While Load Enable is ''high'', the shifter will not accept data. The Load Enable should be driven high during the low level of the clock.

Output Circuit Description

The segment output drivers are push-pull active high. There are 25 low current drivers (0.8 mA) and 8 high current drivers (2 mA). These outputs nominally swing from 0.3V to (V_{CC} − 0.8V) and are designed to drive the anodes of low voltage (about 13V) vacuum fluorescent displays. The digital outputs (DATA OUT and PWM OUT) typically swing form 0.5V to 5V and are designed to drive other logic devices. For example, referring to *(Figure 3)*, if DS8187 devices are cascaded, then DATA OUT and PWM OUT of the first are connected respectively to DATA IN and $\overline{\text{BLANK IN}}$ of the second.

Figures 3, 4 and *5* are typical applications of the DS8187.



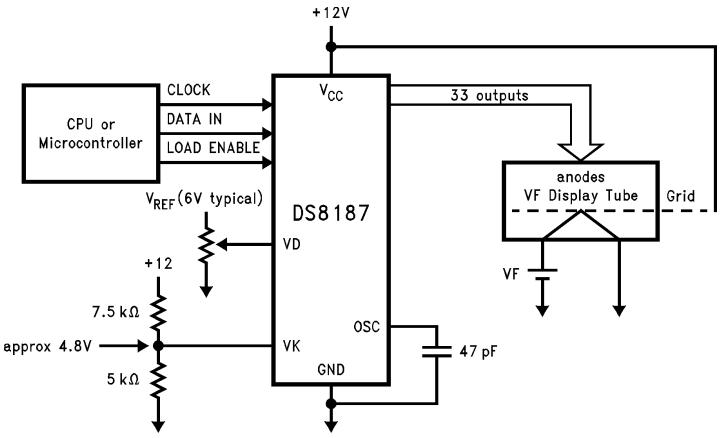
TL/F/11220–2

FIGURE 3. Cascading Two Drivers with Digital Dimming

Pin Description

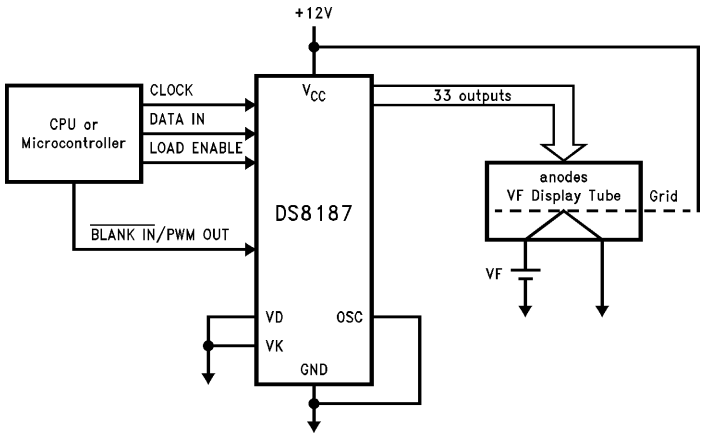
Pin No.	Pin Name	I/O	Description
1	$\overline{\text{TEST2}}$	I	This pin is used to select TEST MODE. (Factory Test)
2	LOAD ENABLE	I	While Low, data is enabled into the shift register. When this pin goes High, the contents of the shift register are loaded into the latch circuit and the shift register is reset to 0.
3	DATA IN	I	This pin inputs data to the shift register. When data is High, the output is ON. When data is Low, the output is OFF.
4	CLOCK	I	This pin is the clock for the shift register. Data is input to the shift register on the positive-going-edge of the clock.
5	VD	I	This analog voltage input pin specifies the output duty cycle per Table I.
6	V_{CC}		This is the power supply pin.
7	$\overline{\text{TEST1}}$		This pin is used to select TEST MODE. (Factory Test)
8−14	OUTPUT 1 to OUTPUT 7	O	These are low current output pins.
15−22	OUTPUT 8 to OUTPUT 15	O	These are high current output pins.
23−31	OUTPUT 16 to OUTPUT 24	O	These are low current output pins.
32	No Connect (NC)		Free pin, no connection to the chip.
33−41	OUTPUT 25 to OUTPUT 33	O	These are low current output pins.
42	VK	I	VK input terminal. This pin selects between analog dimming and digital dimming (duty cycle). When a Logic 0 is applied to VK, the $\overline{\text{BLANK IN}}$/PWM OUT pin functions as an input blanking signal. When a Logic 1 is applied to VK, the dimming is controlled by an analog voltage applied to the VD pin.
43	No Connect (NC)		Free pin, no connection to the chip.
44	OSC	I	This pin generates an oscillation of 500 kHz with an external capacitor of 47 pF connected between the OSC pin and GND.
45	GND		This is the GND pin.
46	DATA OUT	I/O	This pin outputs the data from the 34-bit shift register. Connecting the pin to the DATA IN pin on the next stage provides a cascade connection. Connecting the pin to the LOAD ENABLE pin causes the contents of the shift register to be latched on the leading edge of the signal at the DATA OUT pin. (Auto load function). In the Test Mode, this pin functions as an input.
47	No Connect (NC)		Free pin, no connection to the chip.
48	$\overline{\text{BLANK IN}}$/PWM OUT	I/O	When the internal dimming function is not used (VK = Low), this pin receives an external blank signal and controls the output duty cycle. This pin functions as an output when the internal dimming function is used (VK = High), and in Test Mode.

Typical Application



TL/F/11220–5

FIGURE 4. Analog Dimming Control Using the V_D Pin



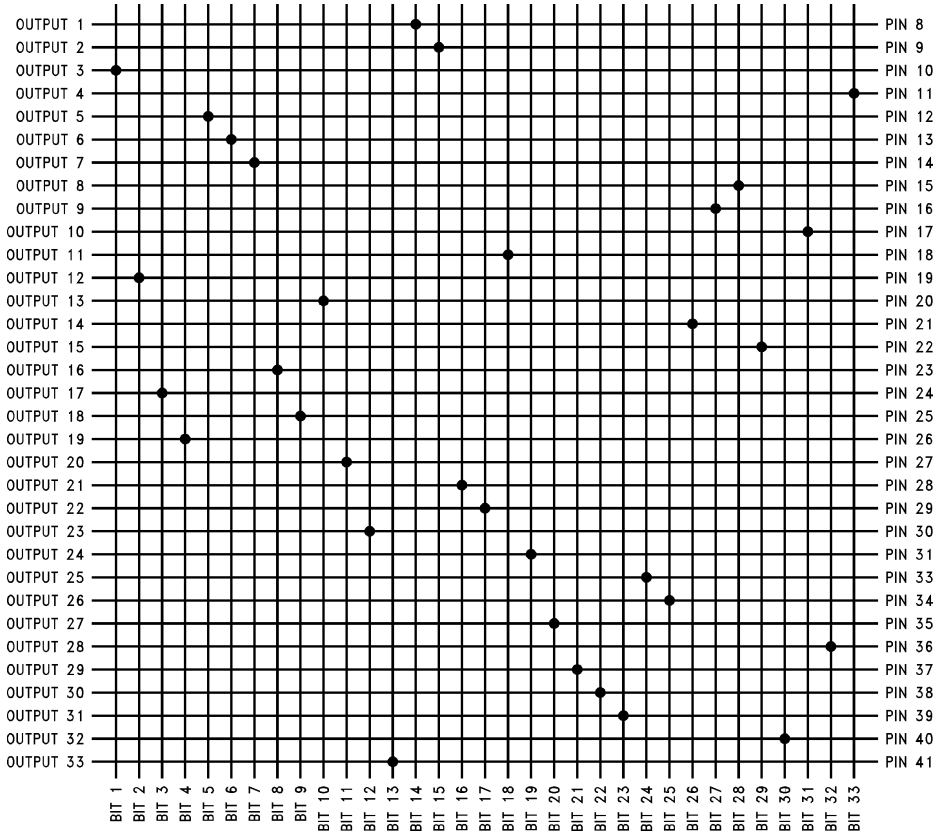
TL/F/11220–7

FIGURE 5. Digital Dimming Using the $\overline{\text{BLANK IN}}$/PWM OUT Pin

TABLE I. Output Pin to Shift Register Conversion for Pattern "AA"

Pin Name	Shift Register	Pin Name	Shift Register	Pin Name	Shift Register
OUTPUT 1	BIT 14	OUTPUT 12	BIT 2	OUTPUT 23	BIT 12
OUTPUT 2	BIT 15	OUTPUT 13	BIT 10	OUTPUT 24	BIT 19
OUTPUT 3	BIT 1	OUTPUT 14	BIT 26	OUTPUT 25	BIT 24
OUTPUT 4	BIT 33	OUTPUT 15	BIT 29	OUTPUT 26	BIT 25
OUTPUT 5	BIT 5	OUTPUT 16	BIT 8	OUTPUT 27	BIT 20
OUTPUT 6	BIT 6	OUTPUT 17	BIT 3	OUTPUT 28	BIT 32
OUTPUT 7	BIT 7	OUTPUT 18	BIT 9	OUTPUT 29	BIT 21
OUTPUT 8	BIT 28	OUTPUT 19	BIT 4	OUTPUT 30	BIT 22
OUTPUT 9	BIT 27	OUTPUT 20	BIT 11	OUTPUT 31	BIT 23
OUTPUT 10	BIT 31	OUTPUT 21	BIT 16	OUTPUT 32	BIT 30
OUTPUT 11	BIT 18	OUTPUT 22	BIT 17	OUTPUT 33	BIT 13

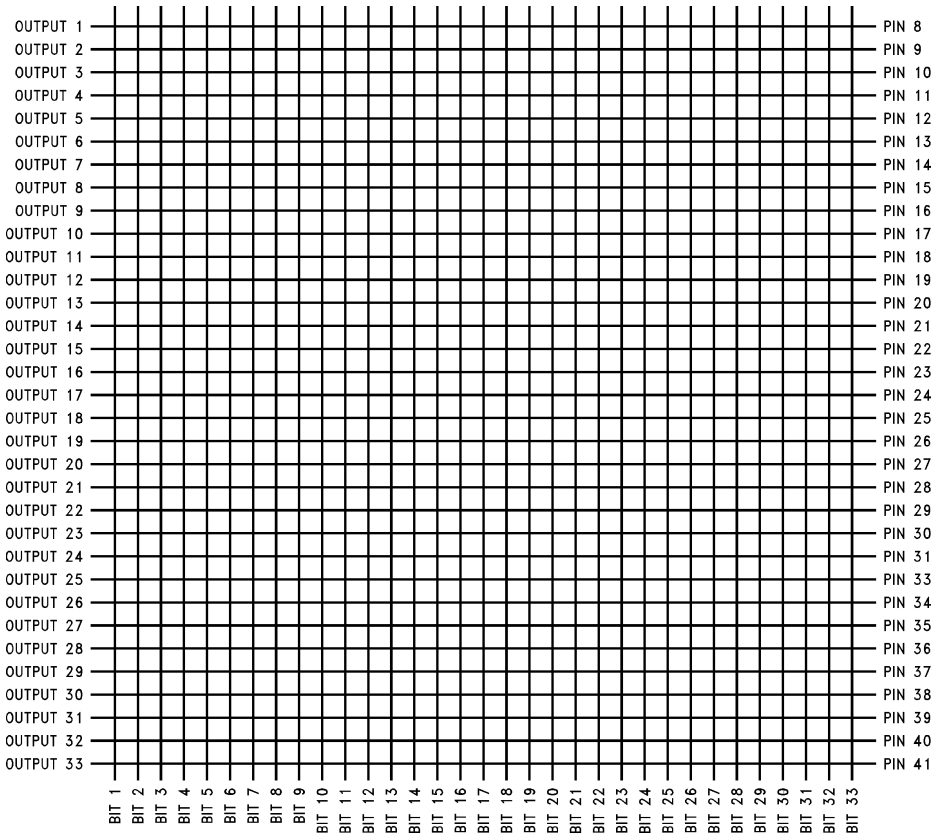
PLA Code Chart



TL/F/11220–8

TABLE II. Customer Fill In, Output Pin to Shift Register Conversion

Pin Name	Shift Register	Pin Name	Shift Register	Pin Name	Shift Register
OUTPUT 1	BIT	OUTPUT 12	BIT	OUTPUT 23	BIT
OUTPUT 2	BIT	OUTPUT 13	BIT	OUTPUT 24	BIT
OUTPUT 3	BIT	OUTPUT 14	BIT	OUTPUT 25	BIT
OUTPUT 4	BIT	OUTPUT 15	BIT	OUTPUT 26	BIT
OUTPUT 5	BIT	OUTPUT 16	BIT	OUTPUT 27	BIT
OUTPUT 6	BIT	OUTPUT 17	BIT	OUTPUT 28	BIT
OUTPUT 7	BIT	OUTPUT 18	BIT	OUTPUT 29	BIT
OUTPUT 8	BIT	OUTPUT 19	BIT	OUTPUT 30	BIT
OUTPUT 9	BIT	OUTPUT 20	BIT	OUTPUT 31	BIT
OUTPUT 10	BIT	OUTPUT 21	BIT	OUTPUT 32	BIT
OUTPUT 11	BIT	OUTPUT 22	BIT	OUTPUT 33	BIT



TL/F/11220–6

TABLE III. VD Threshold Dimming Voltage V.S. PWM Duty Cycle (Typical Value at V_{CC} = 12.8V)
10.2% PWM Maximum

Pulse Step Number	PWM Duty Cycle		Threshold Voltage	Pulse Step Number	PWM Duty Cycle		Threshold Voltage
	Pulse Count	%			Pulse Count	%	
			V_{REF}	26	56/2048	2.73	3.385
			V_{REF}	25	52/2048	2.54	3.323
			V_{REF}	24	48/2048	2.34	3.263
49	208/2048	10.2	V_{REF}	23	46/2048	2.25	3.204
48	192/2048	9.38	4.621	22	44/2048	2.15	3.155
47	184/2048	8.98	4.541	21	42/2048	2.05	3.118
46	176/2048	8.59	4.488	20	40/2048	1.95	3.076
45	168/2048	8.20	4.434	19	38/2048	1.86	3.027
44	160/2048	7.81	4.381	18	36/2048	1.76	2.983
43	152/2048	7.42	4.333	17	34/2048	1.66	2.941
42	144/2048	7.03	4.286	16	32/2048	1.56	2.898
41	136/2048	6.64	4.231	15	30/2048	1.46	2.860
40	128/2048	6.25	4.170	14	28/2048	1.37	2.822
39	120/2048	5.86	4.106	13	26/2048	1.27	2.785
38	112/2048	5.47	4.043	12	24/2048	1.17	2.744
37	104/2048	5.08	3.980	11	23/2048	1.12	2.692
36	96/2048	4.69	3.914	10	22/2048	1.07	2.650
35	92/2048	4.49	3.831	9	21/2048	1.03	2.622
34	88/2048	4.30	3.766	8	20/2048	0.98	2.597
33	84/2048	4.10	3.719	7	19/2048	0.93	2.569
32	80/2048	3.91	3.673	6	18/2048	0.88	2.539
31	76/2048	3.71	3.631	5	17/2048	0.83	2.511
30	72/2048	3.52	3.594	4	16/2048	0.78	2.478
29	68/2048	3.32	3.551	3	15/2048	0.73	2.455
28	64/2048	3.13	3.501	2	14/2048	0.68	2.425
27	60/2048	2.93	3.444	1	13/2048	0.63	2.392
							0.000

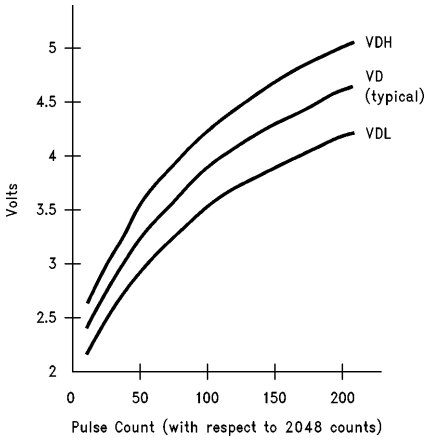


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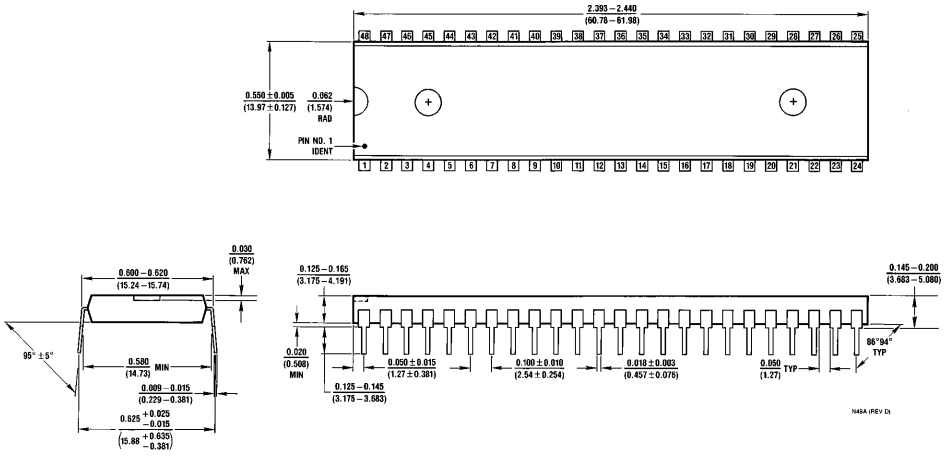
FIGURE 6. Dimming Curve
(Graphical Representation of Table III)

Physical Dimensions inches (millimeters)



48-Lead Mold Dual-In-Line Package (N)
Order Number DS8187N
NS Package Number N48A

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