Symphony™ Audio DSP56720/DSP56721

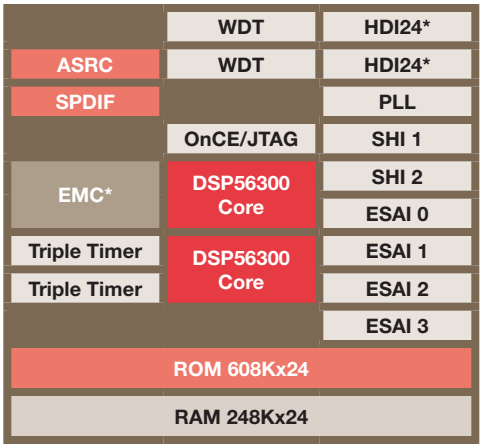
Target Applications

- A/V receivers
- Blu-ray and HD-DVD players
- Car audio/amplifiers
- Professional audio recording systems

Overview

Responding to the demand for increased memory and performance in advanced audio applications, Freescale has designed digital signal processing (DSP) chips that support multiple high-definition (HD) audio standards. The Symphony™ audio DSP56720 and DSP56721 represent the first in a complete family of multi-core 24-bit processors from Freescale, further broadening the company's expansive audio portfolio. The DSP56720 and DSP56721 retain code compatibility with Freescale's popular DSP56000 and DSP56300 core families of DSPs while enhancing its capabilities with many new features.

The Symphony audio DSP56720 and DSP56721 excel at audio processing for automotive and consumer audio applications requiring high million instructions per second (MIPS). Higher MIPS and memory requirements are driven by the new HD audio standards (Dolby® Digital Plus, Dolby® TrueHD, DTS-HD). In addition, the DSPs are optimal for the professional audio market requiring audio recording, signal processing and digital audio synthesis.



DSP56720/721 Block Diagram

** EMC available on DSP56720 only.*

** 16-bit version available on DSP56721 144LQFP only.*

Features	Benefits
Dual High-Performance 24-bit DSP56300 Cores	
• High-performance 200 MIPS per core using an internal 200 MHz clock at 1.0V core voltage • Dual data arithmetic logic units (ALU) with a 24 x 24-bit multiplier accumulator and a 56-bit barrel shifter • Eight-channel DMA controller per core • Stop and wait low-power standby modes	○ Designed to provide the high performance necessary for many audio applications ○ Dual-core architecture allows optimized use of memory and MIPS
On-Chip Debug Interface	
• Internal address tracing support and on-chip emulation (OnCE) module per core • JTAG port	○ Allows for real-time software development and software download to on-chip or on-board RAM ○ Allows for software running and debug with full-speed operation and breakpoint capability, and the ability to modify all user-accessible registers, memory and peripherals
On-Chip Memory Configuration	
• 248K x 24-bit words RAM • 608K x 24-bit words ROM • Partitioned into program memory space, X and Y data memory space • Shared memory between the two cores	○ Flexibility ○ Allows two address ALUs and the ability to feed two operands simultaneously to the data ALU ○ Provides flexibility to the user by allowing custom allocation of memory
External Memory Controller (EMC)	
• Supports external memories: SDRAM, SRAM, flash and EEPROM • External memory is accessible via either core and any memory space • Available on the 144 pin package on the DSP56720 only	○ Provides for memory expansion to either cost-effective SDRAM or fast SRAM ○ Provides flexibility in system design by providing memory expansion for one or both cores
Asynchronous Sample Rate Converter (ASRC)	
• Ten channels • Input and output sample rate 32 kHz to 192 kHz • Three input and output clock ratio conversions • Shared by the two cores	○ Allows multiple audio data rates in a system ○ Synchronizes up to three asynchronous audio streams

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S/PDIF Transceiver Module

- S/PDIF receiver module with four mux'd inputs
- S/PDIF transmitter module with two outputs
- Supports IEC958, IECG-1937 format

- Reduces system costs by integrating S/PDIF transceiver on-chip

Host Interface for DMA Support (HDI24)

- Support for multiplexed address/data buses
- 16-bit bond out available on DSP56721 144LQFP package only
- Future DSP5672x family derivatives may support 24-bits

- Allows for high-speed audio or control transfers

Four Enhanced Serial Audio Interfaces (ESAI)

- Two dedicated Tx and four selectable Tx/Rx signals
- TDM capable with up to 32 words per frame
- Supports many programmable protocols such as I^2S, Sony, AC97 and network
- Two ESAI ports per core

- Glueless connection to industry standard CODECS (I^2S, left justified, right justified and AC97)
- Full-duplex serial port for serial communications with DSPs, MPUs and MCUs

Dual Serial Host Interfaces (SHI)

- Serial peripheral interface (SPI) protocol
- Inter-IC (I^2C) protocol
- Support for 8-, 16- and 24-bit width data transfers

- High-speed synchronous communication between multiple DSPs or between DSP and MCU or between DSP and serial peripherals
- Designed to provide a simple, efficient method of data exchange between devices

Dual Triple Timer Module

- Timer, measurement, PWM, watchdog modes available
- Three timers per module, one module per core

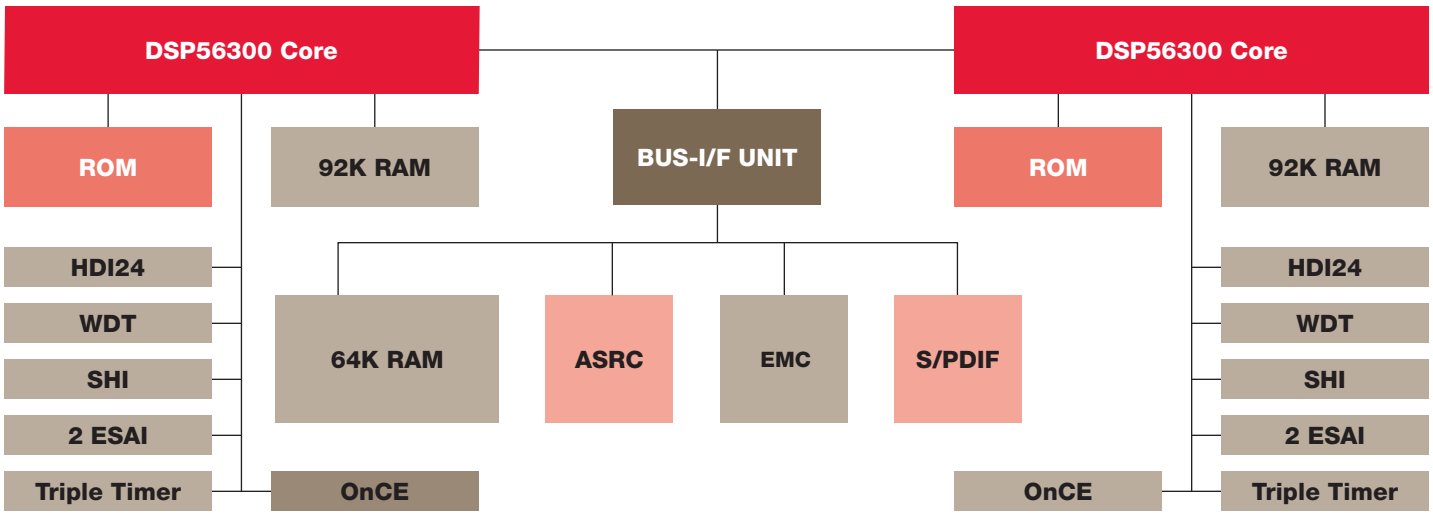
- Flexible, programmable timer system

Dual Hardware Watchdog Timers (WDT)

- Based on a 16-bit free-running down counter
- One WDT per core

- Allows recovery from runaway code

Symphony Audio DSP56720/DSP56721



Learn More: For additional information about Freescale's Symphony portfolio, visit **www.freescale.com/symphony**.

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