DSP56857

Preliminary Technical Data

DSP56857 16-bit Digital Signal Processor

- 120 MIPS at 120MHz
- 40K x 16-bit Program SRAM
- 24K x 16-bit Data SRAM
- 1K x 16-bit Boot ROM
- Six (6) independent channels of DMA
- Two (2) Enhanced Synchronous Serial Interfaces (ESSI)
- Two (2) Serial Communication Interfaces (SCI)
- Serial Port Interface (SPI)
- Four (4) dedicated GPIO
- 8-bit Parallel Host Interface
- General Purpose 16-bit Quad Timer
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Computer Operating Properly (COP)/Watchdog Timer
- Time-of-Day (TOD)
- 100 LQFP package
- Up to 47 GPIO

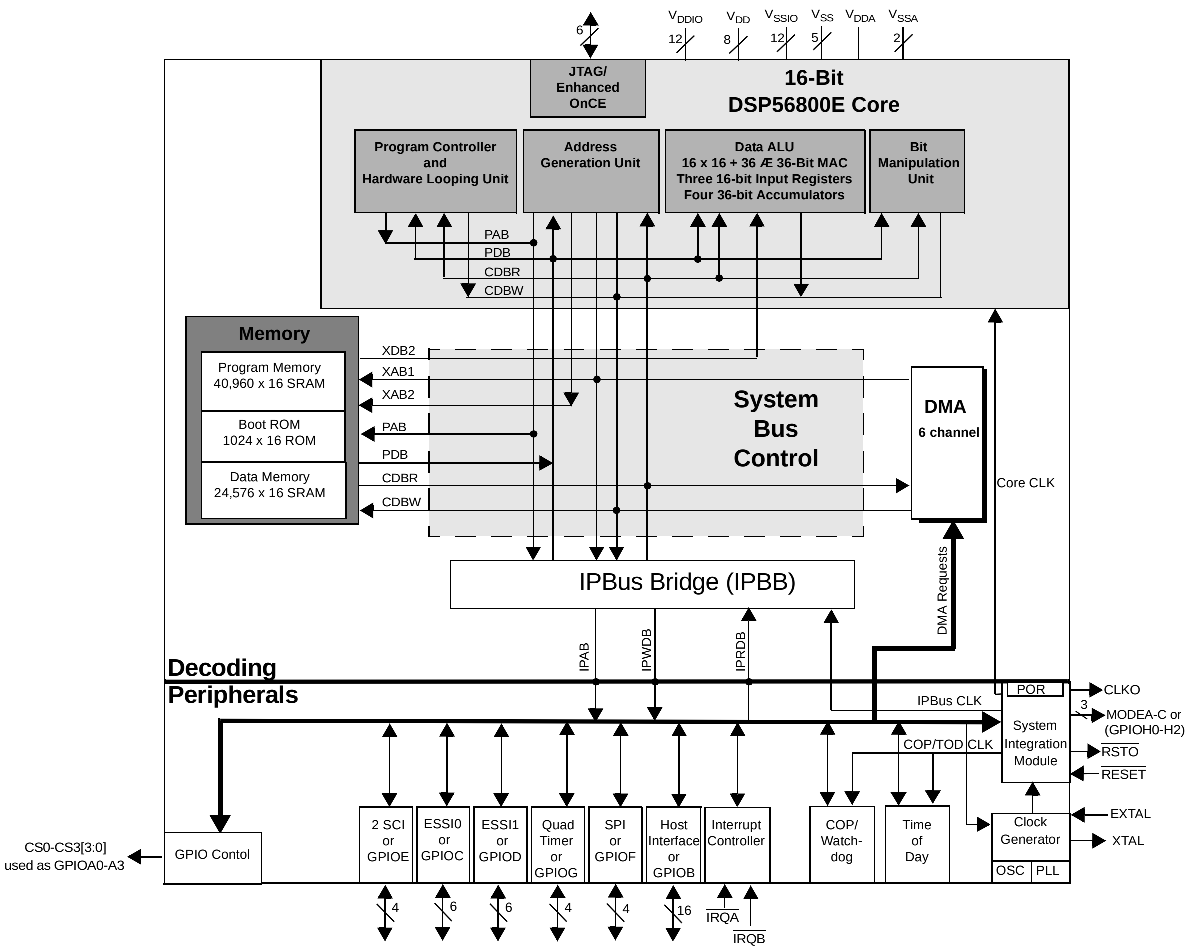


Figure 1. DSP56857 Block Diagram

Part 1 Overview

1.1 DSP56857 Features

1.1.1 Digital Signal Processing Core

- Efficient 16-bit DSP engine with dual Harvard architecture
- 120 Million Instructions Per Second (MIPS) at 120MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four (4)36-bit accumulators including extension bits
- 16-bit bidirectional shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three (3) internal address buses
- Four (4) internal data buses
- Instruction set supports both DSP and controller functions
- Four (4) hardware interrupt levels
- Five (5) software interrupt levels
- Controller-style addressing modes and instructions for compact code
- Efficient C Compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced OnCE debug programming interface

1.1.2 Memory

- Harvard architecture permits up to three (3) simultaneous accesses to program and data memory
- On-Chip Memory
  - 40K × 16-bit Program RAM
  - 24K × 16-bit Data RAM
  - 1K × 16-bit Boot ROM
  - Chip Select Logic used as dedicated GPIO

1.1.3 Peripheral Circuits for DSP56857

- General Purpose 16-bit Quad Timer*
- Two Serial Communication Interfaces (SCI)*
- Serial Peripheral Interface (SPI) Port*
- Two (2) Enhanced Synchronous Serial Interface (ESSI) modules*
- Computer Operating Properly (COP)/Watchdog Timer
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging
- Six (6) independent channels of DMA

- 8-bit Parallel Host Interface*
- Time of Day
- Up to 47 GPIO

* Each peripheral I/O can be used alternately as a General Purpose I/O if not needed

1.1.4 Energy Information

- Fabricated in high-density CMOS with 3.3V, TTL-compatible digital inputs
- Wait and Stop modes available

1.2 DSP56857 Description

The DSP56857 is a member of the DSP56800E core-based family of Digital Signal Processors (DSPs). It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the DSP56857 is well-suited for many applications. The DSP56857 includes many peripherals that are especially useful for low-end Internet appliance applications and low-end client applications such as telephony; portable devices; Internet audio; and point-of-sale systems, such as noise suppression; ID tag readers; sonic/subsonic detectors; security access devices; remote metering; sonic alarms.

The DSP56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C Compilers, enabling rapid development of optimized control applications.

The DSP56857 supports program execution from either internal or external memories. Two data operands can be accessed from the on-chip Data RAM per instruction cycle. The DSP56857 also provides two external dedicated interrupt lines, and up to 47 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The DSP56857 DSP controller includes 40K words of Program RAM, 24K words of Data RAM and 1K of Boot ROM.

This DSP controller also provides a full set of standard programmable peripherals that include 8-bit parallel Host Interface, Two Enhanced Synchronous Serial Interfaces (ESSI), one Serial Peripheral Interface (SPI), two Serial Communications Interfaces (SCI), and one Quad Timer. The ESSIs, SPI, SCIs IO and Quad Timer can be used as General Purpose Input/Outputs when its primary function is not required.

1.3 “Best in Class” Development Environment

The SDK (Software Development Kit) provides fully-debugged peripheral drivers, libraries and interfaces that allow a programmer to create his own unique C application code independent of component architecture. The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, the SDK, CodeWarrior, and EVMs create a complete, scalable tools solution for easy, fast and efficient development.

1.4 Product Documentation

The four documents listed in **Table 1** are required for a complete description of and proper design with the DSP56857. Documentation is available from local Motorola distributors, Motorola semiconductor sales offices, Motorola Literature Distribution Centers, or online at www.motorola.com/semiconductors/.

Table 1. DSP56857 Chip Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the DSP56800E architecture, 16-bit DSP core processor and the instruction set	DSP56800ERM/D
DSP56857 User's Manual	Detailed description of memory, peripherals, and interfaces of the DSP56857	DSP5685xUM/D
DSP56857 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	DSP56857/D
DSP56857 Product Brief	Summary description and block diagram of the DSP56857 core, memory, peripherals and interfaces	DSP56857PB/D

1.5 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
"asserted"	A high true (active high) signal is high or a low true (active low) signal is low.
"deasserted"	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:

Signal/Symbol	Logic State	Signal State	Voltage[1]
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for VIL, VOL, VIH, and VOH are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the DSP56857 are organized into functional groups, as shown in **Table 2** and as illustrated in **Figure 2**. In **Table 3** each table row describes the package pin and the signal or signals present.

Table 2. Functional Group Pin Allocations

Functional Group	Number of Pins
Power (V_{DD}, V_{DDIO}, or V_{DDA})	(8, 12, 1)[1]
Ground (V_{SS}, V_{SSIO}, or V_{SSA})	(5, 12, 2)[1]
PLL and Clock	3
Chip Select Logic used as dedicated GPIO	4
Interrupt and Program Control	7[2]
Host Interface (HI)*	16[3]
Enhanced Synchronous Serial Interface (ESSI0) Port*	6
Enhanced Synchronous Serial Interface (ESSI1) Port*	6
Serial Communications Interface (SCI0) Ports*	2
Serial Communications Interface (SCI1) Ports*	2
Serial Peripheral Interface (SPI) Port*	4
Quad Timer Module Port*	4
JTAG/Enhanced On-Chip Emulation (EOnCE)	6

*Alternately, GPIO pins

1. $V_{DD} = V_{DD\ CORE}$, $V_{SS} = V_{SS\ CORE}$, $V_{DDIO} = V_{DD\ IO}$, $V_{SSIO} = V_{SS\ IO}$, $V_{DDA} = V_{DD\ ANA}$, $V_{SSA} = V_{SS\ ANA}$
2. MODE A, MODE B and MODE C can be used as GPIO after the bootstrap process has completed.
3. The following Host Interface signals are multiplexed: HRWB to $\overline{HRD}$, $\overline{HDS}$ to $\overline{HWR}$, $\overline{HREQ}$ to $\overline{HTRQ}$ and $\overline{HACK}$ to HRRQ.

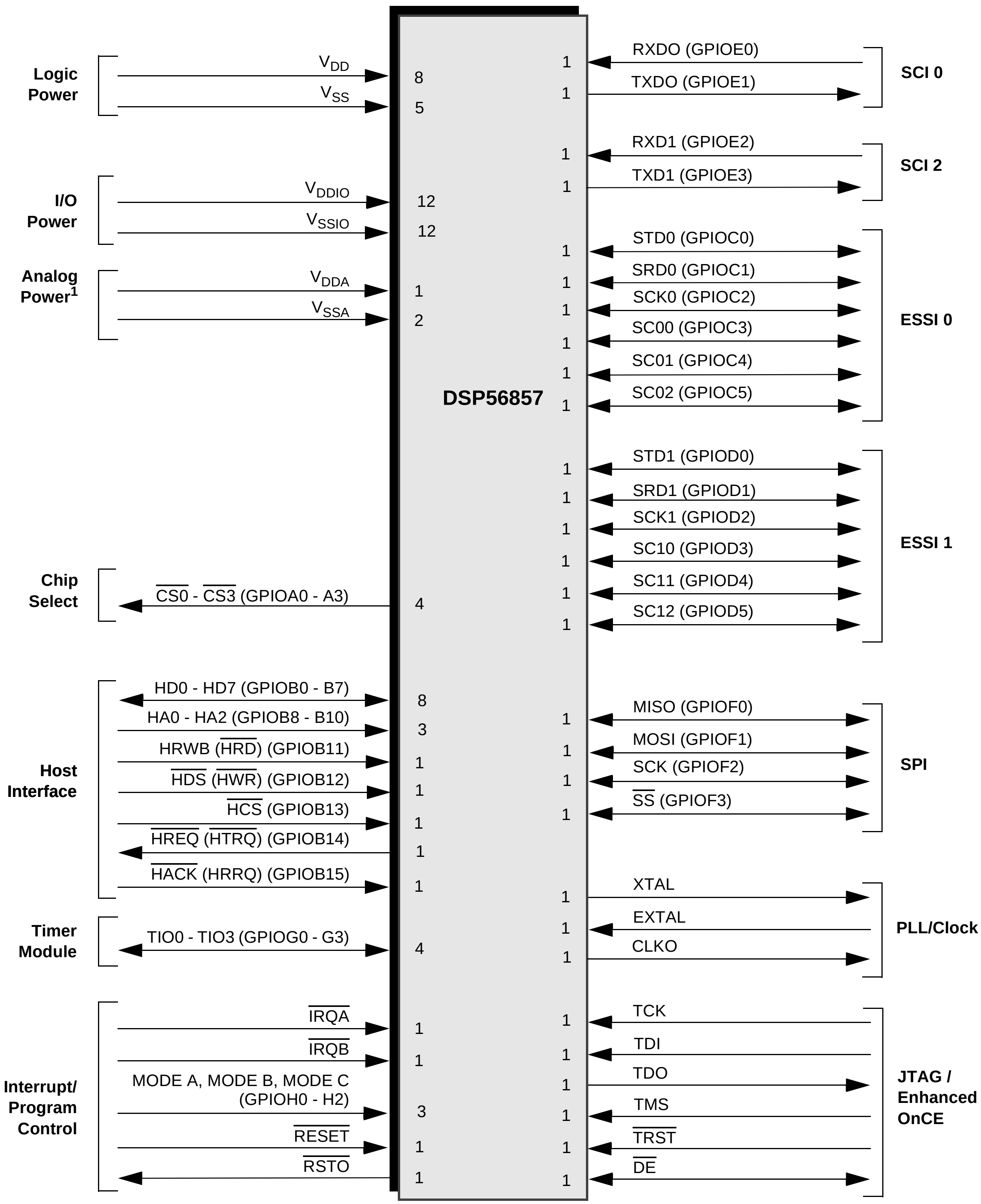


Figure 2. DSP56857 Signals Identified by Functional Group[2]

1. Specifically for PLL, OSC, and POR.
2. Alternate pin functions are shown in parentheses.

Part 3 Signals and Package Information

All digital inputs have a weak internal pull-up circuit associated with them. These pull-up circuits are enabled by default. Exceptions:

1. When a pin has GPIO functionality, the pull-up may be disabled under software control.
2. MODE A, MODE B, and MODE C pins have no pull-up.
3. TCK has a weak pull-down circuit always active.
4. Bidirectional I/O pullups automatically disable when the output is enabled.

This table is presented consistently with the *Signals Identified by Functional Group* figure.

1. **BOLD** entries in the *Type* column represents the state of the pin just out of reset.
2. Ouput(Z) means an output in a High-Z condition..

Table 3. DSP56857 Signal and Package Information for the 100-pin LQFP

Pin No.	Signal Name	Type	Description
8	V_{DD}	V_{DD}	**Power (V_{DD})**—These pins provide power to the internal structures of the chip, and should all be attached to V_{DD}.
25	V_{DD}		
36	V_{DD}		
50	V_{DD}		
59	V_{DD}		
60	V_{DD}		
76	V_{DD}		
87	V_{DD}		
9	V_{SS}	V_{SS}	**Ground (V_{SS})**—These pins provide grounding for the internal structures of the chip and should all be attached to V_{SS}.
37	V_{SS}		
38	V_{SS}		
61	V_{SS}		
88	V_{SS}		
5	V_{DDIO}	V_{DDIO}	**Power (V_{DDIO})**—These pins provide power for all I/O and ESD structures of the chip, and should all be attached to V_{DDIO} (3.3V).
6	V_{DDIO}		
13	V_{DDIO}		
34	V_{DDIO}		
45	V_{DDIO}		
47	V_{DDIO}		

Table 3. DSP56857 Signal and Package Information for the 100-pin LQFP

Pin No.	Signal Name	Type	Description
48	V_{DDIO}	V_{DDIO}	**Power (V_{DDIO})**—These pins provide power for all I/O and ESD structures of the chip, and should all be attached to V_{DDIO} (3.3V).
53	V_{DDIO}		
72	V_{DDIO}		
80	V_{DDIO}		
90	V_{DDIO}		
98	V_{DDIO}		
7	V_{SSIO}	V_{SSIO}	**Ground (V_{SSIO})**—These pins provide grounding for all I/O and ESD structures of the chip and should all be attached to V_{SS}.
14	V_{SSIO}		
35	V_{SSIO}		
46	V_{SSIO}		
49	V_{SSIO}		
54	V_{SSIO}		
73	V_{SSIO}		
82	V_{SSIO}		
89	V_{SSIO}		
91	V_{SSIO}		
99	V_{SSIO}		
100	V_{SSIO}		
17	V_{DDA}	V_{DDA}	**Analog Power (V_{DDA})**—These pins supply an analog power source.
18	V_{SSA}	V_{SSA}	**Analog Ground (V_{SSA})**—This pin supplies an analog ground.
19	V_{SSA}		
55	$\overline{CS0}$ GPIOA0	**Output** **Input**/Output	**External Chip Select ($\overline{CS0}$)**—This pin is used as a dedicated GPIO. **Port A GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
56	$\overline{CS1}$ GPIOA1	**Output** **Input**/Output	**External Chip Select ($\overline{CS1}$)**—This pin is used as a dedicated GPIO. **Port A GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.

Table 3. DSP56857 Signal and Package Information for the 100-pin LQFP

Pin No.	Signal Name	Type	Description
57	$\overline{\text{CS2}}$ GPIOA2	**Output** **Input**/Output	**External Chip Select ($\overline{\textbf{CS2}}$)**—This pin is used as a dedicated GPIO. **Port A GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
58	$\overline{\text{CS3}}$ GPIOA3	**Output** **Input**/Output	**External Chip Select ($\overline{\textbf{CS3}}$)**—This pin is used as a dedicated GPIO**.** **Port A GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
22	HD0 GPIOB0	**Input** Input/Output	**Host Address (HD0)—**This input provides the address selection for HI registers. This pin is disconnected internally. **Port B GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
23	HD1 GPIOB1	**Input** Input/Output	**Host Address (HD1)—**This input provides the address selection for HI registers. This pin is disconnected internally. **Port B GPIO (1)**—This pin is a General Purpose I/O (GPIO) pins when not configured for host port usage.
24	HD2 GPIOB2	**Input** Input/Output	**Host Address (HD2)—**This input provides the address selection for HI registers. This pin is disconnected internally. **Port B GPIO (2)**—This pin is a General Purpose I/O (GPIO) pins when not configured for host port usage.
29	HD3 GPIOB3	**Input** Input/Output	**Host Address (HD3)—**This input provides the address selection for HI registers. This pin is disconnected internally. **Port B GPIO (3)**—This pin is a General Purpose I/O (GPIO) pins when not configured for host port usage.
30	HD4 GPIOB4	**Input** Input/Output	**Host Address (HD4)—**This input provides the address selection for HI registers. This pin is disconnected internally. **Port B GPIO (4)**—This pin is a General Purpose I/O (GPIO) pins when not configured for host port usage.

Table 3. DSP56857 Signal and Package Information for the 100-pin LQFP

Pin No.	Signal Name	Type	Description
31	HD5	**Input**	**Host Address (HD5)—**This input provides the address selection for HI registers. This pin is disconnected internally.
	GPIOB5	Input/Output	**Port B GPIO (5)**—This pin is a General Purpose I/O (GPIO) pins when not configured for host port usage.
32	HD6	**Input**	**Host Address (HD6)—**This input provides the address selection for HI registers. This pin is disconnected internally.
	GPIOB6	Input/Output	**Port B GPIO (6)**—This pin is a General Purpose I/O (GPIO) pins when not configured for host port usage.
33	HD7	**Input**	**Host Address (HD7)—**This input provides the address selection for HI registers. This pin is disconnected internally.
	GPIOB7	Input/Output	**Port B GPIO (7)**—This pin is a General Purpose I/O (GPIO) pins when not configured for host port usage.
62	HA0	**Input**	**Host Address (HA0)**—This input provides the address selection for HI registers. This pin is disconnected internally.
	GPIOB8	Input/Output	**Port B GPIO (8)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
63	HA1	**Input**	**Host Address (HA1)**—This input provides the address selection for HI registers. This pin is disconnected internally.
	GPIOB9	Input/Output	**Port B GPIO (9)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
64	HA2	**Input**	**Host Address (HA2)**—This input provides the address selection for HI registers. This pin is disconnected internally.
	GPIOB10	Input/Output	**Port B GPIO (10)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.

Table 3. DSP56857 Signal and Package Information for the 100-pin LQFP

Pin No.	Signal Name	Type	Description
65	HRWB	**Input**	**Host Read/Write (HRWB)**—When the HI08 is programmed to interface to a single-data-strobe host bus and the HI function is selected, this signal is the Read/Write input . These pins are disconnected internally.
	$\overline{HRD}$	**Input**	**Host Read Data ($\overline{HRD}$)**—This signal is the Read Data input when the HI08 is programmed to interface to a double-data-strobe host bus and the HI function is selected.
	GPIOB11	Input/Output	**Port B GPIO (11)** —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
83	$\overline{HDS}$	**Input**	**Host Data Strobe ($\overline{HDS}$)**—When the HI08 is programmed to interface to a single-data-strobe host bus and the HI function is selected, this input enables a data transfer on the HI when $\overline{HCS}$ is asserted. These pins are disconnected internally.
	$\overline{HWR}$	**Input**	**Host Write Enable ($\overline{HWR}$)**—This signal is the Write Data input when the HI08 is programmed to interface to a double-data-strobe host bus and the HI function is selected.
	GPIOB12	Input/Output	**Port B GPIO (12)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
84	$\overline{HCS}$	**Input**	**Host Chip Select ($\overline{HCS}$)**—This input is the chip select input for the Host Interface. These pins are disconnected internally.
	GPIOB13	Input/Output	**Port B GPIO (13)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
85	$\overline{HREQ}$	**Open Drain Output**	**Host Request ($\overline{HREQ}$)**—When the HI08 is programmed for HRMS=0 functionality (typically used on a single-data- strobe bus), this open drain output is used by the HI to request service from the host processor. The $\overline{HREQ}$ may be connected to an interrupt request pin of a host processor, a transfer request of a DMA controller, or a control input of external circuitry. These pins are disconnected internally.
	$\overline{HTRQ}$	**Open Drain Output**	**Transmit Host Request ($\overline{HTRQ}$)**—This signal is the Transmit Host Request output when the HI08 is programmed for HRMS=1 functionality and is typically used on a double-data-strobe bus.
	GPIOB14	Input/Output	**Port B GPIO (14)** —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.

Table 3. DSP56857 Signal and Package Information for the 100-pin LQFP

Pin No.	Signal Name	Type	Description
86	$\overline{\text{HACK}}$	**Input**	**Host Acknowledge ($\overline{\text{HACK}}$)**—When the HI08 is programmed for HRMS=0 functionality (typically used on a single-data-strobe bus), this input has two functions: (1) provide a Host Acknowledge signal for DMA transfers or (2) to control handshaking and provide a Host Interrupt Acknowledge compatible with the MC68000 family processors. These pins are disconnected internally during reset.
	HRRQ	Open Drain Output	**Receive Host Request (HRRQ)**—This signal is the Receive Host Request output when the HI08 is programmed for HRMS=1 functionality and is typically used on a double-data-strobe bus.
	GPIOB15	Input/Output	**Port B GPIO (15)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
81	TIO0	**Input**/Output	**Timer Input/Output (TIO0)**—This pin can be independently configured to be either a timer input source or an output flag.
	GPIOG0	Input/Output	**Port G GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
79	TIO1	**Input**/Output	**Timer Input/Output (TIO1)**—This pin can be independently configured to be either a timer input source or an output flag.
	GPIOG1	Input/Output	**Port G GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
78	TIO2	**Input**/Output	**Timer Input/Output (TIO2)**—This pin can be independently configured to be either a timer input source or an output flag.
	GPIOG2	Input/Output	**Port G GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
77	TIO3	**Input**/Output	**Timer Input/Output (TIO3)**—This pin can be independently configured to be either a timer input source or an output flag.
	GPIOG3	Input/Output	**Port G GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
15	$\overline{\text{IRQA}}$	Input	**External Interrupt Request A and B**—The $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ inputs are asynchronous external interrupt requests that indicate that an external device is requesting service. A Schmitt trigger input is used for noise immunity. They can be programmed to be level-sensitive or negative-edge- triggered. If level-sensitive triggering is selected, an external pull-up resistor is required for Wired-OR operation.
16	$\overline{\text{IRQB}}$		
10	MODE A	**Input**	**Mode Select (MODE A)**—During the bootstrap process MODE A selects one of the eight bootstrap modes.
	GPIOH0	Input/Output	**Port H GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin after the bootstrap process has completed.

Table 3. DSP56857 Signal and Package Information for the 100-pin LQFP

Pin No.	Signal Name	Type	Description
11	MODE B GPIOH1	**Input** Input/Output	**Mode Select (MODE B)**—During the bootstrap process MODE B selects one of the eight bootstrap modes. **Port H GPIOH1**—This pin is a General Purpose I/O (GPIO) pin after the bootstrap process has completed.
12	MODE C GPIOH2	**Input** Input/Output	**Mode Select (MODE C)**—During the bootstrap process MODE C selects one of the eight bootstrap modes. **Port H GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin after the bootstrap process has completed.
28	$\overline{\text{RESET}}$	Input	**Reset ($\overline{\text{RESET}}$)**—This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the DSP is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the $\overline{\text{RESET}}$ pin is deasserted, the initial chip operating mode is latched from the MODE A, MODE B, and MODE C pins. To ensure complete hardware reset, $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$ should be asserted together. The only exception occurs in a debugging environment when a hardware DSP reset is required and it is necessary not to reset the JTAG/Enhanced OnCE module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$.
27	$\overline{\text{RSTO}}$	Output	**Reset Output ($\overline{\text{RSTO}}$)**—This output is asserted on any reset condition (external reset, low voltage, software or COP).
51	RXD0 GPIOE0	**Input** Input/Output	**Serial Receive Data 0 (RXD0)**—This input receives byte-oriented serial data and transfers it to the SCI 0 receive shift register. **Port E GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
52	TXD0 GPIOE1	**Output(Z)** Input/Output	**Serial Transmit Data 0 (TXD0)**—This signal transmits data from the SCI 0 transmit data register. **Port E GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
74	RXD1 GPIOE2	**Input** Input/Output	**Serial Receive Data 1 (RXD1)**—This input receives byte-oriented serial data and transfers it to the SCI 1 receive shift register. **Port E GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
75	TXD1 GPIOE3	**Output(Z)** Input/Output	**Serial Transmit Data 1 (TXD1)**—This signal transmits data from the SCI 1 transmit data register. **Port E GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.

Table 3. DSP56857 Signal and Package Information for the 100-pin LQFP

Pin No.	Signal Name	Type	Description
92	STD0	Output	**ESSI Transmit Data (STD0)**—This output pin transmits serial data from the ESSI Transmitter Shift Register.
	GPIOC0	**Input**/Output	**Port C GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
93	SRD0	Input	**ESSI Receive Data (SRD0)**—This input pin receives serial data and transfers the data to the ESSI Receive Shift Register.
	GPIOC1	**Input**/Output	**Port C GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
94	SCK0	**Input**/Output	**ESSI Serial Clock (SCK0)**—This bidirectional pin provides the serial bit rate clock for the transmit section of the ESSI. The clock signal can be continuous or gated and can be used by both the transmitter and receiver in synchronous mode.
	GPIOC2	Input/Output	**Port C GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
95	SC00	**Input**/Output	**ESSI Serial Control Pin 0 (SC00)**—The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin will be used for the receive clock I/O. For synchronous mode, this pin is used either for transmitter1 output or for serial I/O flag 0.
	GPIOC3	Input/Output	**Port C GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
96	SC01	**Input**/Output	**ESSI Serial Control Pin 1 (SC01)**—The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin is the receiver frame sync I/O. For synchronous mode, this pin is used either for transmitter2 output or for serial I/O flag 1.
	GPIOC4	Input/Output	**Port C GPIO (4)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
97	SC02	**Input**/Output	**ESSI Serial Control Pin 2 (SC02)**—This pin is used for frame sync I/O. SC02 is the frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. When configured as an output, this pin is the internally generated frame sync signal. When configured as an input, this pin receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
	GPIOC5	Input/Output	**Port C GPIO (5)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
66	STD1	Output	**ESSI Transmit Data (STD1)**—This output pin transmits serial data from the ESSI Transmitter Shift Register.
	GPIOD0	**Input**/Output	**Port D GPIOD0**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.

Table 3. DSP56857 Signal and Package Information for the 100-pin LQFP

Pin No.	Signal Name	Type	Description
67	SRD1	Input	**ESSI Receive Data (SRD1)**—This input pin receives serial data and transfers the data to the ESSI Receive Shift Register.
	GPIOD1	**Input/**Output	**Port D GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
68	SCK1	**Input**/Output	**ESSI Serial Clock (SCK1)**—This bidirectional pin provides the serial bit rate clock for the transmit section of the ESSI. The clock signal can be continuous or gated and can be used by both the transmitter and receiver in synchronous mode.
	GPIOD2	Input/Output	**Port D GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
69	SC10	**Input**/Output	**ESSI Serial Control Pin 0 (SC10)**—The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin will be used for the receive clock I/O. For synchronous mode, this pin is used either for transmitter1 output or for serial I/O flag 0.
	GPIOD3	Input/Output	**Port D GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
70	SC11	**Input**/Output	**ESSI Serial Control Pin 1 (SC11)**—The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin is the receiver frame sync I/O. For synchronous mode, this pin is used either for transmitter2 output or for serial I/O flag 1.
	GPIOD4	Input/Output	**Port D GPIO (4)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
71	SC12	**Input**/Output	**ESSI Serial Control Pin 2 (SC12)**—This pin is used for frame sync I/O. SC02 is the frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. When configured as an output, this pin is the internally generated frame sync signal. When configured as an input, this pin receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
	GPIOD5	Input/Output	**Port D GPIO (5)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
1	MISO	**Input**/Output	**SPI Master In/Slave Out (MISO)**—This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. The driver on this pin can be configured as an open-drain driver by the SPI's Wired-OR mode (WOM) bit when this pin is configured for SPI operation.
	GPIOF0	Input/Output	**Port F GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.

Table 3. DSP56857 Signal and Package Information for the 100-pin LQFP

Pin No.	Signal Name	Type	Description
2	MOSI	Input/ **Output (Z)**	**SPI Master Out/Slave In (MOSI)**—This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data. The driver on this pin can be configured as an open-drain driver by the SPI's WOM bit when this pin is configured for SPI operation.
	GPIOF1	Input/Output	**Port F GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as input or output pin.
3	SCK	**Input/**Output	**SPI Serial Clock (SCK)**—This bidirectional pin provides a serial bit rate clock for the SPI. This gated clock signal is an input to a slave device and is generated as an output by a master device. Slave devices ignore the SCK signal unless the $\overline{SS}$ pin is active low. In both master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. The driver on this pin can be configured as an open-drain driver by the SPI's WOM bit when this pin is configured for SPI operation. When using Wired-OR mode, the user must provide an external pull-up device.
	GPIOF2	Input/Output	**Port F GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
4	$\overline{SS}$	**Input**	**SPI Slave Select ($\overline{SS}$)**—This input pin selects a slave device before a master device can exchange data with the slave device. $\overline{SS}$ must be low before data transactions and must stay low for the duration of the transaction. The $\overline{SS}$ line of the master must be held high.
	GPIOF3	Input/Output	**Port F GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
20	XTAL	Input/**Output**	**Crystal Oscillator Output (XTAL)**—This output connects the internal crystal oscillator output to an external crystal. If an external clock source other than a crystal oscillator is used, XTAL must be used as the input.
21	EXTAL	Input	**External Crystal Oscillator Input (EXTAL)**—This input should be connected to an external crystal. If an external clock source other than a crystal oscillator is used, EXTAL must be tied off. See Section 4.5.2
26	CLKO	Output	**Clock Output (CLKO)**—This pin outputs a buffered clock signal. When enabled, this signal is the system clock divided by four.
44	TCK	Input	**Test Clock Input (TCK)**—This input pin provides a gated clock to synchronize the test logic and to shift serial data to the JTAG/Enhanced OnCE port. The pin is connected internally to a pull-down resistor.

Table 3. DSP56857 Signal and Package Information for the 100-pin LQFP

Pin No.	Signal Name	Type	Description
42	TDI	Input	**Test Data Input (TDI)**—This input pin provides a serial input data stream to the JTAG/Enhanced OnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
41	TDO	Output (Z)	**Test Data Output (TDO)**—This tri-statable output pin provides a serial output data stream from the JTAG/Enhanced OnCE port. It is driven in the Shift-IR and Shift-DR controller states, and changes on the falling edge of TCK.
43	TMS	Input	**Test Mode Select Input (TMS)**—This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
40	$\overline{\text{TRST}}$	Input	**Test Reset ($\overline{\text{TRST}}$)**—As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, $\overline{\text{TRST}}$ should be asserted whenever $\overline{\text{RESET}}$ is asserted. The only exception occurs in a debugging environment, since the Enhanced OnCE/JTAG module is under the control of the debugger. In this case it is not necessary to assert $\overline{\text{TRST}}$ when asserting $\overline{\text{RESET}}$. Outside of a debugging environment $\overline{\text{RESET}}$ should be permanently asserted by grounding the signal, thus disabling the Enhanced OnCE/JTAG module on the DSP.
39	$\overline{\text{DE}}$	**Input**/Output	**Debug Event ($\overline{\text{DE}}$)**—This is an open-drain, bidirectional, active low signal. As an input, it is a means of entering debug mode of operation from an external command controller. As an output, it is a means of acknowledging that the chip has entered debug mode. This pin is connected internally to a weak pull-up resistor.

Part 4 Specifications

4.1 General Characteristics

The DSP56857 is fabricated in high-density CMOS with 5-volt tolerant TTL-compatible digital inputs. The term "5-volt tolerant" refers to the capability of an I/O pin, built on a 3.3V compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V tolerant capability therefore offers the power savings of 3.3V I/O levels while being able to receive 5V levels without being damaged.

Absolute maximum ratings given in **Table 4** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

The DSP56857 DC/AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 4. Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Supply voltage, core	V_{DD}[1]	V_{SS} – 0.3	V_{SS} + 2.0	V
Supply voltage, IO Supply voltage, analog	V_{DDIO}[2] V_{DDIO}[2]	V_{SSIO} – 0.3 V_{SSA} – 0.3	V_{SSIO} + 4.0 V_{DDA} + 4.0	V
Digital input voltages Analog input voltages (XTAL, EXTAL)	V_{IN} V_{INA}	V_{SSIO} – 0.3 V_{SSA} – 0.3	V_{SSIO} + 5.5 V_{DDA} + 0.3	V
Current drain per pin excluding V_{DD}, GND	I	—	8	mA
Junction temperature	T_J	-40	120	°C
Storage temperature range	T_{STG}	-55	150	°C

1. V_{DD} must not exceed V_{DDIO}
2. V_{DDIO} and V_{DDA} must not differ by more that 0.5V

Table 5. Recommended Operating Conditions

Characteristic	Symbol	Min	Max	Unit
Supply voltage for Logic Power	V_{DD}	1.62	1.98	V
Supply voltage for I/O Power	V_{DDIO}	3.0	3.6	V
Supply voltage for Analog Power	V_{DDA}	3.0	3.6	V
Ambient operating temperature	T_A	-40	85	°C
PLL clock frequency[1]	f_{pll}	—	240	MHz

Table 5. Recommended Operating Conditions

Characteristic	Symbol	Min	Max	Unit
Operating Frequency[2]	f_{op}	—	120	MHz
Frequency of peripheral bus	f_{ipb}	—	60	MHz
Frequency of external clock	f_{clk}	—	240	MHz
Frequency of oscillator	f_{osc}	2	4	MHz
Frequency of clock via XTAL	f_{xtal}	—	240	MHz
Frequency of clock via EXTAL	f_{extal}	2	4	MHz

1. Assumes clock source is direct clock to EXTAL or crystal oscillator running 2-4MHz. PLL must be enabled, locked, and selected. The actual frequency depends on the source clock frequency and programming of the CGM module.
2. Master clock is derived from on of the following four sources:
   $f_{clk} = f_{xtal}$ when the source clock is the direct clock to EXTAL
   $f_{clk} = f_{pll}$ when PLL is selected
   $f_{clk} = f_{osc}$ when the source clock is the crystal oscillator and PLL is not selected
   $f_{clk} = f_{extal}$ when the source clock is the direct clock to EXTAL and PLL is not selected

Table 6. Thermal Characteristics[1]

Characteristic	100-pin LQFP		
	Symbol	Value	Unit
Thermal resistance junction-to-ambient (estimated)	θ_{JA}	41.2	°C/W
I/O pin power dissipation	$P_{I/O}$	User Determined	W
Power dissipation	P_D	$P_D = (I_{DD} \times V_{DD}) + P_{I/O}$	W
Maximum allowed P_D	P_{DMAX}	$(T_J - T_A) / \theta_{JA}$	×C

1. See **Section 6.1** for more detail.

4.2 DC Electrical Characteristics

Table 7. DC Electrical Characteristics

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = –40°$ to +120°C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (XTAL/EXTAL)	V_{IHC}	$V_{DDA} – 0.8$	V_{DDA}	$V_{DDA} + 0.3$	V
Input low voltage (XTAL/EXTAL)	V_{ILC}	-0.3	—	0.5	V
Input high voltage	V_{IH}	2.0	—	5.5	V

Table 7. DC Electrical Characteristics (Continued)

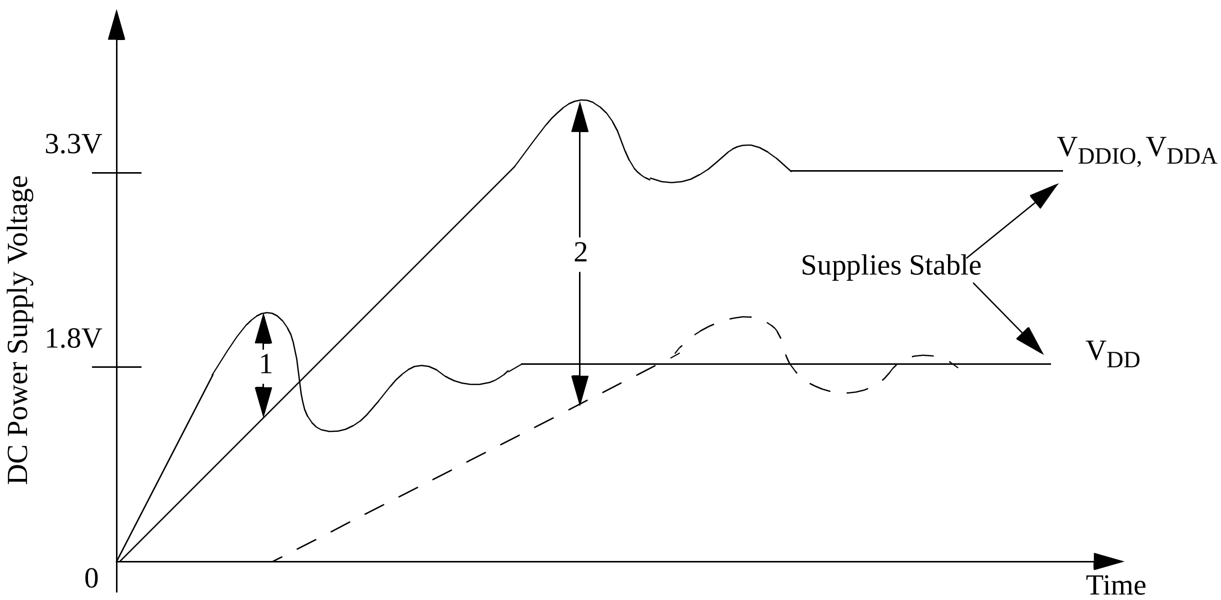
Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, V_{DD} = 1.62-1.98V, $V_{DDIO} = V_{DDA}$ = 3.0–3.6V, T_A = –40° to +120°C, $C_L \leq$ 50pF, f_{op} = 120MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input low voltage	V_{IL}	-0.3	—	0.8	V
Input current low (pullups disabled)	I_{IL}	-1	—	1	µA
Input current high (pullups disabled)	I_{IH}	-1	—	1	µA
Output tri-state current low	I_{OZL}	-10	—	10	µA
Output tri-state current high	I_{OZH}	-10	—	10	µA
Output High Voltage	V_{OH}	V_{DD} – 0.7	—	—	V
Output Low Voltage	V_{OL}	—	—	0.4	V
Output High Current	I_{OH}	8	—	16	mA
Output Low Current	I_{OL}	8	—	16	mA
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF
V_{DD} supply current @ nominal voltage and 25 °C Run [1] Deep Stop[2] Light Stop[3]	I_{DD}[4]	 — — —	 70 100 2.6	 — — —	 mA µA mA
V_{DDIO} supply current @ nominal voltage and 25 °C Run[5]	I_{DDIO}	 —	 40	 —	 mA
V_{DDA} supply current @ nominal voltage and 25 °C Deep Stop[2]	I_{DDA}	 —	 60	 —	 µA
Low Voltage Interrupt[6]	V_{EI}	—	2.5	2.85	V
Low Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power on Reset[7]	POR	—	1.5	2.0	V

1. Run (operating) I_{DD} measured using external square wave clock source (f_{osc} = 4MHz) into XTAL. All inputs 0.2V from rail; no DC loads; outputs unloaded. All ports configured as inputs; measured with all modules enabled. PLL set to 240MHz out. Running Core, performing 50% NOP and 50% FIR. Clock at 120 MHz.
2. Deep Stop Mode - Operation frequency = 4 MHz, PLL set to 4 MHz, crystal oscillator and time of day module operating.
3. Light Stop Mode - Operation frequency = 120 MHz, PLL set to 240 MHz, crystal oscillator and time of day module operating.
4. I_{DD} includes current for core logic, internal memories, and all internal peripheral logic circuitry.
5. Running core and performing external memory access. Clock at 120 MHz.
6. When V_{DD} drops below V_{EI} max value, an interrupt is generated.
7. Power-on reset occurs whenever the digital supply drops below 1.8V. While power is ramping up, this signal remains active for as long as the internal 2.5V is below 1.8V no matter how long the ramp up rate is. The internally regulated voltage is typically 100 mV less than V_{DD} during ramp up until 2.5V is reached, at which time it self-regulates.

4.3 Supply Voltage Sequencing and Separation Cautions

Figure 3 shows two situations to avoid in sequencing the V_{DD} and V_{DDIO}, V_{DDA} supplies.



Notes: 1. V_{DD} rising before V_{DDIO}, V_{DDA}
2. V_{DDIO}, V_{DDA} rising much faster than V_{DD}

Figure 3. Supply Voltage Sequencing and Separation Cautions

V_{DD} should not be allowed to rise early (1). This is usually avoided by running the regulator for the V_{DD} supply (1.8V) from the voltage generated by the 3.3V V_{DDIO} supply, see Figure 4. This keeps V_{DD} from rising faster than V_{DDIO}.

V_{DD} should not rise so late that a large voltage difference is allowed between the two supplies (2). Typically this situation is avoided by using external discrete diodes in series between supplies, as shown in Figure 4. The series diodes forward bias when the difference between V_{DDIO} and V_{DD} reaches approximately 2.1, causing V_{DD} to rise as V_{DDIO} ramps up. When the V_{DD} regulator begins proper operation, the difference between supplies will typically be 0.8V and conduction through the diode chain reduces to essentially leakage current. During supply sequencing, the following general relationship should be adhered to:
$V_{DDIO} \geq V_{DD} \geq (V_{DDIO} - 2.1V)$

In practice, V_{DDA} is typically connected directly to V_{DDIO} with some filtering.

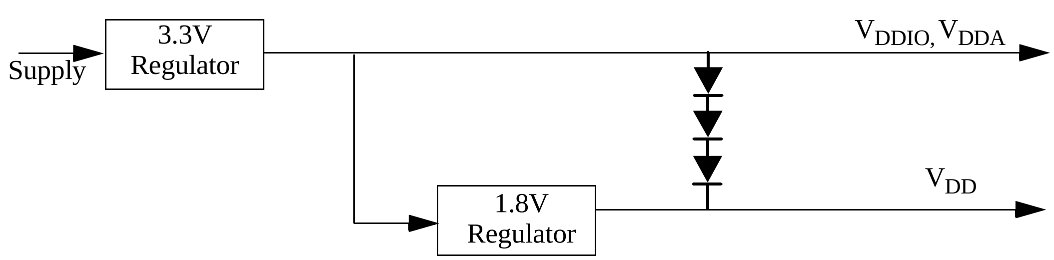
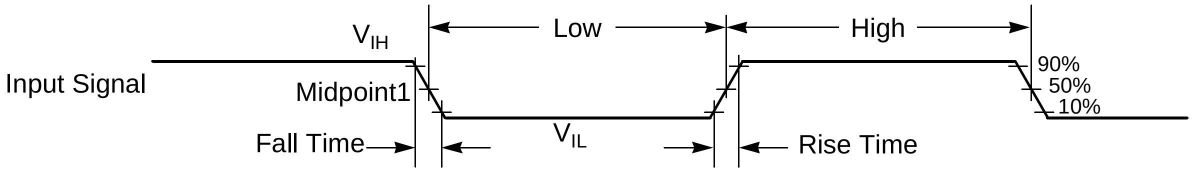


Figure 4. Example Circuit to Control Supply Sequencing

4.4 AC Electrical Characteristics

Timing waveforms in Section 4.4 are tested with a V_{IL} maximum of 0.8V and a V_{IH} minimum of 2.0V for all pins except XTAL, which is tested using the input levels in Section 4.2. In Figure 5 the levels of V_{IH} and V_{IL} for an input signal are shown.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 5. Input Signal Measurement References

Figure 6 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

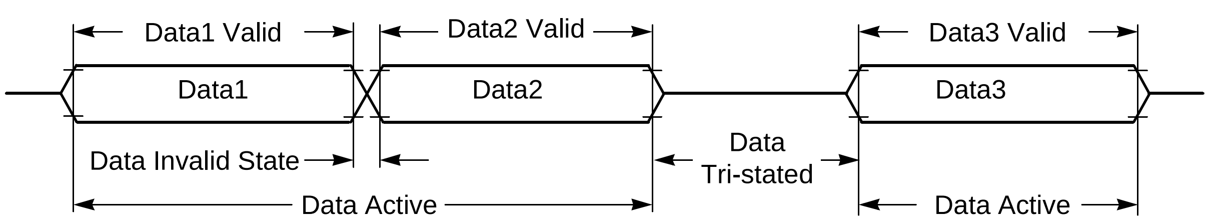


Figure 6. Signal States

4.5 External Clock Operation

The DSP56857 system clock can be derived from a crystal or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal must be connected between the EXTAL and XTAL pins.

4.5.1 Crystal Oscillator

The internal oscillator is designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in **Table 9**. In **Figure 7** a typical crystal oscillator circuit is shown. Follow the crystal supplier's recommendations when selecting a crystal, because crystal parameters determine the component values required to provide maximum stability and reliable start-up. The crystal and associated components should be mounted as close as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

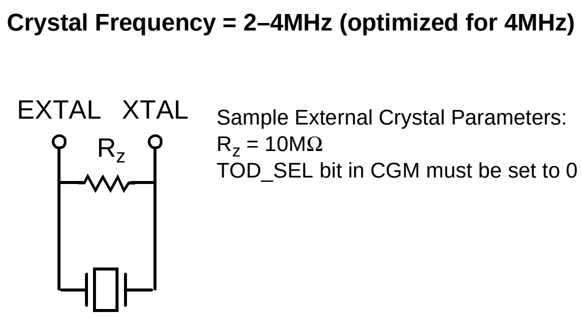


Figure 7. Crystal Oscillator

4.5.2 High Speed External Clock Source (> 4MHz)

The recommended method of connecting an external clock is given in **Figure 8.** The external clock source is connected to XTAL and the EXTAL pin is held at ground, V_{DDA}, or $V_{DDA}/2$. The TOD_SEL bit in CGM must be set to 0.

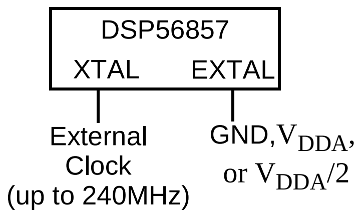


Figure 8. Connecting a High Speed External Clock Signal using XTAL

4.5.3 Low Speed External Clock Source (2-4MHz)

The recommended method of connecting an external clock is given in **Figure 9.** The external clock source is connected to XTAL and the EXTAL pin is held at $V_{DDA}/2$. The TOD_SEL bit in CGM must be set to 0.

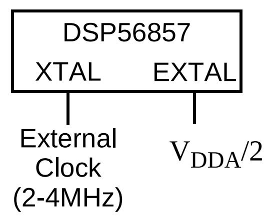


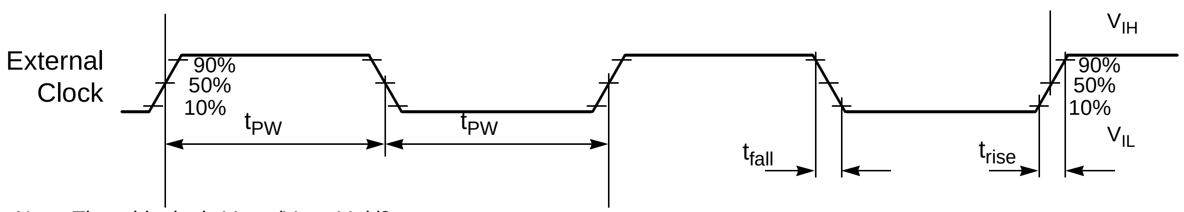
Figure 9. Connecting a Low Speed External Clock Signal using XTAL

Table 8. External Clock Operation Timing Requirements[4]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62$-1.98V, $V_{DDIO} = V_{DDA} = 3.0$–3.6V, $T_A = –40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	0	—	240	MHz
Clock Pulse Width[4]	t_{PW}	6.25	—	—	ns
External clock input rise time[2, 4]	t_{rise}	—	—	TBD	ns
External clock input fall time[3, 4]	t_{fall}	—	—	TBD	ns

1. See **Figure 8** for details on using the recommended connection of an external clock driver.
2. External clock input rise time is measured from 10% to 90%.
3. External clock input fall time is measured from 90% to 10%.
4. Parameters listed are guaranteed by design.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 10. External Clock Timing

Table 9. PLL Timing

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62$-1.98V, $V_{DDIO} = V_{DDA} = 3.0$–3.6V, $T_A = –40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL[1]	f_{osc}	2	4	4	MHz
PLL output frequency	f_{clk}	40	—	240	MHz
PLL stabilization time [2]	t_{plls}	—	1	10	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 4MHz input crystal.
2. This is the minimum time required after the PLL setup is changed to ensure reliable operation.

4.6 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Table 10. Reset, Stop, Wait, Mode Select, and Interrupt Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62$-1.98V, $V_{DDIO} = V_{DDA} = 3.0$–3.6V, $T_A = –40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Typ Min	Typ Max	Unit	See Figure
Minimum $\overline{RESET}$ Assertion Duration[3]	t_{RA}	30	—	ns	Figure 11
Edge-sensitive Interrupt Request Width	t_{IRW}	1T + 3	—	ns	Figure 12
$\overline{IRQA}$, $\overline{IRQB}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	t_{IG}	—	18T	ns	Figure 13
$\overline{IRQA}$ Width Assertion to Recover from Stop State	t_{IW}	2T	—	ns	Figure 14
Delay from $\overline{IRQA}$ Assertion to Fetch of first instruction (exiting Stop)[4] Fast[5] Normal[6, 7]	t_{IF}	 — —	 13T 25ET	 ns ns	Figure 14
$\overline{RSTO}$ pulse width[7] normal operation internal reset mode	t_{RSTO}	 128ET 8ET	 — —	 — —	Figure 15

1. In the formulas, T = clock cycle. For f_{op} = 120MHz operation and f_{ipb} = 60MHz, T = 8.33ns.
2. Parameters listed are guaranteed by design.
3. At reset, the PLL is disabled and bypassed. The part is then put into Run mode and t_{clk} assumes the period of the source clock, t_{xtal}, t_{extal} or t_{osc}.
4. This interrupt instruction fetch is visible on the pins only in Mode 3.
5. Fast stop mode:

   Fast stop recovery applies when external clocking is in use (direct clocking to XTAL) or when fast stop mode recovery is requested (OMR bit 6 is set to 1). In both cases the PLL and the master clock are unaffected by stop mode entry. Recovery takes one less cycle and t_{clk} will continue with the same value it had before stop mode was entered.
6. Normal stop mode:

   As a power saving feature, normal stop mode disables and bypasses the PLL. Stop mode will then shut down the master clock, recovery will take an extra cycle (to restart the clock), and t_{clk} will resume at the input clock source rate.
7. ET = External Clock period; for an external crystal frequency of 4MHz, ET=250ns.

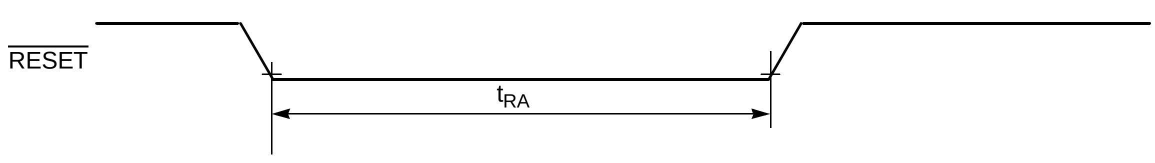


Figure 11. Asynchronous Reset Timing

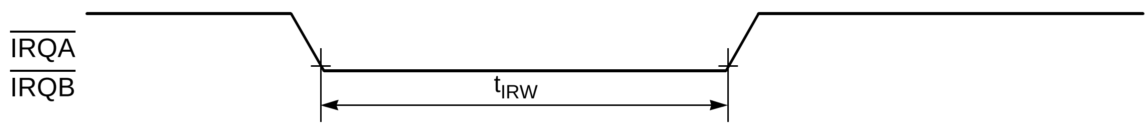


Figure 12. External Interrupt Timing (Negative-Edge-Sensitive)

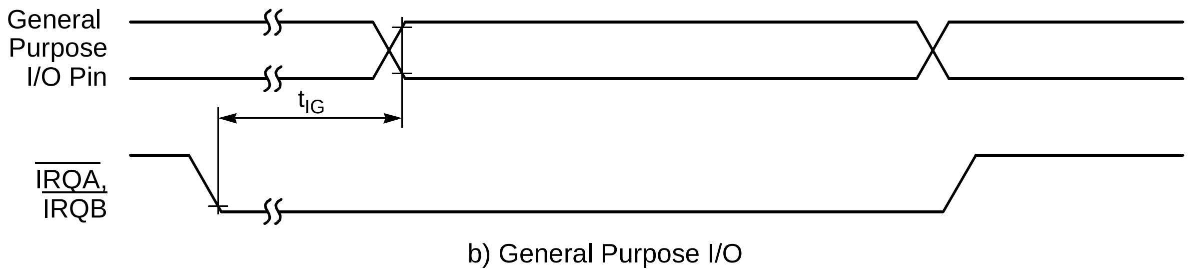


Figure 13. External Level-Sensitive Interrupt Timing

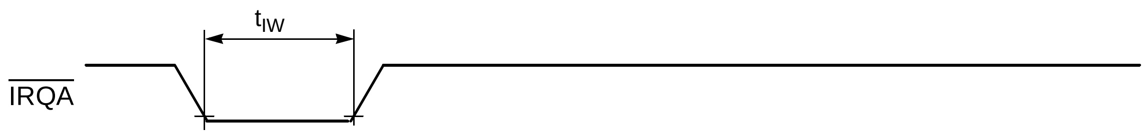


Figure 14. Recovery from Stop State Using Asynchronous Interrupt Timing

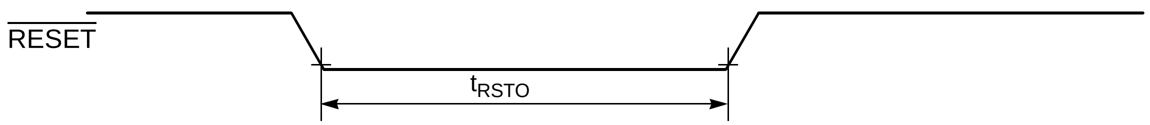


Figure 15. Reset Output Timing

4.7 Host Interface Port

Table 11. Host Interface Port Timing[1]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
Access time	TACKDV	—	13	ns	Figure 18
Disable time	TACKDZ	3	—	ns	Figure 18
Time to disassert	TACKREQH	3.5	9	ns	Figure 18 Figure 21
Lead time	TREQACKL	0	—	ns	Figure 18 Figure 21
Access time	TRADV	—	13	ns	Figure 19 Figure 20
Disable time	TRADX	5	—	ns	Figure 19 Figure 20
Disable time	TRADZ	3	—	ns	Figure 19 Figure 20
Setup time	TDACKS	3	—	ns	Figure 21
Hold time	TACKDH	1	—	ns	Figure 21
Setup time	TADSS	3	—	ns	Figure 22 Figure 23
Hold time	TDSAH	1	—	ns	Figure 22 Figure 23
Pulse width	TWDS	5	—	ns	Figure 22 Figure 23
Time to re-assert 1. After second write in 16-bit mode 2. After first write in 16-bit mode or after write in 8-bit mode	TACKREQL	4T + 5 5	5T + 9 13	ns ns	Figure 18, Figure 21

1. The formulas: T = clock cycle. f ipb = 60MHz, T = 16.7ns.

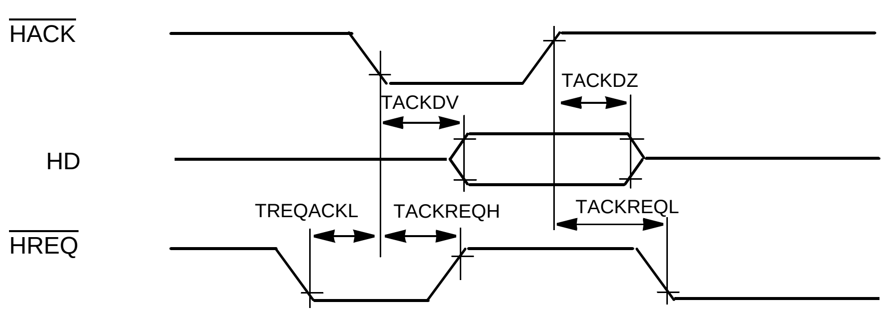


Figure 16. DSP-to-Host DMA Read Model

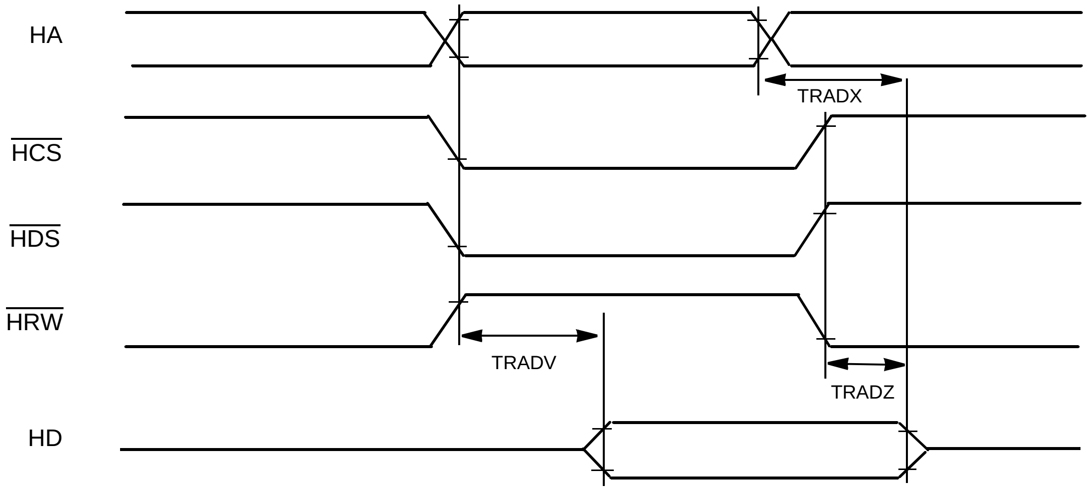


Figure 17. Single Strobe Read Mode

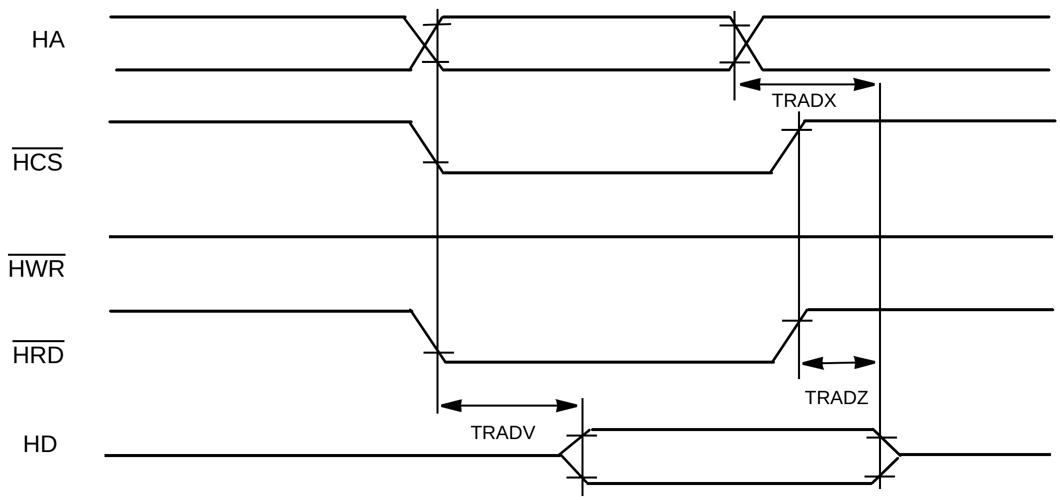


Figure 18. Dual Strobe Read Mode

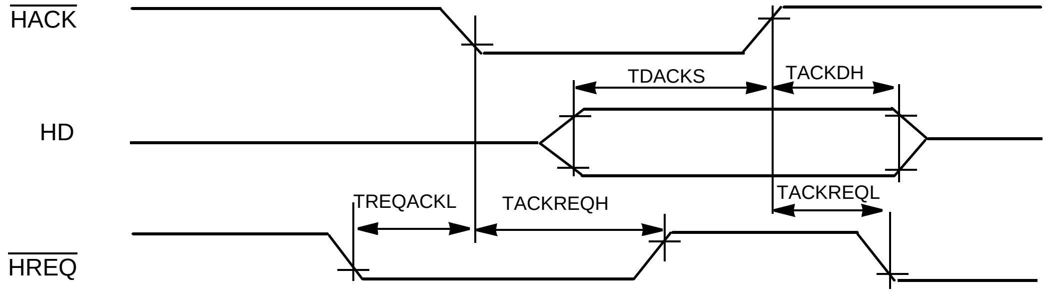


Figure 19. Host-to-DSP DMA Write Mode

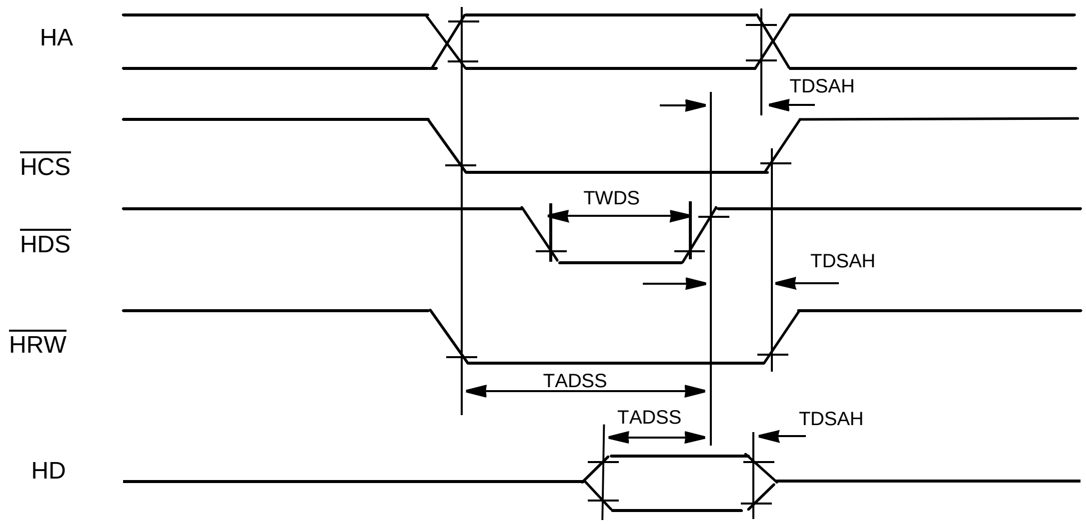


Figure 20. Single Strobe Write Mode

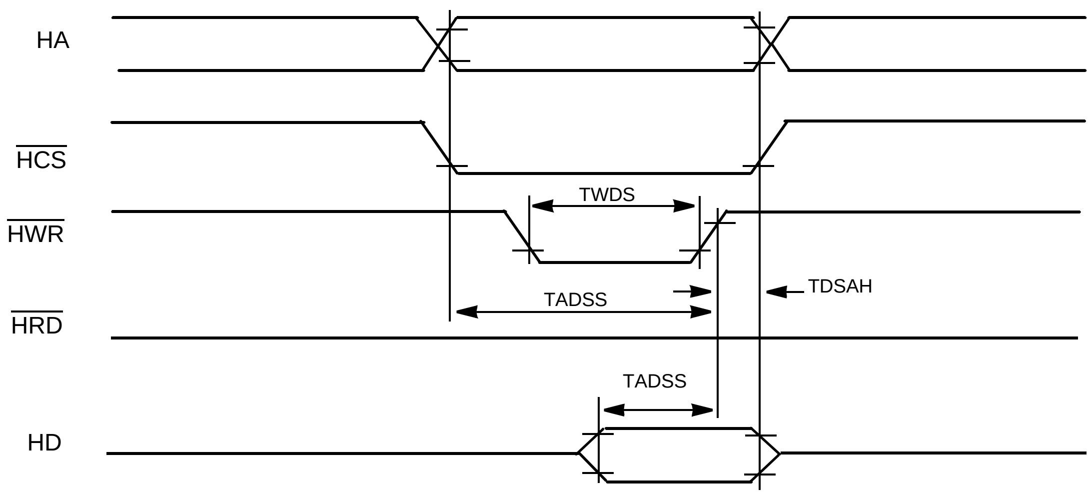


Figure 21. Dual Strobe Write Mode

4.8 Serial Peripheral Interface (SPI) Timing

Table 12. SPI Timing [1]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62$-1.98V, $V_{DDIO} = V_{DDA} = 3.0$–3.6V, $T_A = -40°$ to $+120°C$, $C_L \leq 50pF$, $f_{op} = 120MHz$

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 25 25	 — —	 ns ns	Figures 22, 23, 24, 25
Enable lead time Master Slave	t_{ELD}	 — 12.5	 — —	 ns ns	Figure 25
Enable lag time Master Slave	t_{ELG}	 — 12.5	 — —	 ns ns	Figure 25
Clock (SCLK) high time Master Slave	t_{CH}	 9 12.5	 — —	ns ns	Figures 22, 23, 24, 25
Clock (SCLK) low time Master Slave	t_{CL}	 12 12.5	 — —	 ns ns	Figure 25
Data set-up time required for inputs Master Slave	t_{DS}	 10 2	 — —	 ns ns	Figures 22, 23, 24, 25
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figures 22, 23, 24, 25
Access time (time to data active from high-impedance state) Slave	t_A	 5	 15	ns ns	Figure 25
Disable time (hold time to high-impedance state) Slave	t_D	 2	 9	ns ns	Figure 25
Data valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 2 14	 ns ns	Figures 22, 23, 24, 25
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	Figures 22, 23, 24, 25
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	Figures 22, 23, 24, 25
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	Figures 22, 23, 24, 25

1. Parameters listed are guaranteed by design.

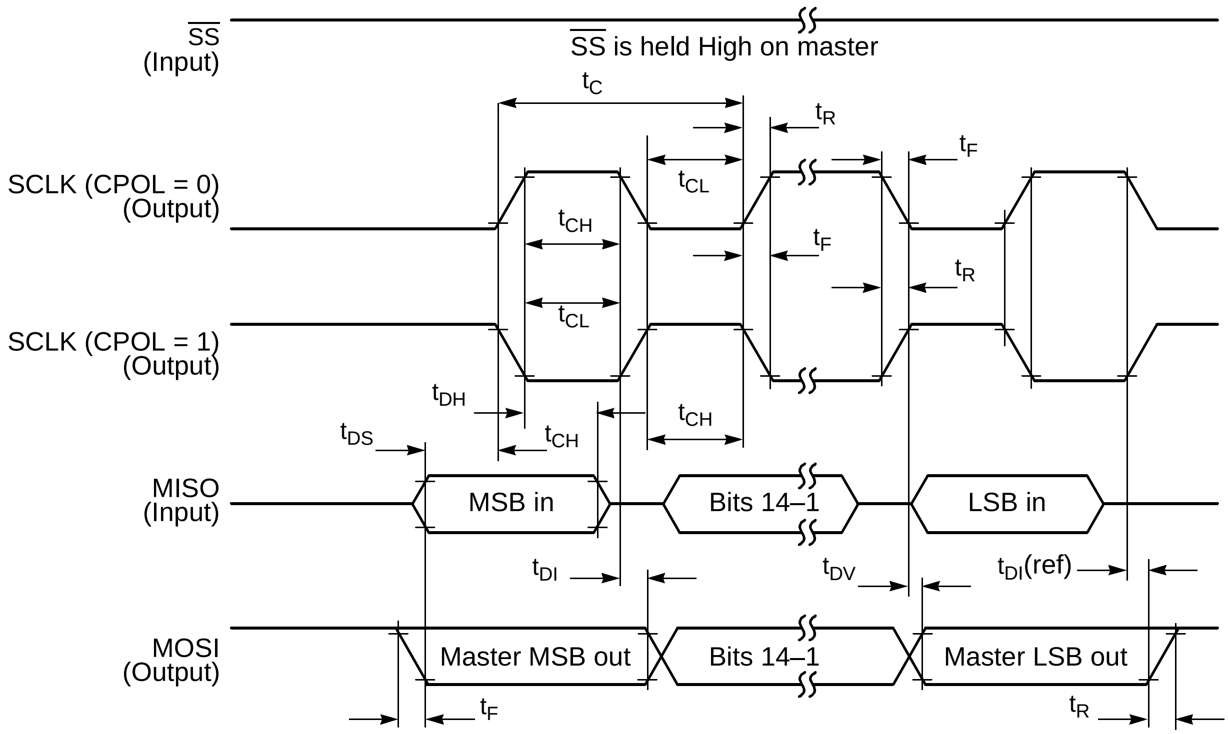


Figure 22. SPI Master Timing (CPHA = 0)

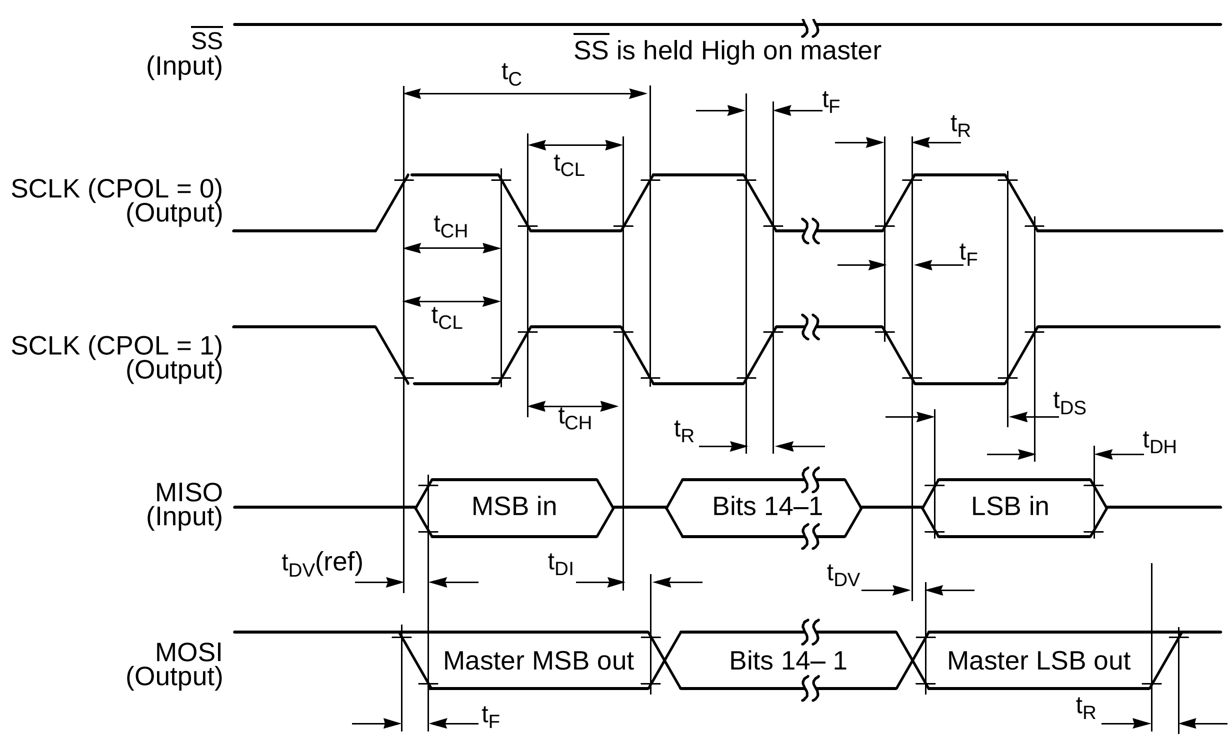


Figure 23. SPI Master Timing (CPHA = 1)

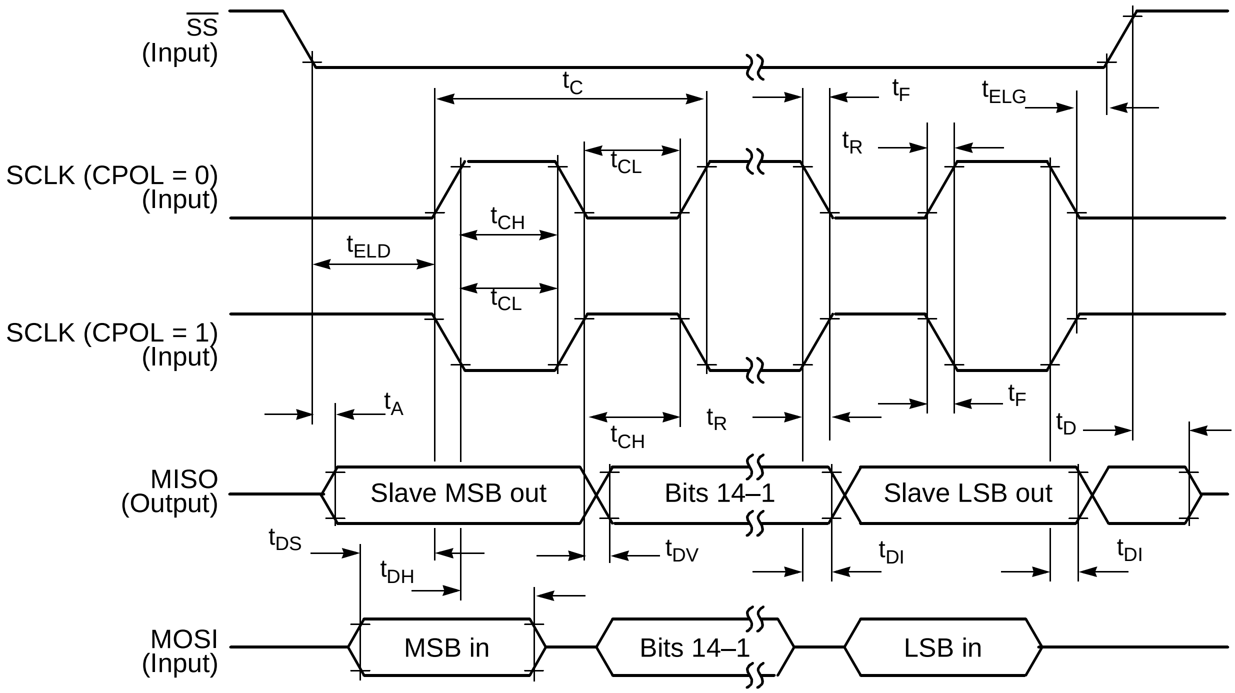


Figure 24. SPI Slave Timing (CPHA = 0)

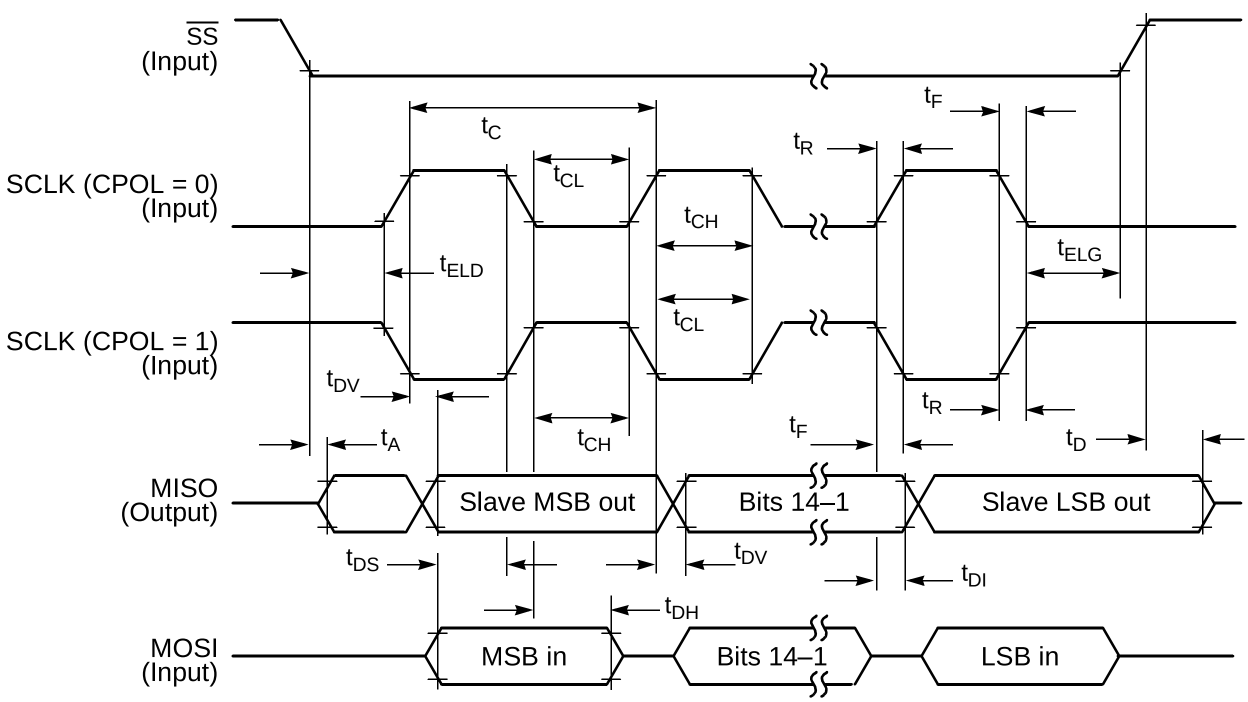


Figure 25. SPI Slave Timing (CPHA = 1)

4.9 Quad Timer Timing

Table 13. Quad Timer Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62$-1.98V, $V_{DDIO} = V_{DDA} = 3.0$–3.6V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Max	Unit
Timer input period	P_{IN}	2T + 3	—	ns
Timer input high/low period	P_{INHL}	1T + 3	—	ns
Timer output period	P_{OUT}	2T - 3	—	ns
Timer output high/low period	P_{OUTHL}	1T - 3	—	ns

1. In the formulas listed, T = clock cycle. For f_{op} = 120MHz operation and fipb = 60MHz, T = 8.33ns.
2. Parameters listed are guaranteed by design.

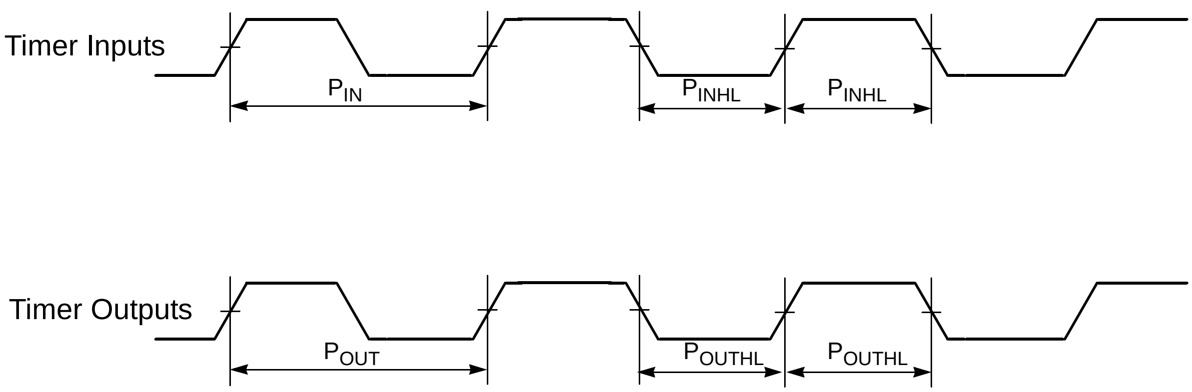


Figure 26. Timer Timing

4.10 Enhanced Synchronous Serial Interface (ESSI) Timing

Table 14. ESSI Master Mode[1] Switching Characteristics

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62$-1.98V, $V_{DDIO} = V_{DDA} = 3.0$–3.6V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Parameter	Symbol	Min	Typ	Max	Units
SCK frequency	fs	—	—	15[2]	MHz
SCK period[3]	t_{SCKW}	66.7	—	—	ns
SCK high time	t_{SCKH}	33.4[4]	—	—	ns
SCK low time	t_{SCKL}	33.4[4]	—	—	ns
Output clock rise/fall time	—	—	4	—	ns
Delay from SCK high to SC2 (bl) high - Master[5]	t_{TFSBHM}	-1.0	—	1.0	ns
Delay from SCK high to SC2 (wl) high - Master[5]	t_{TFSWHM}	-1.0	—	1.0	ns

Table 14. ESSI Master Mode[1] Switching Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62$-1.98V, $V_{DDIO} = V_{DDA} = 3.0$–3.6V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Parameter	Symbol	Min	Typ	Max	Units
Delay from SC0 high to SC1 (bl) high - Master[5]	t_{RFSBHM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (wl) high - Master[5]	t_{RFSWHM}	-1.0	—	1.0	ns
Delay from SCK high to SC2 (bl) low - Master[5]	t_{TFSBLM}	-1.0	—	1.0	ns
Delay from SCK high to SC2 (wl) low - Master[5]	t_{TFSWLM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (bl) low - Master[5]	t_{RFSBLM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (wl) low - Master[5]	t_{RFSWLM}	-1.0	—	1.0	ns
SCK high to STD enable from high impedance - Master	t_{TXEM}	-0.1	—	2	ns
SCK high to STD valid - Master	t_{TXVM}	-0.1	—	2	ns
SCK high to STD not valid - Master	t_{TXNVM}	-0.1	—	—	ns
SCK high to STD high impedance - Master	t_{TXHIM}	-4	—	0	ns
SRD Setup time before SC0 low - Master	t_{SM}	4	—	—	ns
SRD Hold time after SC0 low - Master	t_{HM}	4	—	—	ns
Synchronous Operation (in addition to standard internal clock parameters)					
SRD Setup time before SCK low - Master	t_{TSM}	4	—	—	ns
SRD Hold time after SCK low - Master	t_{THM}	4	—	—	ns

1. Master mode is internally generated clocks and frame syncs
2. Max clock frequency is IP_clk/4 = 60MHz / 4 = 15MHz for an 120MHz part.
3. All the timings for the ESSI are given for a non-inverted serial clock polarity (TSCKP=0 in SCR2 and RSCKP=0 in SCSR) and a non-inverted frame sync (TFSI=0 in SCR2 and RFSI=0 in SCSR). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal SCK/SC0 and/or the frame sync SC2/SC1 in the tables and in the figures.
4. 50 percent duty cycle
5. bl = bit length; wl = word length

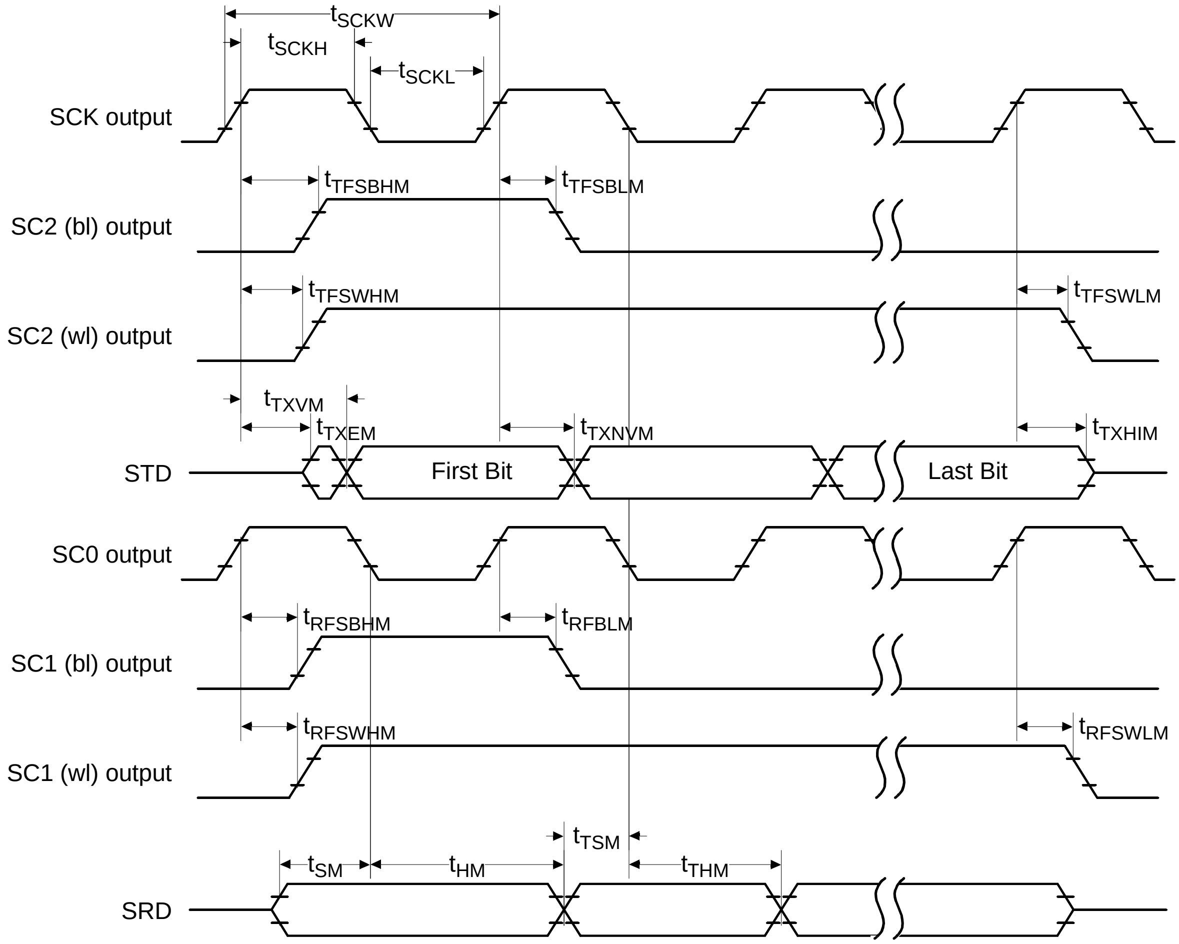


Figure 27. Master Mode Timing Diagram

Table 15: ESSI Slave Mode[1] Switching Characteristics

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, V_{DD} = 1.62-1.98V, $V_{DDIO} = V_{DDA}$ = 3.0–3.6V, T_A = –40° to +120°C, $C_L \leq$ 50pF, f_{op} = 120MHz

Parameter	Symbol	Min	Typ	Max	Units
SCK frequency	fs	—	—	15[2]	MHz
SCK period[3]	t_{SCKW}	66.7	—	—	ns
SCK high time	t_{SCKH}	33.4[4]	—	—	ns
SCK low time	t_{SCKL}	33.4[4]	—	—	ns
Output clock rise/fall time	—	—	4	—	ns
Delay from SCK high to SC2 (bl) high - Slave[5]	t_{TFSBHS}	-1	—	29	ns
Delay from SCK high to SC2 (wl) high - Slave[5]	t_{TFSWHS}	-1	—	29	ns
Delay from SC0 high to SC1 (bl) high - Slave[5]	t_{RFSBHS}	-1	—	29	ns

Table 15: ESSI Slave Mode[1] Switching Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62$-1.98V, $V_{DDIO} = V_{DDA} = 3.0$–3.6V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Parameter	Symbol	Min	Typ	Max	Units
Delay from SC0 high to SC1 (wl) high - Slave[5]	t_{RFSWHS}	-1	—	29	ns
Delay from SCK high to SC2 (bl) low - Slave[5]	t_{TFSBLS}	-29	—	29	ns
Delay from SCK high to SC2 (wl) low - Slave[5]	t_{TFSWLS}	-29	—	29	ns
Delay from SC0 high to SC1 (bl) low - Slave[5]	t_{RFSBLS}	-29	—	29	ns
Delay from SC0 high to SC1 (wl) low - Slave[5]	t_{RFSWLS}	-29	—	29	ns
SCK high to STD enable from high impedance - Slave	t_{TXES}	—	—	15	ns
SCK high to STD valid - Slave	t_{TXVS}	4	—	15	ns
SC2 high to STD enable from high impedance (first bit) - Slave	t_{FTXES}	4	—	15	ns
SC2 high to STD valid (first bit) - Slave	t_{FTXVS}	4	—	15	ns
SCK high to STD not valid - Slave	t_{TXNVS}	4	—	15	ns
SCK high to STD high impedance - Slave	t_{TXHIS}	4	—	15	ns
SRD Setup time before SC0 low - Slave	t_{SS}	4	—	—	ns
SRD Hold time after SC0 low - Slave	t_{HS}	4	—	—	ns
Synchronous Operation (in addition to standard external clock parameters)					
SRD Setup time before SCK low - Slave	t_{TSS}	4	—	—	ns
SRD Hold time after SCK low - Slave	t_{THS}	4	—	—	ns

1. Slave mode is externally generated clocks and frame syncs
2. Max clock frequency is IP_clk/4 = 60MHz / 4 = 15MHz for a 120MHz part.
3. All the timings for the ESSI are given for a non-inverted serial clock polarity (TSCKP=0 in SCR2 and RSCKP=0 in SCSR) and a non-inverted frame sync (TFSI=0 in SCR2 and RFSI=0 in SCSR). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal SCK/SC0 and/or the frame sync SC2/SC1 in the tables and in the figures.
4. 50 percent duty cycle
5. bl = bit length; wl = word length

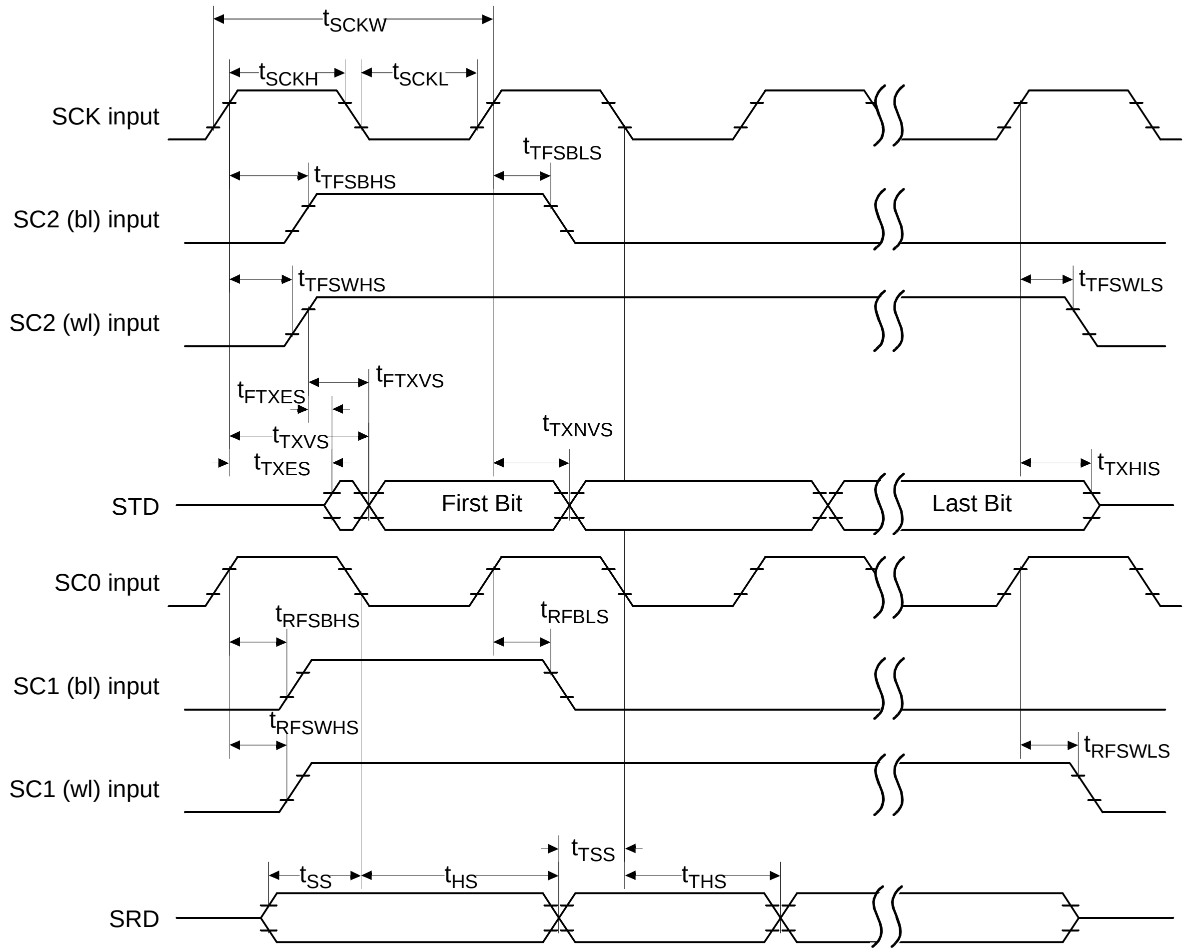


Figure 28. Slave Mode Clock Timing

4.11 Serial Communication Interface (SCI) Timing

Table 16. SCI Timing[4]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62$-1.98V, $V_{DDIO} = V_{DDA} = 3.0$–3.6V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Max	Unit
Baud Rate[1]	BR	—	$(f_{MAX})/(32)$	Mbps
RXD[2] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns
TXD[3] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns

1. f_{MAX} is the frequency of operation of the system clock in MHz.
2. The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
3. The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.
4. Parameters listed are guaranteed by design.

Figure 29. RXD Pulse Width

Figure 30. TXD Pulse Width

4.12 JTAG Timing

Table 17. JTAG Timing[1, 3]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62$-1.98V, $V_{DDIO} = V_{DDA} = 3.0$–3.6V, $T_A = –40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Max	Unit
TCK frequency of operation[2]	f_{OP}	DC	30	MHz
TCK cycle time	t_{CY}	33.3	—	ns
TCK clock pulse width	t_{PW}	16.6	—	ns
TMS, TDI data setup time	t_{DS}	3	—	ns
TMS, TDI data hold time	t_{DH}	3	—	ns
TCK low to TDO data valid	t_{DV}	—	12	ns
TCK low to TDO tri-state	t_{TS}	—	10	ns
$\overline{\text{TRST}}$ assertion time	t_{TRST}	35	—	ns
$\overline{\text{DE}}$ assertion time	t_{DE}	4T	—	ns

1. Timing is both wait state and frequency dependent. For the values listed, T = clock cycle. For 120MHz operation, T = 8.33ns.
2. TCK frequency of operation must be less than 1/4 the processor rate.
3. Parameters listed are guaranteed by design.

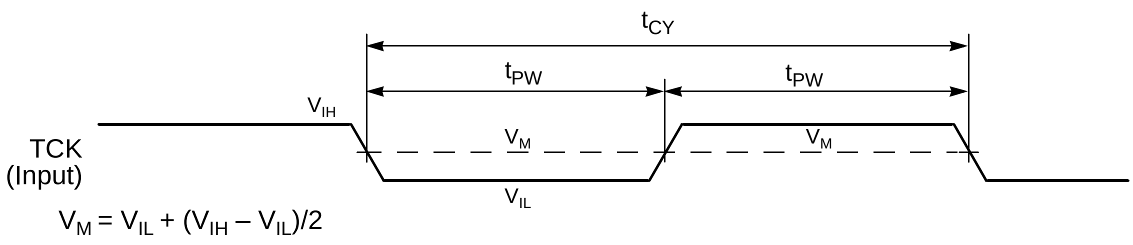


Figure 31. Test Clock Input Timing Diagram

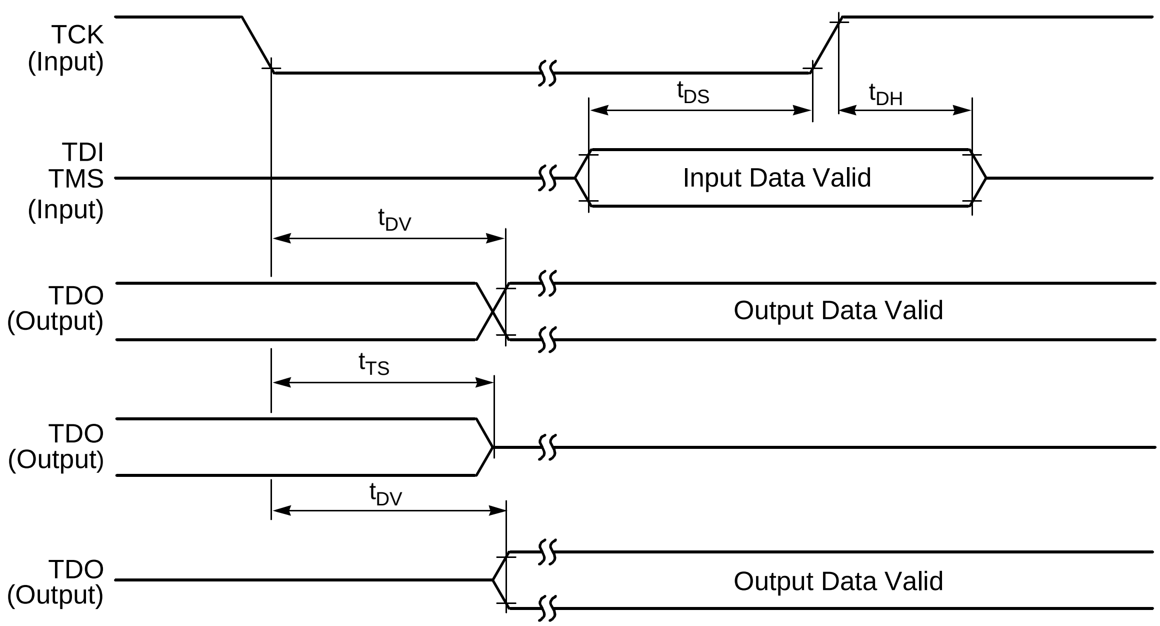


Figure 32. Test Access Port Timing Diagram

Figure 33. $\overline{\text{TRST}}$ Timing Diagram

Figure 34. Enhanced OnCE—Debug Event

4.13 GPIO Timing

Table 18. GPIO Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, V_{DD} = 1.62-1.98V, $V_{DDIO} = V_{DDA}$ = 3.0–3.6V, T_A = –40° to +120°C, $C_L \leq$ 50pF, f_{op} = 120MHz

Characteristic	Symbol	Min	Max	Unit
GPIO input period	P_{IN}	2T + 3	—	ns
GPIO input high/low period	P_{INHL}	1T + 3	—	ns
GPIO output period	P_{OUT}	2T - 3	—	ns
GPIO output high/low period	P_{OUTHL}	1T - 3	—	ns

1. In the formulas listed, T = clock cycle. For f_{op} = 120MHz operation and fipb = 60MHz, T = 8.33ns
2. Parameters listed are guaranteed by design.

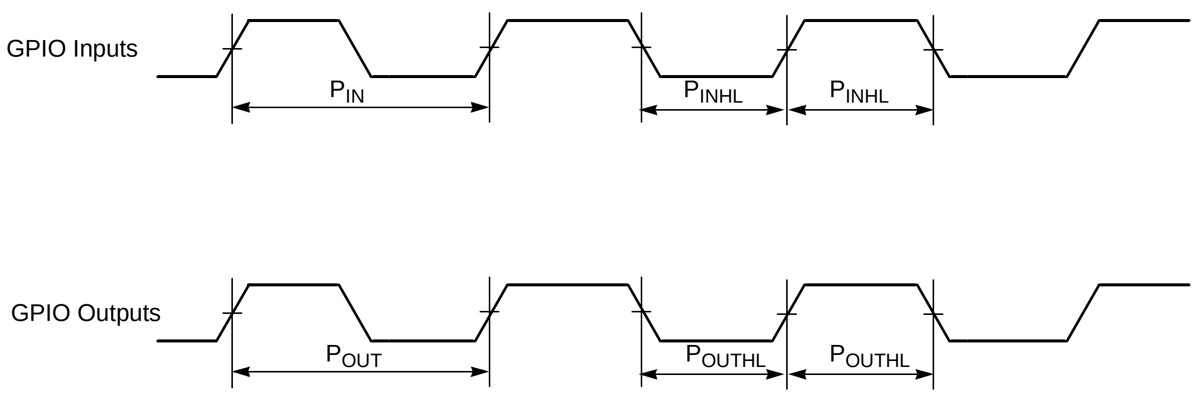


Figure 35. GPIO Timing

Part 5 Packaging

5.1 Package and Pin-Out Information DSP56857

This section contains package and pin-out information for the 100-pin LQFP configuration of the DSP56857.

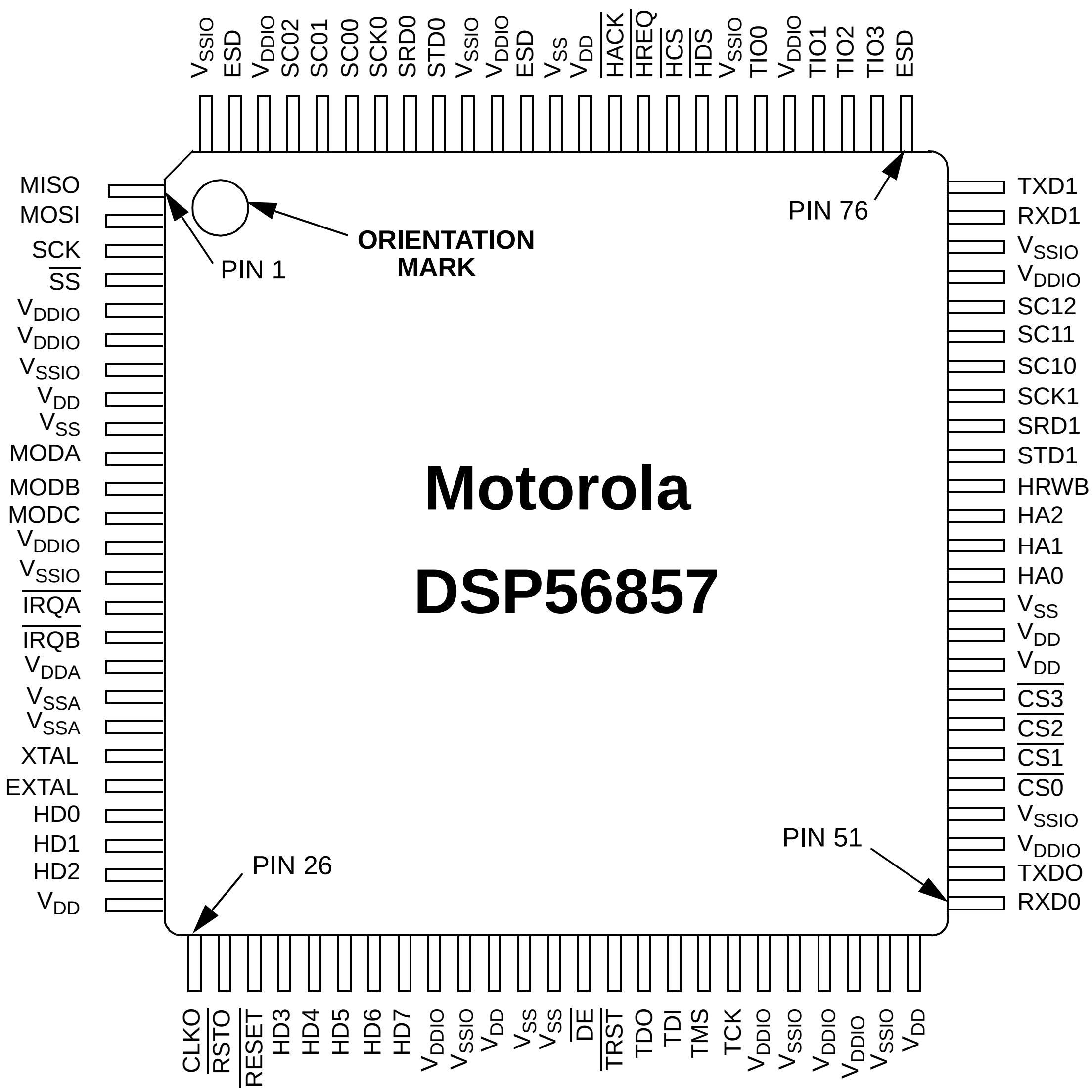
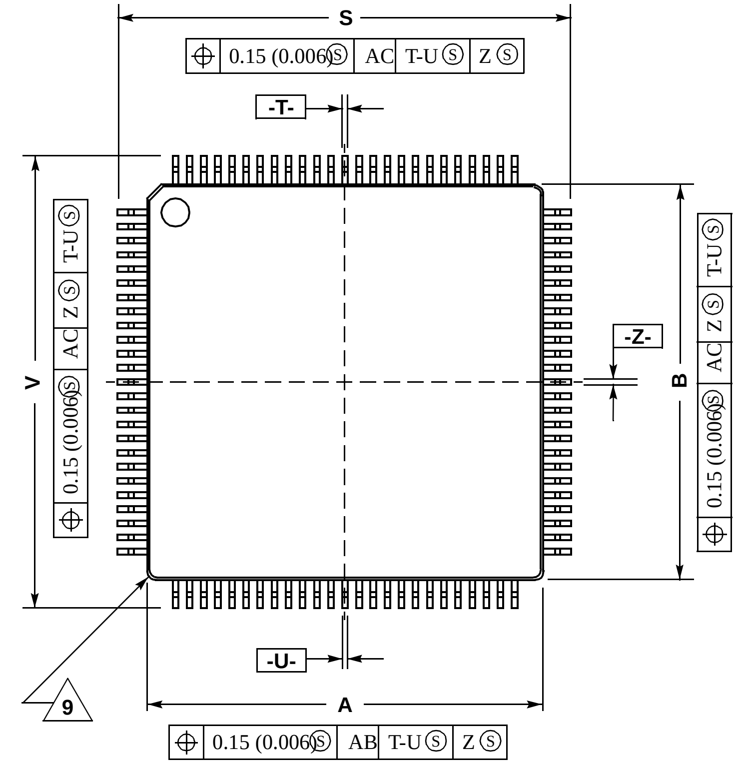


Figure 36. Top View, DSP56857 100-pin LQFP Package

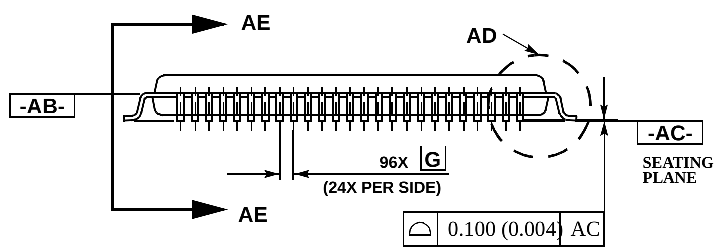
Table 19. DSP56857 Pin Identification By Pin Number

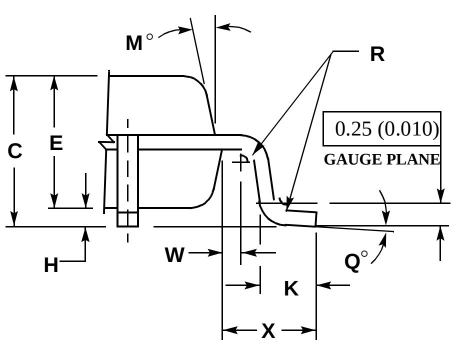
Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	MISO	26	CLKO	51	RXD0	76	V_{DD}
2	MOSI	27	$\overline{RSTO}$	52	TXD0	77	TIO3
3	SCK	28	$\overline{RESET}$	53	V_{DDIO}	78	TIO2
4	$\overline{SS}$	29	HD3	54	V_{SSIO}	79	TIO1
5	V_{DDIO}	30	HD4	55	$\overline{CS0}$	80	V_{DDIO}
6	V_{DDIO}	31	HD5	56	$\overline{CS1}$	81	TIO0
7	V_{SSIO}	32	HD6	57	$\overline{CS2}$	82	V_{SSIO}
8	V_{DD}	33	HD7	58	$\overline{CS3}$	83	$\overline{HDS}$
9	V_{SS}	34	V_{DDIO}	59	V_{DD}	84	$\overline{HCS}$
10	MODA	35	V_{SSIO}	60	V_{DD}	85	$\overline{HREQ}$
11	MODB	36	V_{DD}	61	V_{SS}	86	$\overline{HACK}$
12	MODC	37	V_{SS}	62	HA0	87	V_{DD}
13	V_{DDIO}	38	V_{SS}	63	HA1	88	V_{SS}
14	V_{SSIO}	39	$\overline{DE}$	64	HA2	89	V_{SSIO}
15	$\overline{IRQA}$	40	$\overline{TRST}$	65	HRWB	90	V_{DDIO}
16	$\overline{IRQB}$	41	TDO	66	STD1	91	V_{SSIO}
17	V_{DDA}	42	TDI	67	SRD1	92	STD0
18	V_{SSA}	43	TMS	68	SCK1	93	SRD0
19	V_{SSA}	44	TCK	69	SC10	94	SCK0
20	XTAL	45	V_{DDIO}	70	SC11	95	SC00
21	EXTAL	46	V_{SSIO}	71	SC12	96	SC01
22	HD0	47	V_{DDIO}	72	V_{DDIO}	97	SC02
23	HD1	48	V_{DDIO}	73	V_{SSIO}	98	V_{DDIO}
24	HD2	49	V_{SSIO}	74	RXD1	99	V_{SSIO}
25	V_{DD}	50	V_{DD}	75	TXD1	100	V_{SSIO}



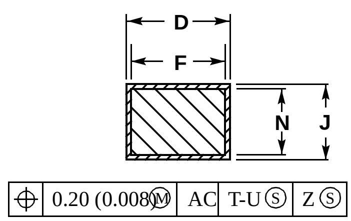
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014). DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.070 (0.003).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	13.950	14.050	0.549	0.553
B	13.950	14.050	0.549	0.553
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BSC		0.020 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	15.950	16.050	0.628	0.632
V	15.950	16.050	0.628	0.632
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	





DETAIL AD



SECTION AE-AE

CASE 842F-01

Figure 37. 100-pin LQPF Mechanical Information

Part 6 Design Considerations

6.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature °C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on the PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common definitions for determining the junction-to-case thermal resistance in plastic packages:

- Measure the thermal resistance from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink. This is done to minimize temperature variation across the surface.
- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.
- Use the value obtained by the equation $(T_J – T_T)/P_D$ where T_T is the temperature of the package case determined by a thermocouple.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual. Hence, the new thermal metric, Thermal Characterization Parameter, or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

6.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the DSP, and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place six 0.01–0.1 μF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the ten V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{DD} and GND.
- Bypass the V_{DD} and GND layers of the PCB with approximately 100 μF, preferably with a high-grade capacitor such as a tantalum capacitor.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels.
- Take special care to minimize noise levels on the V_{DDA} and V_{SSA} pins.
- When using Wired-OR mode on the SPI or the $\overline{\text{IRQx}}$ pins, the user must provide an external pull-up device.

- Designs that utilize the $\overline{TRST}$ pin for JTAG port or Enhance OnCE module functionality (such as development or debugging systems) should allow a means to assert $\overline{TRST}$ whenever $\overline{RESET}$ is asserted, as well as a means to assert $\overline{TRST}$ independently of $\overline{RESET}$. Designs that do not require debugging functionality, such as consumer products, should tie these pins together.
- The internal POR (Power on Reset) will reset the part at power on with $\overline{reset}$ asserted or pulled high but requires that $\overline{TRST}$ be asserted at power on.

Part 7 Ordering Information

Table 20 lists the pertinent information needed to place an order. Consult a Motorola Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 20. DSP56857 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56857	1.8V, 3.3V	Low-Profile Quad Flat Pack (LQFP)	100	120	DSP56857BU120

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3–20–1, Minami–Azabu. Minato–ku, Tokyo 106–8573 Japan. 81–3–3440–3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852–26668334

Technical Information Center: 1–800–521–6274

HOME PAGE: http://www.motorola.com/semiconductors/

MOTOROLA