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Addendum to the e200z6 PowerPC™ Core Reference Manual, Rev. 0

e200z6 with VLE

This addendum describes the features defined by the e200z6 with VLE that differ from those defined for the e200z6. The section number and page number of the errata item in the reference manual are provided. Items in bold are new since the last revision of this document.

To locate any published updates for this document, visit our website listed on the back cover of this document.

Section, Page No.	Changes
1.1, 1-1	Insert the following after the first paragraph: "The e200z6 with VLE core implements the variable-length encoding (VLE) APU, providing improved code density. See the *EREF* for more information about the VLE extension."
3.1, 3-1	Insert the following after the first paragraph: "The e200z6 with VLE core implements the variable-length encoding (VLE) APU, providing improved code density. See the *EREF* for more information about the VLE extension."

freescale™ semiconductor

2.10.4, 2-50 Change bit 59 from Reserved to VLES and replace Figure 2-36 and Table 2-22 with the following:

	32	33	34 35	36	37	38	39	40	41	42	43	44	45	46	47
Field	IDE	UDE	MRR	ICMP	BRT	IRPT	TRAP	IAC1	IAC2	IAC3	IAC4	DAC1R	DAC1W	DAC2R	DAC2W
Reset	0001_0000_0000_0000														
R/W	Read/Clear														

	48	49 52	53	54	55	56	57	58	59	60 62	63
Field	RET	—	DEVT1	DEVT2	DCNT1	DCNT2	CIRPT	CRET	VLES	—	CNT1TRG
Reset	0000_0000_0000_0000										
R/W	Read/Clear										
SPR	SPR 304										

Figure 2-36. DBSR Register

Table 2-22. DBSR Field Descriptions

Bits	Name	Description
32	IDE	Imprecise debug event. Set if MSR[DE] = 0 and DBCR0[EDM] = 0 and a debug event causes its respective debug status register bit to be set. IDE can also be set if DBCR0[EDM] = 1 and an imprecise debug event occurs due to a DAC event on a load or store that is terminated with error, or if an ICMP event occurs in conjunction with a SPE FP round exception.
33	UDE	Unconditional debug event. Set when an unconditional debug event occurs.
34–35	MRR	Most recent reset. 00 No reset since software last cleared these bits. 01 A hard reset occurred since software last cleared these bits. 1*x* Reserved.
36	ICMP	Instruction complete debug event. Set if an instruction complete debug event occurs.
37	BRT	Branch taken debug event. Set if an branch taken debug event occurs.
38	IRPT	Interrupt taken debug event. Set if an interrupt taken debug event occurs.
39	TRAP	Trap taken debug event. Set if a trap taken debug event occurs.
40	IAC1	Instruction address compare 1 debug event. Set if an IAC1 debug event occurs.
41	IAC2	Instruction address compare 2 debug event. Set if an IAC2 debug event occurs.
42	IAC3	Instruction address compare 3 debug event. Set if an IAC3 debug event occurs.
43	IAC4	Instruction address compare 4 debug event. Set if an IAC4 debug event occurs.
44	DAC1R	Data address compare 1 read debug event. Set if a read-type DAC1 debug event occurs while DBCR0[DAC1] = 0b10 or DBCR0[DAC1] = 0b11.
45	DAC1W	Data address compare 1 write debug event. Set if a write-type DAC1 debug event occurs while DBCR0[DAC1] = 0b01 or DBCR0[DAC1] = 0b11.
46	DAC2R	Data address compare 2 read debug event. Set if a read-type DAC2 debug event occurs while DBCR0[DAC2] = 0b10 or DBCR0[DAC2] = 0b11.

Table 2-22. DBSR Field Descriptions (continued)

Bits	Name	Description
47	DAC2W	Data address compare 2 write debug event. Set if a write-type DAC2 debug event occurs while DBCR0[DAC2] = 0b01 or DBCR0[DAC2] = 0b11.
48	RET	Return debug event. Set if a Return debug event occurs.
49–52	—	Reserved, should be cleared.
53	DEVT1	External debug event 1 debug event. Set if a DEVT1 debug event occurs.
54	DEVT2	External debug event 2 debug event. Set if a DEVT2 debug event occurs.
55	DCNT1	Debug counter 1 debug event. Set if a DCNT1 debug event occurs.
56	DCNT2	Debug counter 2 debug event. Set if a DCNT2 debug event occurs.
57	CIRPT	Critical interrupt taken debug event. Set if a critical interrupt taken debug event occurs.
58	CRET	Critical return debug event. Set if a critical return debug event occurs.
59	VLES	VLE status, Set if an ICMP, BRT, TRAP, RET, CRET, IAC, or DAC debug event occurred on a VLE instruction. Undefined for IRPT, CIRPT, DEVT[1,2], DCNT[1,2], and UDE events.
60–62	—	Reserved, should be cleared.
63	CNT1TRG	Counter 1 triggered. Set if debug counter 1 is triggered by a trigger event.

2.14.4, 2-66 Change bit 58 from Reserved to VLE and replace Figure 2-49 and Table 2-35 with the following:

	32 — 51	52 — 57	58	59	60	61	62	63
Field	EPN	—	VLE	W	I	M	G	E
Reset	Undefined on *m_por* assertion, unchanged on *p_reset_b* assertion							
R/W	R/W							
SPR	SPR 626							

Figure 2-49. MMU Assist Register 2 (MAS2)

Table 2-35. MAS2—EPN and Page Attributes

Bits	Name	Description
32–51	EPN	Effective page number.
52–57	—	Reserved, should be cleared.
58	VLE	VLE mode. Identifies pages that contain instructions from the VLE APU. VLE is implemented only if the processor supports the VLE APU. Setting both the VLE and E fields is a programming error; an attempt to fetch instructions from a page so marked produces an ISI byte ordering exception and sets ESR[BO]. 0 Instructions fetched from the page are decoded and executed as PowerPC or EIS instructions. 1 Instructions fetched from the page are decoded and executed as VLE or EIS instructions. Implementation-dependent page attribute.

Table 2-35. MAS2—EPN and Page Attributes (continued)

Bits	Name	Description
59	W	Write-through required. 0 This page is a write-back with respect to the caches in the system. 1 All stores performed to this page are written through to main memory.
60	I	Cache inhibited. 0 This page is cacheable. 1 This page is cache-inhibited.
61	M	Memory coherence required.The e200z6 does *not* support the memory coherence required attribute, and thus it is ignored. 0 Memory coherence is not required. 1 Memory coherence is required.
62	G	Guarded. The e200z6 ignores the guarded attribute (other than for generation of the *p_hprot[4:2]* attributes on an external access), since no speculative or out-of-order processing is performed. Refer to Section 4.16, “Page Table Control Bits,” for more information. 0 Access to this page are not guarded, and can be performed before it is known if they are required by the sequential execution model. 1 All loads and stores to this page are performed without speculation (that is, they are known to be required).
63	E	Endianness. Determines endianness for the corresponding page. Refer to Section 3.2.4, “Byte Lane Specification,” for more information. 0 The page is accessed in big-endian byte order. 1 The page is accessed in true little-endian byte order.

2.14.4, 2-64 Change bit 58 from Reserved to VLE and replace Figure 2-51 and Table 2-37 with the following:

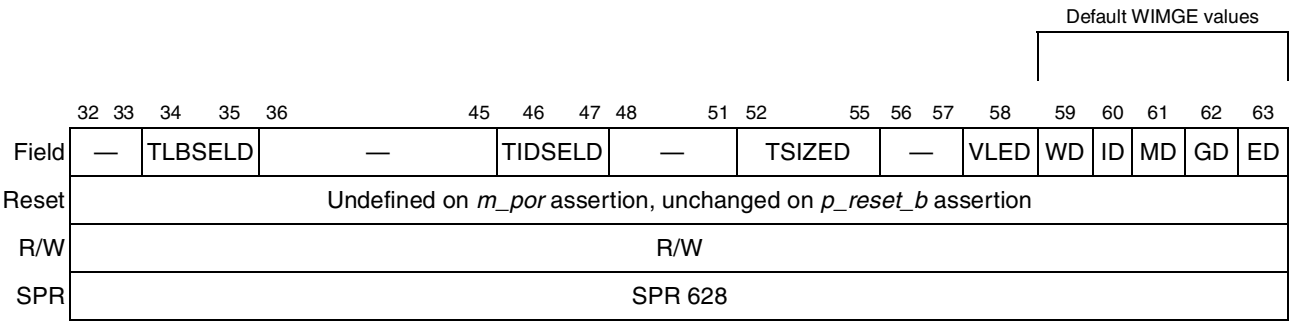

Figure 2-51. MMU Assist Register 4 (MAS4)

Table 2-37. MAS4—Hardware Replacement Assist Configuration Register

Bits	Name	Description
32–33	—	Reserved, should be cleared.
34–35	TLBSELD	Default TLB selected. 01 TLB1 (ignored by the e200z6, should be written to 01 for future compatibility)
36–45	—	Reserved, should be cleared.

Table 2-37. MAS4—Hardware Replacement Assist Configuration Register (continued)

Bits	Name	Description
46–47	TIDSELD	Default PID# to load TID from 00 PID0 01 Reserved, do not use 10 Reserved, do not use 11 TIDZ (8'h00)) (Use all zeros, the globally shared value)
48–51	—	Reserved, should be cleared.
52–55	TSIZED	Default TSIZE value.
56–57	—	Reserved, should be cleared.
58	VLED	Default VLE value. Specifies the default value loaded into MAS2[VLE] on a TLB miss exception.
59–63	DWIMGE	Default WIMGE values.

3.9.2, 3-33

Add the following at the end of Section 3.9.2:[1]

Table 3-11 lists all supported instructions, including VLE instructions. Note that only the e200z6 with VLE supports the instructions defined by the VLE, which are designated with the prefixes, **e_** and **se_**.

Table 3-11. Full Instruction Listing

Mnemonic	Instruction Name	Source
add	Add	Book E
add.	Add & record CR	Book E
addc	Add Carrying	Book E
addc.	Add Carrying & record CR	Book E
addco	Add Carrying & record OV	Book E
addco.	Add Carrying & record OV & CR	Book E
adde	Add Extended with CA	Book E
adde.	Add Extended with CA & record CR	Book E
addeo	Add Extended with CA & record OV	Book E
addeo.	Add Extended with CA & record OV & CR	Book E
addi	Add Immediate	Book E
addic	Add Immediate Carrying	Book E
addic.	Add Immediate Carrying & record CR	Book E
addis	Add Immediate Shifted	Book E
addme	Add to Minus One Extended with CA	Book E
addme.	Add to Minus One Extended with CA & record CR	Book E
addmeo	Add to Minus One Extended with CA & record OV	Book E

1. Note that this change appeared in Revision 0 of the addendum but the source for instructions designated with the prefixes **e_** and **se_** in Table 3-11 has been updated since then.

Table 3-11. Full Instruction Listing (continued)

Mnemonic	Instruction Name	Source
addmeo.	Add to Minus One Extended with CA & record OV & CR	Book E
addo	Add & record OV	Book E
addo.	Add & record OV & CR	Book E
addze	Add to Zero Extended with CA	Book E
addze.	Add to Zero Extended with CA & record CR	Book E
addzeo	Add to Zero Extended with CA & record OV	Book E
addzeo.	Add to Zero Extended with CA & record OV & CR	Book E
and	AND	Book E
and.	AND & record CR	Book E
andc	AND with Complement	Book E
andc.	AND with Complement & record CR	Book E
andi.	AND Immediate and record CR	Book E
andis.	AND Immediate Shifted and record CR	Book E
b	Branch	Book E
ba	Branch Absolute	Book E
bc	Branch Conditional	Book E
bca	Branch Conditional Absolute	Book E
bcctr	Branch Conditional to Count Register	Book E
bcctrl	Branch Conditional to Count Register and Link	Book E
bcl	Branch Conditional and Link	Book E
bcla	Branch Conditional and Link Absolute	Book E
bclr	Branch Conditional to Link Register	Book E
bclrl	Branch Conditional to Link Register and Link	Book E
bl	Branch and Link	Book E
bla	Branch and Link Absolute	Book E
brinc	Bit Reversed Increment[1]	SPE
cmp	Compare	Book E
cmpi	Compare Immediate	Book E
cmpl	Compare Logical	Book E
cmpli	Compare Logical Immediate	Book E
cntlzw	Count Leading Zeros Word	Book E
cntlzw.	Count Leading Zeros Word and record CR	Book E
crand	Condition Register AND	Book E
crandc	Condition Register AND with Complement	Book E
creqv	Condition Register Equivalent	Book E

Table 3-11. Full Instruction Listing (continued)

Mnemonic	Instruction Name	Source
crnand	Condition Register NAND	Book E
crnor	Condition Register NOR	Book E
cror	Condition Register OR	Book E
crorc	Condition Register OR with Complement	Book E
crxor	Condition Register XOR	Book E
dcba	Data Cache Block Allocate	Book E
dcbf	Data Cache Block Flush	Book E
dcbi	Data Cache Block Invalidate	Book E
dcblc	Data Cache Block Lock Clear	Cache locking
dcbst	Data Cache Block Store	Book E
dcbt	Data Cache Block Touch	Book E
dcbtls	Data Cache Block Touch and Lock Set	Cache locking
dcbtst	Data Cache Block Touch for Store	Book E
dcbtstls	Data Cache Block Touch for Store and Lock Set	Cache locking
dcbz	Data Cache Block set to Zero	Book E
divw	Divide Word	Book E
divw.	Divide Word and record CR	Book E
divwo	Divide Word and record OV	Book E
divwo.	Divide Word and record OV and CR	Book E
divwu	Divide Word Unsigned	Book E
divwu.	Divide Word Unsigned and record CR	Book E
divwuo	Divide Word Unsigned and record OV	Book E
divwuo.	Divide Word Unsigned and record OV and CR	Book E
efsabs	Floating-Point Absolute Value	Scalar SPFP
efsadd	Floating-Point Add	Scalar SPFP
efscfsf	Convert Floating-Point from Signed Fraction	Scalar SPFP
efscfsi	Convert Floating-Point from Signed Integer	Scalar SPFP
efscfuf	Convert Floating-Point from Unsigned Fraction	Scalar SPFP
efscfui	Convert Floating-Point from Unsigned Integer	Scalar SPFP
efscmpeq	Floating-Point Compare Equal	Scalar SPFP
efscmpgt	Floating-Point Compare Greater Than	Scalar SPFP
efscmplt	Floating-Point Compare Less Than	Scalar SPFP
efsctsf	Convert Floating-Point to Signed Fraction	Scalar SPFP
efsctsi	Convert Floating-Point to Signed Integer	Scalar SPFP
efsctsiz	Convert Floating-Point to Signed Integer with Round toward Zero	Scalar SPFP

Table 3-11. Full Instruction Listing (continued)

Mnemonic	Instruction Name	Source
efsctuf	Convert Floating-Point to Unsigned Fraction	Scalar SPFP
efsctui	Convert Floating-Point to Unsigned Integer	Scalar SPFP
efsctuiz	Convert Floating-Point to Unsigned Integer with Round toward Zero	Scalar SPFP
efsdiv	Floating-Point Divide	Scalar SPFP
efsmul	Floating-Point Multiply	Scalar SPFP
efsnabs	Floating-Point Negative Absolute Value	Scalar SPFP
efsneg	Floating-Point Negate	Scalar SPFP
efssub	Floating-Point Subtract	Scalar SPFP
efststeq	Floating-Point Test Equal	Scalar SPFP
efststgt	Floating-Point Test Greater Than	Scalar SPFP
efststlt	Floating-Point Test Less Than	Scalar SPFP
eqv	Equivalent	Book E
eqv.	Equivalent and record CR	Book E
evabs	Vector Absolute Value	SPE
evaddiw	Vector Add Immediate Word	SPE
evaddsmiaaw	Vector Add Signed, Modulo, Integer to Accumulator Word	SPE
evaddssiaaw	Vector Add Signed, Saturate, Integer to Accumulator Word	SPE
evaddumiaaw	Vector Add Unsigned, Modulo, Integer to Accumulator Word	SPE
evaddusiaaw	Vector Add Unsigned, Saturate, Integer to Accumulator Word	SPE
evaddw	Vector Add Word	SPE
evand	Vector AND	SPE
evandc	Vector AND with Complement	SPE
evcmpeq	Vector Compare Equal	SPE
evcmpgts	Vector Compare Greater Than Signed	SPE
evcmpgtu	Vector Compare Greater Than Unsigned	SPE
evcmplts	Vector Compare Less Than Signed	SPE
evcmpltu	Vector Compare Less Than Unsigned	SPE
evcntlsw	Vector Count Leading Sign Bits Word	SPE
evcntlzw	Vector Count Leading Zeros Word	SPE
evdivws	Vector Divide Word Signed	SPE
evdivwu	Vector Divide Word Unsigned	SPE
eveqv	Vector Equivalent	SPE
evextsb	Vector Extend Sign Byte	SPE
evextsh	Vector Extend Sign Half Word	SPE
evfsabs	Vector Floating-Point Absolute Value	SPE

Table 3-11. Full Instruction Listing (continued)

Mnemonic	Instruction Name	Source
evfsabs	Floating-Point Absolute Value	Vector SPFP
evfsadd	Vector Floating-Point Add	SPE
evfsadd	Floating-Point Add	Vector SPFP
evfscfsf	Vector Convert Floating-Point from Signed Fraction	SPE
evfscfsf	Convert Floating-Point from Signed Fraction	Vector SPFP
evfscfsi	Vector Convert Floating-Point from Signed Integer	SPE
evfscfsi	Convert Floating-Point from Signed Integer	Vector SPFP
evfscfuf	Vector Convert Floating-Point from Unsigned Fraction	SPE
evfscfuf	Convert Floating-Point from Unsigned Fraction	Vector SPFP
evfscfui	Vector Convert Floating-Point from Unsigned Integer	SPE
evfscfui	Convert Floating-Point from Unsigned Integer	Vector SPFP
evfscmpeq	Vector Floating-Point Compare Equal	SPE
evfscmpeq	Floating-Point Compare Equal	Vector SPFP
evfscmpgt	Vector Floating-Point Compare Greater Than	SPE
evfscmpgt	Floating-Point Compare Greater Than	Vector SPFP
evfscmplt	Vector Floating-Point Compare Less Than	SPE
evfscmplt	Floating-Point Compare Less Than	Vector SPFP
evfsctsf	Vector Convert Floating-Point to Signed Fraction	SPE
evfsctsf	Convert Floating-Point to Signed Fraction	Vector SPFP
evfsctsi	Vector Convert Floating-Point to Signed Integer	SPE
evfsctsi	Convert Floating-Point to Signed Integer	Vector SPFP
evfsctsiz	Vector Convert Floating-Point to Signed Integer with Round toward Zero	SPE
evfsctsiz	Convert Floating-Point to Signed Integer with Round toward Zero	Vector SPFP
evfsctuf	Vector Convert Floating-Point to Unsigned Fraction	SPE
evfsctuf	Convert Floating-Point to Unsigned Fraction	Vector SPFP
evfsctui	Vector Convert Floating-Point to Unsigned Integer	SPE
evfsctui	Convert Floating-Point to Unsigned Integer	Vector SPFP
evfsctuiz	Vector Convert Floating-Point to Unsigned Integer with Round toward Zero	SPE
evfsctuiz	Convert Floating-Point to Unsigned Integer with Round toward Zero	Vector SPFP
evfsdiv	Vector Floating-Point Divide	SPE
evfsdiv	Floating-Point Divide	Vector SPFP
evfsmul	Vector Floating-Point Multiply	SPE
evfsmul	Floating-Point Multiply	Vector SPFP
evfsnabs	Vector Floating-Point Negative Absolute Value	SPE
evfsnabs	Floating-Point Negative Absolute Value	Vector SPFP

Table 3-11. Full Instruction Listing (continued)

Mnemonic	Instruction Name	Source
evfsneg	Vector Floating-Point Negate	SPE
evfsneg	Floating-Point Negate	Vector SPFP
evfssub	Vector Floating-Point Subtract	SPE
evfssub	Floating-Point Subtract	Vector SPFP
evfststeq	Vector Floating-Point Test Equal	SPE
evfststeq	Floating-Point Test Equal	Vector SPFP
evfststgt	Vector Floating-Point Test Greater Than	SPE
evfststgt	Floating-Point Test Greater Than	Vector SPFP
evfststlt	Vector Floating-Point Test Less Than	SPE
evfststlt	Floating-Point Test Less Than	Vector SPFP
evldd	Vector Load Double Word into Double Word	SPE
evlddx	Vector Load Double Word into Double Word Indexed	SPE
evldh	Vector Load Double into Half Words	SPE
evldhx	Vector Load Double into Half Words Indexed	SPE
evldw	Vector Load Double into Two Words	SPE
evldwx	Vector Load Double into Two Words Indexed	SPE
evlhhesplat	Vector Load Half Word into Half Words Even and Splat	SPE
evlhhesplatx	Vector Load Half Word into Half Words Even and Splat Indexed	SPE
evlhhossplat	Vector Load Half Word into Half Word Odd Signed and Splat	SPE
evlhhossplatx	Vector Load Half Word into Half Word Odd Signed and Splat Indexed	SPE
evlhhousplat	Vector Load Half Word into Half Word Odd Unsigned and Splat	SPE
evlhhousplatx	Vector Load Half Word into Half Word Odd Unsigned and Splat Indexed	SPE
evlwhe	Vector Load Word into Two Half Words Even	SPE
evlwhex	Vector Load Word into Two Half Words Even Indexed	SPE
evlwhos	Vector Load Word into Half Words Odd Signed (with sign extension)	SPE
evlwhosx	Vector Load Word into Half Words Odd Signed Indexed (with sign extension)	SPE
evlwhou	Vector Load Word into Two Half Words Odd Unsigned (zero-extended)	SPE
evlwhoux	Vector Load Word into Two Half Words Odd Unsigned Indexed (zero-extended)	SPE
evlwhsplat	Vector Load Word into Half Words and Splat	SPE
evlwhsplatx	Vector Load Word into Half Words and Splat Indexed	SPE
evlwwsplat	Vector Load Word into Word and Splat	SPE
evlwwsplatx	Vector Load Word into Word and Splat Indexed	SPE
evmergehi	Vector Merge High	SPE
evmergehilo	Vector Merge High/Low	SPE
evmergelo	Vector Merge Low	SPE

Table 3-11. Full Instruction Listing (continued)

Mnemonic	Instruction Name	Source
evmergelohi	Vector Merge Low/High	SPE
evmhegsmfaa	Multiply Half Words, Even, Guarded, Signed, Modulo, Fractional and Accumulate	SPE
evmhegsmfan	Multiply Half Words, Even, Guarded, Signed, Modulo, Fractional and Accumulate Negative	SPE
evmhegsmiaa	Multiply Half Words, Even, Guarded, Signed, Modulo, Integer and Accumulate	SPE
evmhegsmian	Multiply Half Words, Even, Guarded, Signed, Modulo, Integer and Accumulate Negative	SPE
evmhegumiaa	Multiply Half Words, Even, Guarded, Unsigned, Modulo, Integer and Accumulate	SPE
evmhegumian	Multiply Half Words, Even, Guarded, Unsigned, Modulo, Integer and Accumulate Negative	SPE
evmhesmf	Vector Multiply Half Words, Even, Signed, Modulo, Fractional	SPE
evmhesmfa	Vector Multiply Half Words, Even, Signed, Modulo, Fractional, Accumulate	SPE
evmhesmfaaw	Vector Multiply Half Words, Even, Signed, Modulo, Fractional and Accumulate into Words	SPE
evmhesmfanw	Vector Multiply Half Words, Even, Signed, Modulo, Fractional and Accumulate Negative into Words	SPE
evmhesmi	Vector Multiply Half Words, Even, Signed, Modulo, Integer	SPE
evmhesmia	Vector Multiply Half Words, Even, Signed, Modulo, Integer, Accumulate	SPE
evmhesmiaaw	Vector Multiply Half Words, Even, Signed, Modulo, Integer and Accumulate into Words	SPE
evmhesmianw	Vector Multiply Half Words, Even, Signed, Modulo, Integer and Accumulate Negative into Words	SPE
evmhessf	Vector Multiply Half Words, Even, Signed, Saturate, Fractional	SPE
evmhessfa	Vector Multiply Half Words, Even, Signed, Saturate, Fractional, Accumulate	SPE
evmhessfaaw	Vector Multiply Half Words, Even, Signed, Saturate, Fractional and Accumulate into Words	SPE
evmhessfanw	Vector Multiply Half Words, Even, Signed, Saturate, Fractional and Accumulate Negative into Words	SPE
evmhessiaaw	Vector Multiply Half Words, Even, Signed, Saturate, Integer and Accumulate into Words	SPE
evmhessianw	Vector Multiply Half Words, Even, Signed, Saturate, Integer and Accumulate Negative into Words	SPE
evmheumi	Vector Multiply Half Words, Even, Unsigned, Modulo, Integer	SPE
evmheumia	Vector Multiply Half Words, Even, Unsigned, Modulo, Integer, Accumulate	SPE
evmheumiaaw	Vector Multiply Half Words, Even, Unsigned, Modulo, Integer and Accumulate into Words	SPE
evmheumianw	Vector Multiply Half Words, Even, Unsigned, Modulo, Integer and Accumulate Negative into Words	SPE
evmheusiaaw	Vector Multiply Half Words, Even, Unsigned, Saturate, Integer and Accumulate into Words	SPE

Table 3-11. Full Instruction Listing (continued)

Mnemonic	Instruction Name	Source
evmheusianw	Vector Multiply Half Words, Even, Unsigned, Saturate, Integer and Accumulate Negative into Words	SPE
evmhogsmfaa	Multiply Half Words, Odd, Guarded, Signed, Modulo, Fractional and Accumulate	SPE
evmhogsmfan	Multiply Half Words, Odd, Guarded, Signed, Modulo, Fractional and Accumulate Negative	SPE
evmhogsmiaa	Multiply Half Words, Odd, Guarded, Signed, Modulo, Integer and Accumulate	SPE
evmhogsmian	Multiply Half Words, Odd, Guarded, Signed, Modulo, Integer and Accumulate Negative	SPE
evmhogumiaa	Multiply Half Words, Odd, Guarded, Unsigned, Modulo, Integer and Accumulate	SPE
evmhogumian	Multiply Half Words, Odd, Guarded, Unsigned, Modulo, Integer and Accumulate Negative	SPE
evmhosmf	Vector Multiply Half Words, Odd, Signed, Modulo, Fractional	SPE
evmhosmfa	Vector Multiply Half Words, Odd, Signed, Modulo, Fractional, Accumulate	SPE
evmhosmfaaw	Vector Multiply Half Words, Odd, Signed, Modulo, Fractional and Accumulate into Words	SPE
evmhosmfanw	Vector Multiply Half Words, Odd, Signed, Modulo, Fractional and Accumulate Negative into Words	SPE
evmhosmi	Vector Multiply Half Words, Odd, Signed, Modulo, Integer	SPE
evmhosmia	Vector Multiply Half Words, Odd, Signed, Modulo, Integer, Accumulate	SPE
evmhosmiaaw	Vector Multiply Half Words, Odd, Signed, Modulo, Integer and Accumulate into Words	SPE
evmhosmianw	Vector Multiply Half Words, Odd, Signed, Modulo, Integer and Accumulate Negative into Words	SPE
evmhossf	Vector Multiply Half Words, Odd, Signed, Saturate, Fractional	SPE
evmhossfa	Vector Multiply Half Words, Odd, Signed, Saturate, Fractional, Accumulate	SPE
evmhossfaaw	Vector Multiply Half Words, Odd, Signed, Saturate, Fractional and Accumulate into Words	SPE
evmhossfanw	Vector Multiply Half Words, Odd, Signed, Saturate, Fractional and Accumulate Negative into Words	SPE
evmhossiaaw	Vector Multiply Half Words, Odd, Signed, Saturate, Integer and Accumulate into Words	SPE
evmhossianw	Vector Multiply Half Words, Odd, Signed, Saturate, Integer and Accumulate Negative into Words	SPE
evmhoumi	Vector Multiply Half Words, Odd, Unsigned, Modulo, Integer	SPE
evmhoumia	Vector Multiply Half Words, Odd, Unsigned, Modulo, Integer, Accumulate	SPE
evmhoumiaaw	Vector Multiply Half Words, Odd, Unsigned, Modulo, Integer and Accumulate into Words	SPE
evmhoumianw	Vector Multiply Half Words, Odd, Unsigned, Modulo, Integer and Accumulate Negative into Words	SPE
evmhousiaaw	Vector Multiply Half Words, Odd, Unsigned, Saturate, Integer and Accumulate into Words	SPE

Table 3-11. Full Instruction Listing (continued)

Mnemonic	Instruction Name	Source
evmhousianw	Vector Multiply Half Words, Odd, Unsigned, Saturate, Integer and Accumulate Negative into Words	SPE
evmra	Initialize Accumulator	SPE
evmwhsmf	Vector Multiply Word High Signed, Modulo, Fractional	SPE
evmwhsmfa	Vector Multiply Word High Signed, Modulo, Fractional and Accumulate	SPE
evmwhsmi	Vector Multiply Word High Signed, Modulo, Integer	SPE
evmwhsmia	Vector Multiply Word High Signed, Modulo, Integer and Accumulate	SPE
evmwhssf	Vector Multiply Word High Signed, Saturate, Fractional	SPE
evmwhssfa	Vector Multiply Word High Signed, Saturate, Fractional and Accumulate	SPE
evmwhumi	Vector Multiply Word High Unsigned, Modulo, Integer	SPE
evmwhumia	Vector Multiply Word High Unsigned, Modulo, Integer and Accumulate	SPE
evmwlsmi	Vector Multiply Word Low Unsigned, Modulo, Integer	SPE
evmwlsmiaaw	Vector Multiply Word Low Signed, Modulo, Integer and Accumulate in Words	SPE
evmwlsmianw	Vector Multiply Word Low Signed, Modulo, Integer and Accumulate Negative in Words	SPE
evmwlssiaaw	Vector Multiply Word Low Signed, Saturate, Integer and Accumulate in Words	SPE
evmwlssianw	Vector Multiply Word Low Signed, Saturate, Integer and Accumulate Negative in Words	SPE
evmwlumia	Vector Multiply Word Low Unsigned, Modulo, Integer and Accumulate	SPE
evmwlumiaaw	Vector Multiply Word Low Unsigned, Modulo, Integer and Accumulate in Words	SPE
evmwlumianw	Vector Multiply Word Low Unsigned, Modulo, Integer and Accumulate Negative in Words	SPE
evmwlusiaaw	Vector Multiply Word Low Unsigned, Saturate, Integer and Accumulate in Words	SPE
evmwlusianw	Vector Multiply Word Low Unsigned, Saturate, Integer and Accumulate Negative in Words	SPE
evmwsmf	Vector Multiply Word Signed, Modulo, Fractional	SPE
evmwsmfa	Vector Multiply Word Signed, Modulo, Fractional and Accumulate	SPE
evmwsmfaa	Vector Multiply Word Signed, Modulo, Fractional and Accumulate	SPE
evmwsmfan	Vector Multiply Word Signed, Modulo, Fractional and Accumulate Negative	SPE
evmwsmi	Vector Multiply Word Signed, Modulo, Integer	SPE
evmwsmia	Vector Multiply Word Signed, Modulo, Integer and Accumulate	SPE
evmwsmiaa	Vector Multiply Word Signed, Modulo, Integer and Accumulate	SPE
evmwsmian	Vector Multiply Word Signed, Modulo, Integer and Accumulate Negative	SPE
evmwssf	Vector Multiply Word Signed, Saturate, Fractional	SPE
evmwssfa	Vector Multiply Word Signed, Saturate, Fractional and Accumulate	SPE
evmwssfaa	Vector Multiply Word Signed, Saturate, Fractional and Accumulate	SPE
evmwssfan	Vector Multiply Word Signed, Saturate, Fractional and Accumulate Negative	SPE

Table 3-11. Full Instruction Listing (continued)

Mnemonic	Instruction Name	Source
evmwumi	Vector Multiply Word Unsigned, Modulo, Integer	SPE
evmwumia	Vector Multiply Word Unsigned, Modulo, Integer and Accumulate	SPE
evmwumiaa	Vector Multiply Word Unsigned, Modulo, Integer and Accumulate	SPE
evmwumian	Vector Multiply Word Unsigned, Modulo, Integer and Accumulate Negative	SPE
evnand	Vector NAND	SPE
evneg	Vector Negate	SPE
evnor	Vector NOR	SPE
evor	Vector OR	SPE
evorc	Vector OR with Complement	SPE
evrlw	Vector Rotate Left Word	SPE
evrlwi	Vector Rotate Left Word Immediate	SPE
evrndw	Vector Round Word	SPE
evsel	Vector Select	SPE
evslw	Vector Shift Left Word	SPE
evslwi	Vector Shift Left Word Immediate	SPE
evsplatfi	Vector Splat Fractional Immediate	SPE
evsplati	Vector Splat Immediate	SPE
evsrwis	Vector Shift Right Word Immediate Signed	SPE
evsrwiu	Vector Shift Right Word Immediate Unsigned	SPE
evsrws	Vector Shift Right Word Signed	SPE
evsrwu	Vector Shift Right Word Unsigned	SPE
evstdd	Vector Store Double of Double	SPE
evstddx	Vector Store Double of Double Indexed	SPE
evstdh	Vector Store Double of Four Half Words	SPE
evstdhx	Vector Store Double of Four Half Words Indexed	SPE
evstdw	Vector Store Double of Two Words	SPE
evstdwx	Vector Store Double of Two Words Indexed	SPE
evstwhe	Vector Store Word of Two Half Words from Even	SPE
evstwhex	Vector Store Word of Two Half Words from Even Indexed	SPE
evstwho	Vector Store Word of Two Half Words from Odd	SPE
evstwhox	Vector Store Word of Two Half Words from Odd Indexed	SPE
evstwwe	Vector Store Word of Word from Even	SPE
evstwwex	Vector Store Word of Word from Even Indexed	SPE
evstwwo	Vector Store Word of Word from Odd	SPE
evstwwox	Vector Store Word of Word from Odd Indexed	SPE

Table 3-11. Full Instruction Listing (continued)

Mnemonic	Instruction Name	Source
evsubfsmiaaw	Vector Subtract Signed, Modulo, Integer to Accumulator Word	SPE
evsubfssiaaw	Vector Subtract Signed, Saturate, Integer to Accumulator Word	SPE
evsubfumiaaw	Vector Subtract Unsigned, Modulo, Integer to Accumulator Word	SPE
evsubfusiaaw	Vector Subtract Unsigned, Saturate, Integer to Accumulator Word	SPE
evsubfw	Vector Subtract from Word	SPE
evsubifw	Vector Subtract Immediate from Word	SPE
evxor	Vector XOR	SPE
extsb	Extend Sign Byte	Book E
extsb.	Extend Sign Byte and record CR	Book E
extsh	Extend Sign Half Word	Book E
extsh.	Extend Sign Half Word and record CR	Book E
e_add16i	Add Immediate	VLE (32-bit opcodes)
e_add2i.	Add (2 operand) Immediate and Record CR	VLE (32-bit opcodes)
e_add2is	Add (2 operand) Immediate Shifted	VLE (32-bit opcodes)
e_addi	Add Immediate	VLE (32-bit opcodes)
e_addi.	Add Immediate and Record	VLE (32-bit opcodes)
e_addic	Add Immediate Carrying	VLE (32-bit opcodes)
e_addic.	Add Immediate Carrying and Record	VLE (32-bit opcodes)
e_and2i.	AND (2 operand) Immediate & record CR	VLE (32-bit opcodes)
e_and2is.	AND (2 operand) Immediate Shifted & record CR	VLE (32-bit opcodes)
e_andi	AND Immediate	VLE (32-bit opcodes)
e_andi.	AND Immediate and Record	VLE (32-bit opcodes)
e_b	Branch	VLE (32-bit opcodes)
e_bc	Branch Conditional	VLE (32-bit opcodes)
e_bcl	Branch Conditional & Link	VLE (32-bit opcodes)
e_bl	Branch & Link	VLE (32-bit opcodes)
e_cmp16i	Compare Immediate	VLE (32-bit opcodes)
e_cmph	Compare Halfword	VLE (32-bit opcodes)
e_cmph16i	Compare Halfword Immediate	VLE (32-bit opcodes)
e_cmphl	Compare Halfword Logical	VLE (32-bit opcodes)
e_cmphl16i	Compare Halfword Logical Immediate	VLE (32-bit opcodes)
e_cmpi	Compare Immediate	VLE (32-bit opcodes)
e_cmpl16i	Compare Logical Immediate	VLE (32-bit opcodes)
e_cmpli	Compare Logical Immediate	VLE (32-bit opcodes)
e_crand	Condition Register AND	VLE (32-bit opcodes)

Table 3-11. Full Instruction Listing (continued)

Mnemonic	Instruction Name	Source
e_crandc	Condition Register AND with Complement	VLE (32-bit opcodes)
e_creqv	Condition Register Equivalent	VLE (32-bit opcodes)
e_crnand	Condition Register NAND	VLE (32-bit opcodes)
e_crnor	Condition Register NOR	VLE (32-bit opcodes)
e_cror	Condition Register OR	VLE (32-bit opcodes)
e_crorc	Condition Register OR with Complement	VLE (32-bit opcodes)
e_crxor	Condition Register XOR	VLE (32-bit opcodes)
e_lbz	Load Byte & Zero	VLE (32-bit opcodes)
e_lbzu	Load Byte & Zero with Update	VLE (32-bit opcodes)
e_lha	Load Halfword Algebraic	VLE (32-bit opcodes)
e_lhau	Load Halfword Algebraic With Update	VLE (32-bit opcodes)
e_lhz	Load Halfword & Zero	VLE (32-bit opcodes)
e_lhzu	Load Halfword & Zero with Update	VLE (32-bit opcodes)
e_li	Load Immediate	VLE (32-bit opcodes)
e_lis	Load Immediate Shifted	VLE (32-bit opcodes)
e_lmw	Load Multiple Word	VLE (32-bit opcodes)
e_lwz	Load Word & Zero	VLE (32-bit opcodes)
e_lwzu	Load Word & Zero with Update	VLE (32-bit opcodes)
e_mcrf	Move Condition Register Field	VLE (32-bit opcodes)
e_mull2i	Multiply Low Word (2 operand) Immediate	VLE (32-bit opcodes)
e_mulli	Multiply Low Immediate	VLE (32-bit opcodes)
e_or2i	OR (2 operand) Immediate	VLE (32-bit opcodes)
e_or2is	OR (2 operand) Immediate Shifted	VLE (32-bit opcodes)
e_ori	OR Immediate	VLE (32-bit opcodes)
e_ori.	OR Immediate and Record	VLE (32-bit opcodes)
e_rlw	Rotate Left Word	VLE (32-bit opcodes)
e_rlw.	Rotate Left Word & record CR	VLE (32-bit opcodes)
e_rlwi	Rotate Left Word Immediate	VLE (32-bit opcodes)
e_rlwi.	Rotate Left Word Immediate & record CR	VLE (32-bit opcodes)
e_rlwimi	Rotate Left Word Immed then Mask Insert	VLE (32-bit opcodes)
e_rlwinm	Rotate Left Word Immed then AND with Mask	VLE (32-bit opcodes)
e_slwi	Shift Left Word Immediate	VLE (32-bit opcodes)
e_slwi.	Shift Left Word Immediate & record CR	VLE (32-bit opcodes)
e_srwi	Shift Right Word Immediate	VLE (32-bit opcodes)
e_srwi.	Shift Right Word Immediate & record CR	VLE (32-bit opcodes)

Table 3-11. Full Instruction Listing (continued)

Mnemonic	Instruction Name	Source
e_stb	Store Byte	VLE (32-bit opcodes)
e_stbu	Store Byte with Update	VLE (32-bit opcodes)
e_sth	Store Halfword	VLE (32-bit opcodes)
e_sthu	Store Halfword with Update	VLE (32-bit opcodes)
e_stmw	Store Multiple Word	VLE (32-bit opcodes)
e_stw	Store Word	VLE (32-bit opcodes)
e_stwu	Store Word with Update	VLE (32-bit opcodes)
e_subfic	Subtract from Immediate Carrying	VLE (32-bit opcodes)
e_subfic.	Subtract from Immediate and Record	VLE (32-bit opcodes)
e_xori	XOR Immediate	VLE (32-bit opcodes)
e_xori.	XOR Immediate and Record	VLE (32-bit opcodes)
icbi	Instruction Cache Block Invalidate	Book E
icblc	Instruction Cache Block Lock Clear	Cache locking
icbt	Instruction Cache Block Touch	Book E
icbtls	Instruction Cache Block Touch and Lock Set	Cache locking
isel	Integer Select	EIS
isync	Instruction Synchronize	Book E
lbz	Load Byte and Zero	Book E
lbzu	Load Byte and Zero with Update	Book E
lbzux	Load Byte and Zero with Update Indexed	Book E
lbzx	Load Byte and Zero Indexed	Book E
lha	Load Half Word Algebraic	Book E
lhau	Load Half Word Algebraic with Update	Book E
lhaux	Load Half Word Algebraic with Update Indexed	Book E
lhax	Load Half Word Algebraic Indexed	Book E
lhbrx	Load Half Word Byte-Reverse Indexed	Book E
lhz	Load Half Word and Zero	Book E
lhzu	Load Half Word and Zero with Update	Book E
lhzux	Load Half Word and Zero with Update Indexed	Book E
lhzx	Load Half Word and Zero Indexed	Book E
lmw	Load Multiple Word	Book E
lwarx	Load Word and Reserve Indexed	Book E
lwbrx	Load Word Byte-Reverse Indexed	Book E
lwz	Load Word and Zero	Book E
lwzu	Load Word and Zero with Update	Book E

Table 3-11. Full Instruction Listing (continued)

Mnemonic	Instruction Name	Source
lwzux	Load Word and Zero with Update Indexed	Book E
lwzx	Load Word and Zero Indexed	Book E
mbar[2]	Memory Barrier	Book E
mcrf	Move Condition Register Field	Book E
mcrxr	Move to Condition Register from XER	Book E
mfcr	Move From Condition Register	Book E
mfdcr[3]	Move From Device Control Register	Book E
mfdcrx[3]	Move From Device Control Register Indexed	Book E
mfmsr	Move From Machine State Register	Book E
mfspr	Move From Special Purpose Register	Book E
msync[2]	Memory Synchronize	Book E
mtcrf	Move To Condition Register Fields	Book E
mtdcr[3]	Move To Device Control Register	Book E
mtdcrx[3]	Move To Device Control Register Indexed	Book E
mtmsr	Move To Machine State Register	Book E
mtspr	Move To Special Purpose Register	Book E
mulhw	Multiply High Word	Book E
mulhw.	Multiply High Word and record CR	Book E
mulhwu	Multiply High Word Unsigned	Book E
mulhwu.	Multiply High Word Unsigned and record CR	Book E
mulli	Multiply Low Immediate	Book E
mullw	Multiply Low Word	Book E
mullw.	Multiply Low Word and record CR	Book E
mullwo	Multiply Low Word and record OV	Book E
mullwo.	Multiply Low Word and record OV and CR	Book E
nand	NAND	Book E
nand.	NAND and record CR	Book E
neg	Negate	Book E
neg.	Negate and record CR	Book E
nego	Negate and record OV	Book E
nego.	Negate and record OV and record CR	Book E
nor	NOR	Book E
nor.	NOR and record CR	Book E
or	OR	Book E
or.	OR and record CR	Book E

Table 3-11. Full Instruction Listing (continued)

Mnemonic	Instruction Name	Source
orc	OR with Complement	Book E
orc.	OR with Complement and record CR	Book E
ori	OR Immediate	Book E
oris	OR Immediate Shifted	Book E
rfci	Return From Critical Interrupt	Book E
rfdi	Return From Debug Interrupt	Debug
rfi	Return From Interrupt	Book E
rlwimi	Rotate Left Word Immed then Mask Insert	Book E
rlwimi.	Rotate Left Word Immed then Mask Insert and record CR	Book E
rlwinm	Rotate Left Word Immed then AND with Mask	Book E
rlwinm.	Rotate Left Word Immed then AND with Mask and record CR	Book E
rlwnm	Rotate Left Word then AND with Mask	Book E
rlwnm.	Rotate Left Word then AND with Mask and record CR	Book E
sc	System Call	Book E
se_add	Add	VLE (16-bit opcodes)
se_addi	Add Immediate	VLE (16-bit opcodes)
se_and	AND	VLE (16-bit opcodes)
se_and.	AND and Record	VLE (16-bit opcodes)
se_andc	AND with Complement	VLE (16-bit opcodes)
se_andi	And Immediate	VLE (16-bit opcodes)
se_b	Branch	VLE (16-bit opcodes)
se_bc	Branch Conditional	VLE (16-bit opcodes)
se_bclri	Bit Clear Immediate	VLE (16-bit opcodes)
se_bctr	Branch to Count Register	VLE (16-bit opcodes)
se_bctrl	Branch to Count Register & Link	VLE (16-bit opcodes)
se_bgeni	Bit Generate Immediate	VLE (16-bit opcodes)
se_bl	Branch and Link	VLE (16-bit opcodes)
se_blr	Branch to Link Register	VLE (16-bit opcodes)
se_blrl	Branch to Link Register & Link	VLE (16-bit opcodes)
se_bmaski	Bit Mask Generate Immediate	VLE (16-bit opcodes)
se_bseti	Bit Set Immediate	VLE (16-bit opcodes)
se_btsti	Bit Test Immediate	VLE (16-bit opcodes)
se_cmp	Compare	VLE (16-bit opcodes)
se_cmph	Compare Halfword	VLE (16-bit opcodes)
se_cmphl	Compare Halfword Logical	VLE (16-bit opcodes)

Table 3-11. Full Instruction Listing (continued)

Mnemonic	Instruction Name	Source
se_cmpi	Compare Immediate	VLE (16-bit opcodes)
se_cmpl	Compare Logical	VLE (16-bit opcodes)
se_cmpli	Compare Logical Immediate	VLE (16-bit opcodes)
se_extsb	Extend Sign Byte	VLE (16-bit opcodes)
se_extsh	Extend Sign Halfword	VLE (16-bit opcodes)
se_extzb	Extend with Zeros Byte	VLE (16-bit opcodes)
se_extzh	Extend with Zeros Halfword	VLE (16-bit opcodes)
se_illegal	Illegal	VLE (16-bit opcodes)
se_isync	Instruction Synchronize	VLE (16-bit opcodes)
se_lbz	Load Byte and Zero	VLE (16-bit opcodes)
se_lhz	Load Halfword and Zero	VLE (16-bit opcodes)
se_li	Load Immediate	VLE (16-bit opcodes)
se_lwz	Load Word and Zero	VLE (16-bit opcodes)
se_mfar	Move from Alternate Register	VLE (16-bit opcodes)
se_mfctr	Move From Count Register	VLE (16-bit opcodes)
se_mflr	Move From Link Register	VLE (16-bit opcodes)
se_mr	Move Register	VLE (16-bit opcodes)
se_mtar	Move to Alternate Register	VLE (16-bit opcodes)
se_mtctr	Move To Count Register	VLE (16-bit opcodes)
se_mtlr	Move To Link Register	VLE (16-bit opcodes)
se_mullw	Multiply Low Word	VLE (16-bit opcodes)
se_neg	Negate	VLE (16-bit opcodes)
se_not	NOT	VLE (16-bit opcodes)
se_or	OR	VLE (16-bit opcodes)
se_rfci	Return From Critical Interrupt	VLE (16-bit opcodes)
se_rfdi	Return From Debug Interrupt	VLE (16-bit opcodes)
se_rfi	Return From Interrupt	VLE (16-bit opcodes)
se_sc	System Call	VLE (16-bit opcodes)
se_slw	Shift Left Word	VLE (16-bit opcodes)
se_slwi	Shift Left Word Immediate	VLE (16-bit opcodes)
se_sraw	Shift Right Algebraic Word	VLE (16-bit opcodes)
se_srawi	Shift Right Algebraic Word Immediate	VLE (16-bit opcodes)
se_srw	Shift Right Word	VLE (16-bit opcodes)
se_srwi	Shift Right Word Immediate	VLE (16-bit opcodes)
se_stb	Store Byte	VLE (16-bit opcodes)

Table 3-11. Full Instruction Listing (continued)

Mnemonic	Instruction Name	Source
se_sth	Store Halfword	VLE (16-bit opcodes)
se_stw	Store Word	VLE (16-bit opcodes)
se_sub	Subtract	VLE (16-bit opcodes)
se_subf	Subtract From	VLE (16-bit opcodes)
se_subi	Subtract Immediate	VLE (16-bit opcodes)
se_subi.	Subtract Immediate and Record	VLE (16-bit opcodes)
slw	Shift Left Word	Book E
slw.	Shift Left Word and record CR	Book E
sraw	Shift Right Algebraic Word	Book E
sraw.	Shift Right Algebraic Word and record CR	Book E
srawi	Shift Right Algebraic Word Immediate	Book E
srawi.	Shift Right Algebraic Word Immediate and record CR	Book E
srw	Shift Right Word	Book E
srw.	Shift Right Word and record CR	Book E
stb	Store Byte	Book E
stbu	Store Byte with Update	Book E
stbux	Store Byte with Update Indexed	Book E
stbx	Store Byte Indexed	Book E
sth	Store Half Word	Book E
sthbrx	Store Half Word Byte-Reverse Indexed	Book E
sthu	Store Half Word with Update	Book E
sthux	Store Half Word with Update Indexed	Book E
sthx	Store Half Word Indexed	Book E
stmw	Store Multiple Word	Book E
stw	Store Word	Book E
stwbrx	Store Word Byte-Reverse Indexed	Book E
stwcx.	Store Word Conditional Indexed and record CR	Book E
stwu	Store Word with Update	Book E
stwux	Store Word with Update Indexed	Book E
stwx	Store Word Indexed	Book E
subf	Subtract From	Book E
subf.	Subtract From and record CR	Book E
subfc	Subtract From Carrying	Book E
subfc.	Subtract From Carrying and record CR	Book E
subfco	Subtract From Carrying and record OV	Book E

Table 3-11. Full Instruction Listing (continued)

Mnemonic	Instruction Name	Source
subfco.	Subtract From Carrying and record OV and CR	Book E
subfe	Subtract From Extended with CA	Book E
subfe.	Subtract From Extended with CA and record CR	Book E
subfeo	Subtract From Extended with CA and record OV	Book E
subfeo.	Subtract From Extended with CA and record OV and CR	Book E
subfic	Subtract From Immediate Carrying	Book E
subfme	Subtract From Minus One Extended with CA	Book E
subfme.	Subtract From Minus One Extended with CA and record CR	Book E
subfmeo	Subtract From Minus One Extended with CA and record OV	Book E
subfmeo.	Subtract From Minus One Extended with CA and record OV and CR	Book E
subfo	Subtract From and record OV	Book E
subfo.	Subtract From and record OV and CR	Book E
subfze	Subtract From Zero Extended with CA	Book E
subfze.	Subtract From Zero Extended with CA and record CR	Book E
subfzeo	Subtract From Zero Extended with CA and record OV	Book E
subfzeo.	Subtract From Zero Extended with CA and record OV and CR	Book E
tlbivax	TLB Invalidate Virtual Address Indexed	Book E
tlbre	TLB Read Entry	Book E
tlbsx	TLB Search Indexed	Book E
tlbsync	TLB Synchronize	Book E
tlbwe	TLB Write Entry	Book E
tw	Trap Word	Book E
twi	Trap Word Immediate	Book E
wrtee	Write External Enable	Book E
wrteei	Write External Enable Immediate	Book E
xor	XOR	Book E
xor.	XOR and record CR	Book E
xori	XOR Immediate	Book E
xoris	XOR Immediate Shifted	Book E

[1] An implementation can restrict the number of bits specified in a mask. Devices that implements 16-bit instructions are limited to 16 bits, which allows the user to perform bit-reversed address computations for 65536-byte samples.

[2] See Section 3.7, “Memory Synchronization and Reservation Instructions.”

[3] The core CPU will take an illegal instruction exception for unsupported DCR values.

11.3, 11-8 Added the following rows to Table 11-5, “Event Code Encodings (TCODE = 33)”:

1110	Entry into a VLE page from a non-VLE page
1111	Entry into a non-VLE page from a VLE page

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+33 1 69 35 48 48 (French)
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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
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