GENERAL INSTRUMENT	ER59256

34 Res Only

005828

5828 GF

256 BIT SERIAL ELECTRICALLY ERASABLE AND PROGRAMMABLE ROM

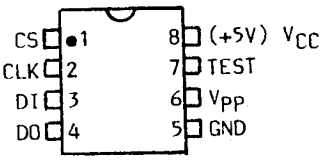
FEATURES

- Low cost
- 16 x 16 serial EEPROM
- Single +5V only operation
- Binary addressing
- Word and chip erasable
- Unlimited read accesses
- Fully TTL compatible inputs and outputs
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL-STD 883
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word
- 0°C to +70°C operating ambient temperature range
- Power on/off data protection circuitry

PIN CONFIGURATION

8 Pin Dual-In-Line

TOP VIEW



PIN FUNCTIONS

CS	Chip Select
CLK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+5V Power Supply
GND	Ground

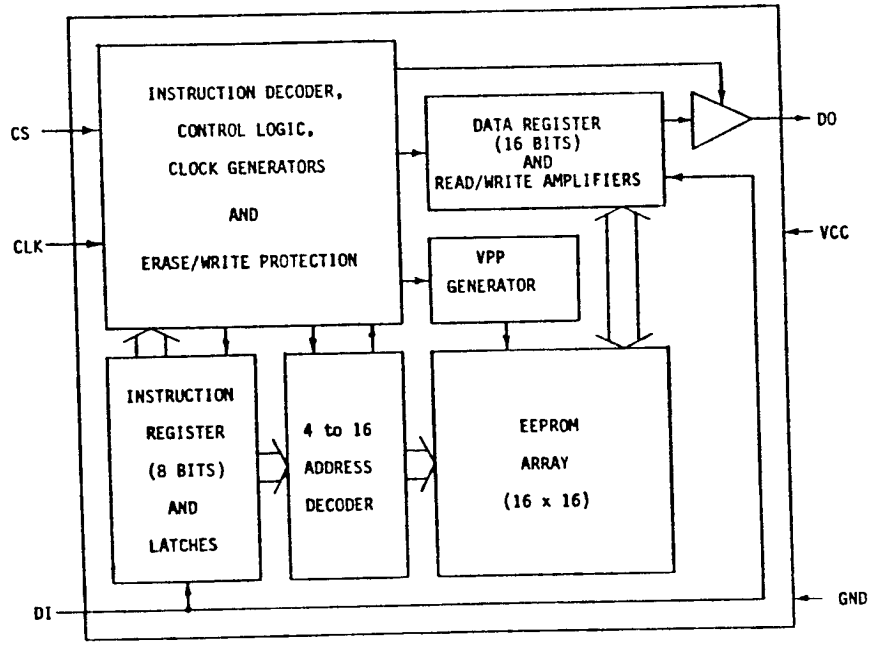
TEST PINS

V_{PP}	High Voltage Test (Float)
TEST	EEPROM Margin Test (Ground/Float)

DESCRIPTION

The ER59256 is a low cost, serial EEPROM manufactured in General Instrument's highly reliable SNOS technology. The key features of this device are its +5V only operation and microcomputer compatible architecture. Six 9-bit instructions can be executed. See Table 1. The instruction format has a logical "1" as a start bit, four bits as an op code, and four bits of address. See Table 1.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to ground..... +7V to -0.3V
Storage temperature (unpowered and without data retention)..... -65°C to 150°C
Soldering temperature of leads (10 seconds)..... +300°C

Standard Conditions (unless otherwise noted)

V_{CC} = +5 ± 10% volts
GND = 0 volts
Operating Temperature Range (T_A):
0°C to +70°C (Commercial)

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data labelled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty, expressed or implied, as to the merchantability of fitness for a particular purpose of this device or its software supplied to the customer.

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
High Level Input Voltage	V_{IH}	2.0	-	V_{CC}+1.0	V	
Low Level Input Voltage	V_{IL}	-0.3	-	+0.8	V	
High Level Output Voltage	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -400µA
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 3.2mA
Input Leakage Current	I_{LI}	-	-	+10	µA	V_{IN} = GND to V_{CC}
Output Leakage Current	I_{LO}	-	-	+10	µA	V_{OUT} = GND to V_{CC}
POWER SUPPLY REQUIREMENTS						
Operating Current	I_{CC}^1	-	-	10	mA	V_{CC} = 5.5V, CS = 1
Standby Current	I_{CC}^2	-	-	3	mA	V_{CC} = 5.5V, CS = 0
E/W Operating Current	I_{CC}^3	-	-	12	mA	V_{CC} = 5.5V
Power Consumption (Operating)	P_{CC}^1	-	-	55	mW	V_{CC} = 5.5V, CS = 1
Power Consumption (Standby)	P_{CC}^2	-	-	17	mW	V_{CC} = 5.5V, CS = 0
Power Consumption (E/W)	P_{CC}^3	-	-	66	mW	V_{CC} = 5.5V, CS = 1

AC CHARACTERISTICS

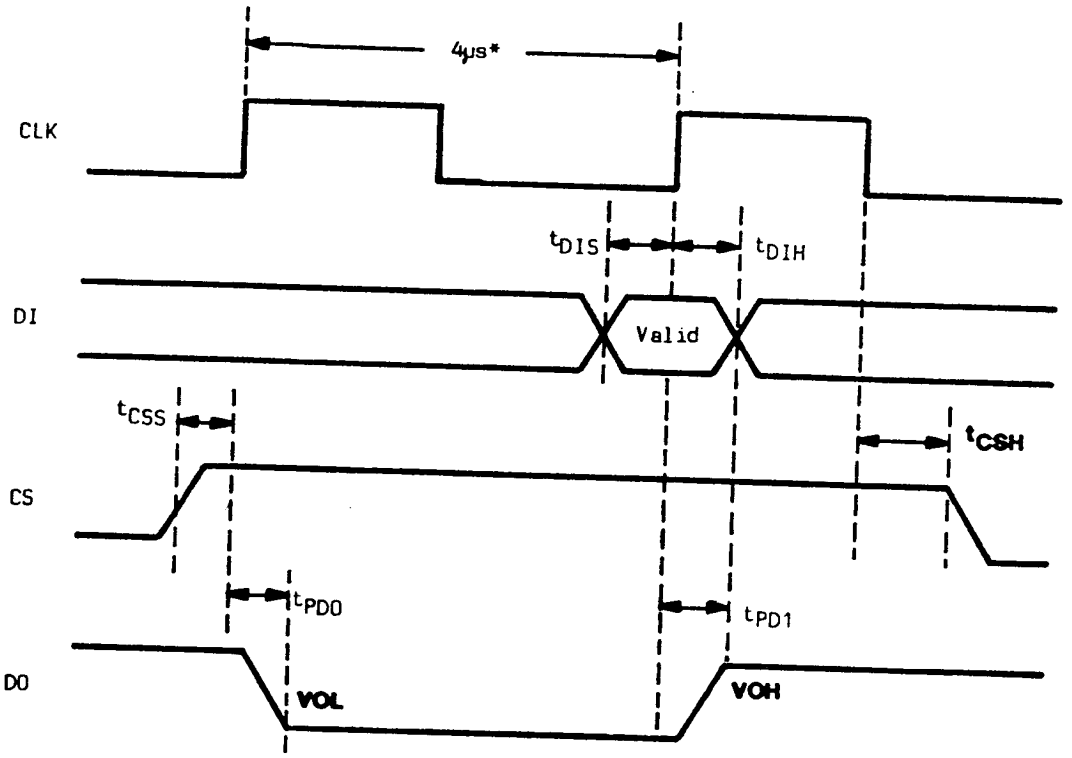
Characteristic	Sym	Min	Typ	Max	Units	Conditions
Clock Frequency	f_{CLK}	0	-	250	KHZ	
Clock Duty Cycle	D_{CLK}	25	-	75	%	
Chip Select Setup Time	t_{CSS}	0.2	-	-	µs	
Chip Select Hold Time	t_{CSH}	0	-	-	µs	
Data Input Setup Time	t_{DIS}	0.4	-	-	µs	
Data Input Hold Time	t_{DIH}	0.4	-	-	µs	
DO Output Delay (H to L)	t_{PDO}	-	-	2	µs	C_L = 100pf
DO Output Delay (L to H)	t_{PDI}	-	-	2	µs	C_L = 100pf
Erase/Write Pulse Width	$t_{E/W}$	10	-	30	ms	
Input Capacitance	C_I	-	-	6	pf	V_{IN} = 0V
Output Capacitance	C_O	-	-	10	pf	V_{OUT} = 0V

DS20014H-2

Table 1 - Instruction Set

Instruction	SB	Op Code	Address	Data	Comments
READ	1	1000	A3A2A1A0		Read register A3A2A1A0
WRITE	1	0100	A3A2A1A0	D15-D0	Write register A3A2A1A0
ERASE	1	1100	A3A2A1A0		Erase Register A3A2A1A0
EWEN	1	0011	0000		Erase/write enable
EWDS	1	0000	0000		Erase/write disable
ERAL	1	0010	0000		Erase all registers

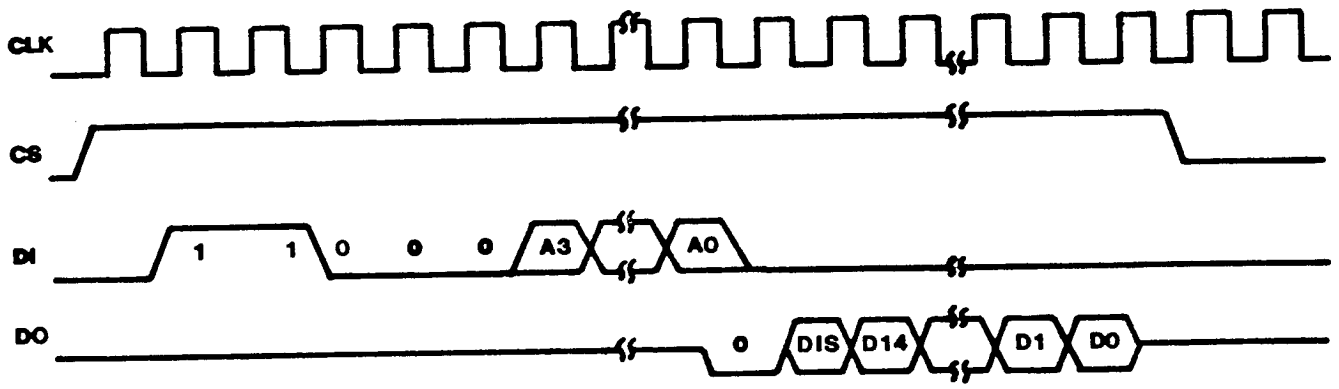
Figure 1. Synchronous Data Timing



*This is the maximum clock frequency.

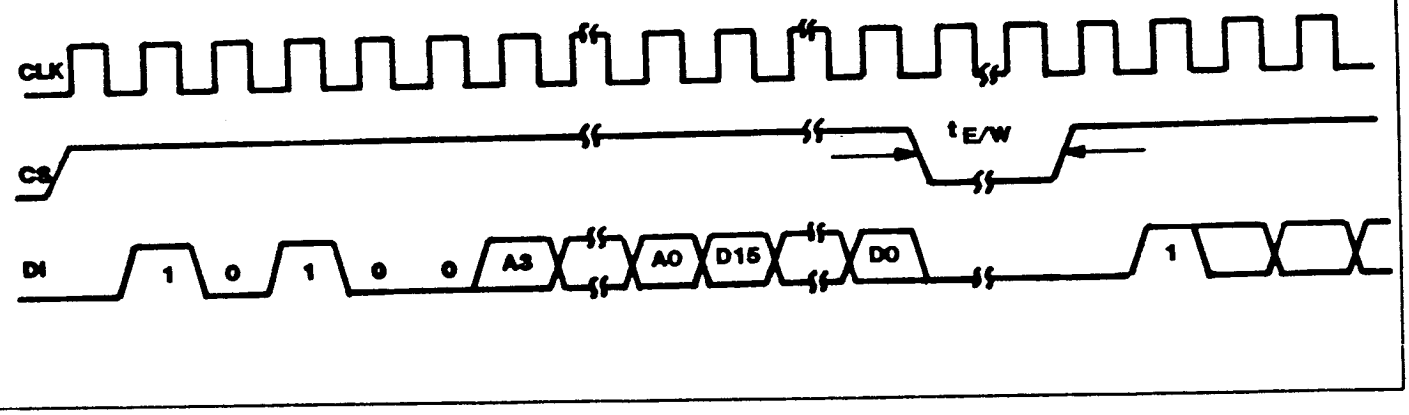
DS20014H-3

Figure 2. Read Mode



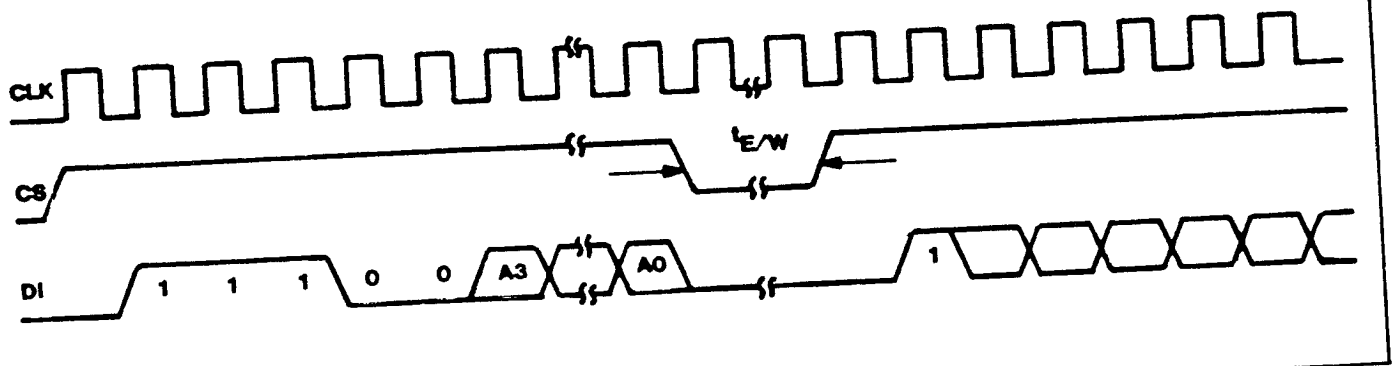
The READ instruction is the only instruction which outputs serial data on the DO pin. Only during the READ mode is the output pin (DO) valid. During all other modes the DO pin is in tri-state, eliminating bus contention. A dummy bit (logical "0") precedes the 16-bit output string. The output data changes during the high state of the system clock.

Figure 3. Write Mode



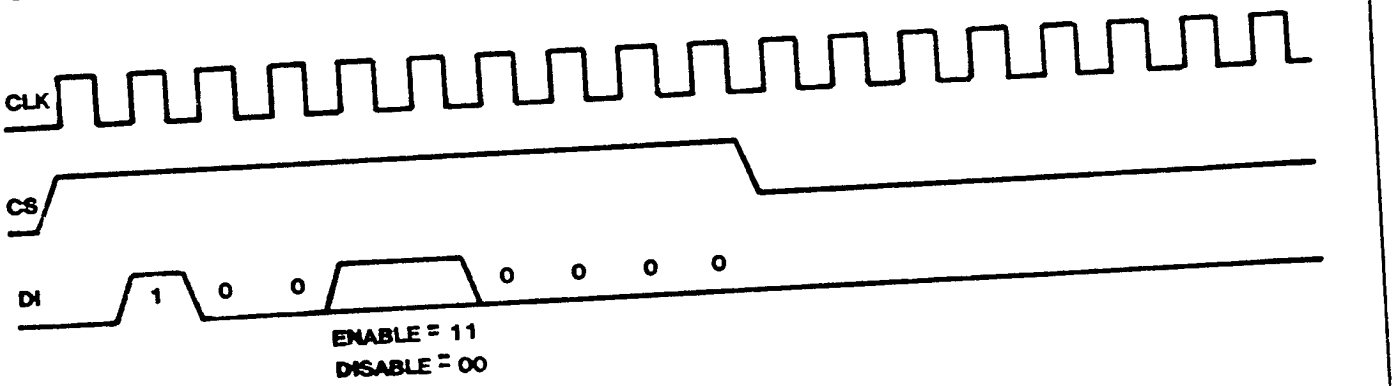
The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycle ends. All programming modes should be ended with CS high for one CLK period, or followed by another instruction.

Figure 4. Erase Mode



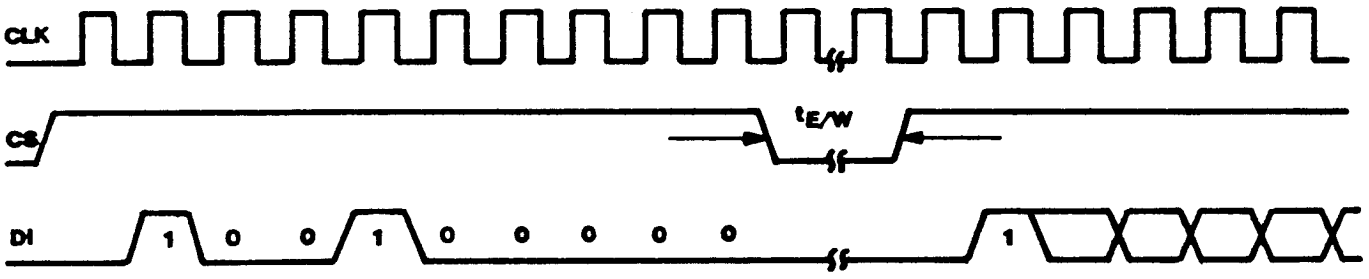
Like most E^2PROMs, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one CLK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

Figure 5. Erase/Write Enable and Disable



Programming must be preceded once by an Erase/Write Enable (EWEN) instruction. Programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions. The device powers up in the Erase/Write Disable (EWDS) mode.

Figure 6. Chip Erase Mode

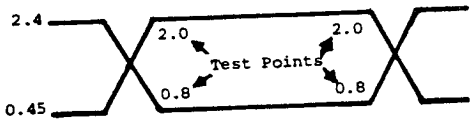


Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

DI/DO: It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A_0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A_0. The higher the current sourcing capability of A_0, the higher the voltage at the Data Out pin.

Power On/Off Data Protection Circuitry: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

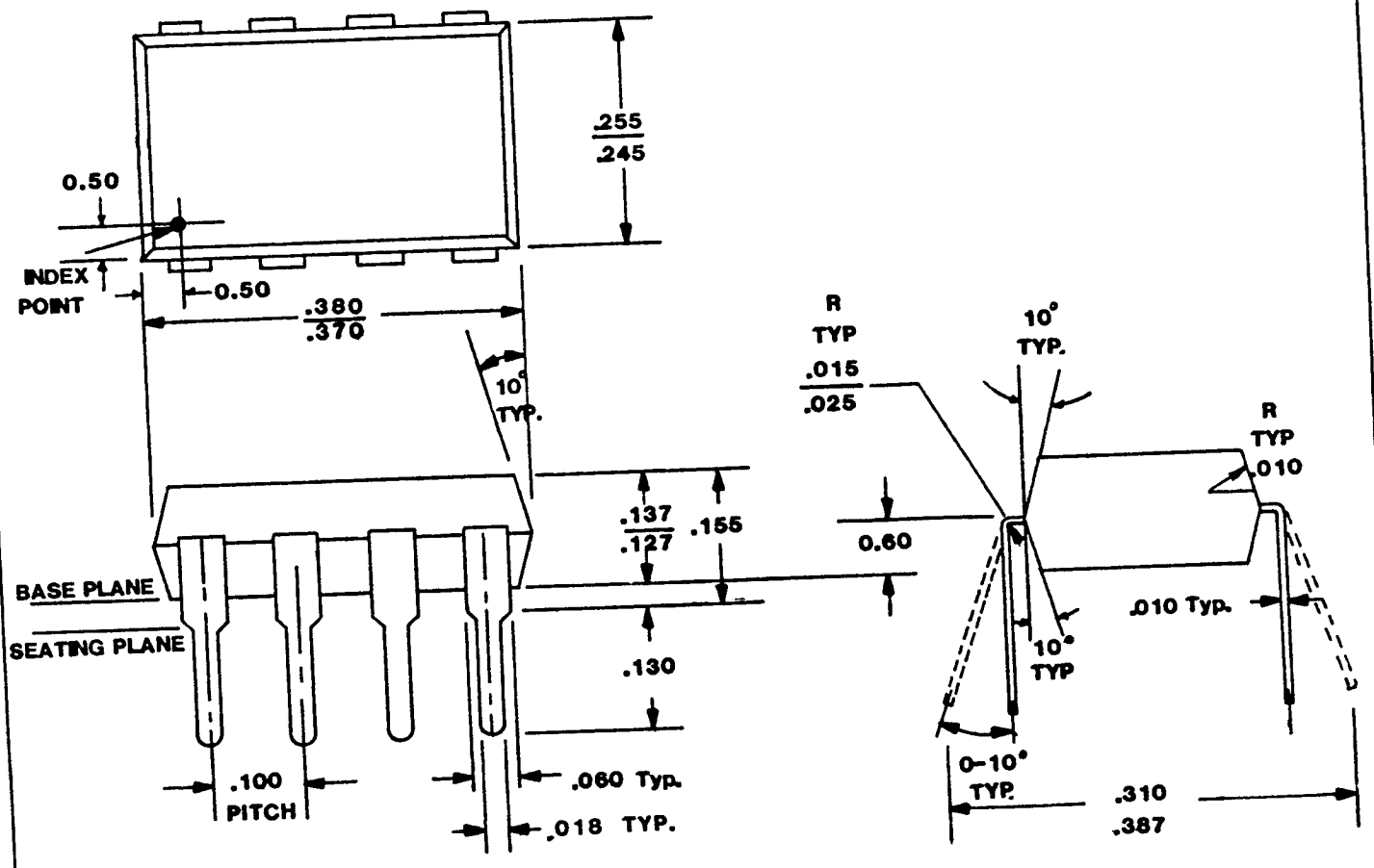
A.C. Testing Input/Output Waveform



A.C. Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

PACKAGE OUTLINE

8 Lead Dual-In-Line (All dimensions are in inches)



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

DS20014H-7