HA13568AT

CD-ROM Combo Driver

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Description

The HA13568AT is combination of Spindle, Forcus, Tracking, Slide, Tray designed for CD-ROM and have following functions and features.
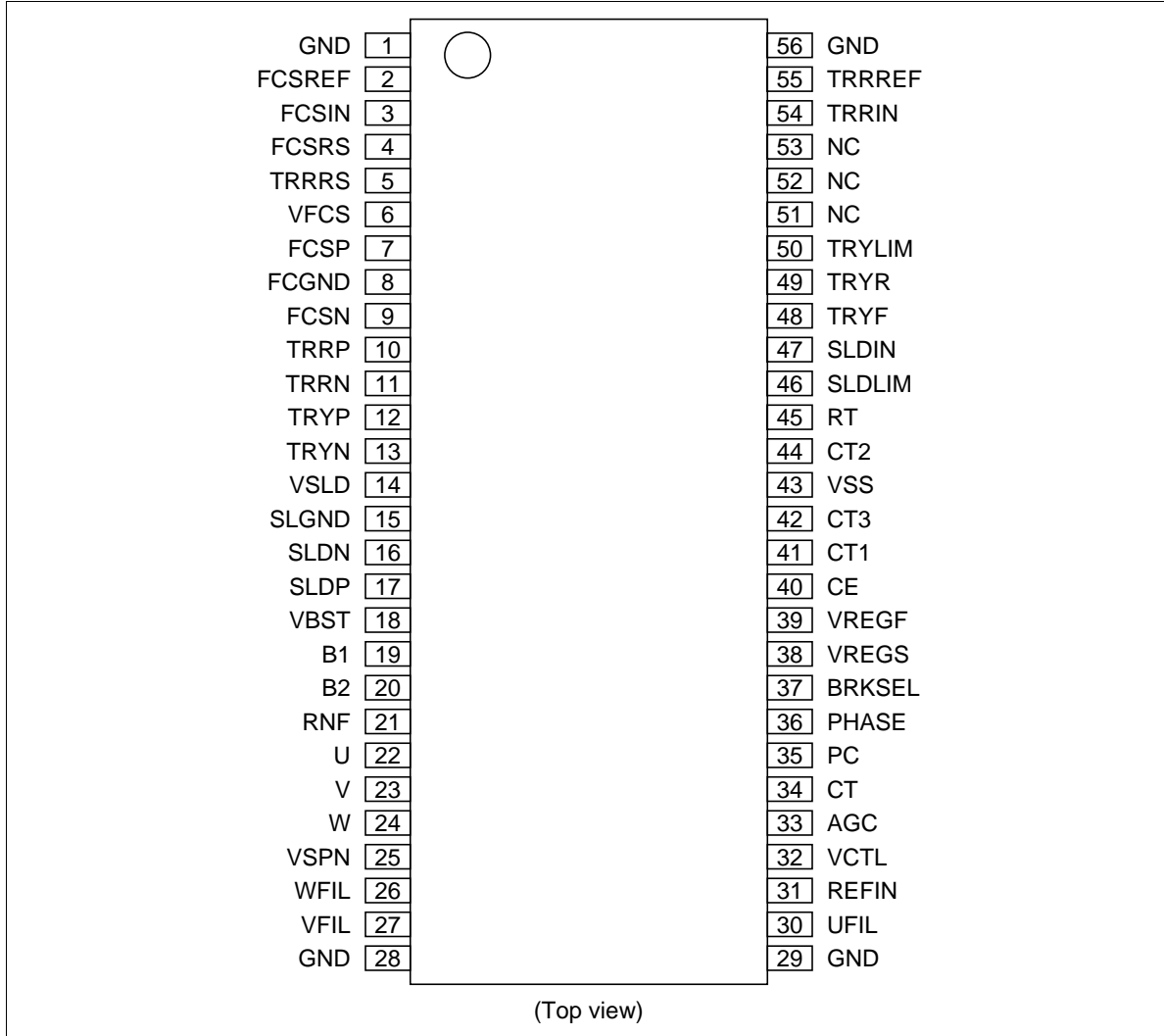
Features

- 1.5 A sensorless spindle driver
- 0.5 A BTL focus driver
- 0.5 A BTL tracking driver
- 1.5 A H bridge slide motor driver
- 0.5 A H bridge tray motor driver
- Over temperature shut down (OTSD)
- Voltage regulator control circuit

Functions

- Sensorless driver with self start
- Soft switching drive
- Snubberless
- Low output saturation voltage
- Direct PWM slide driver

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Pin Arrangement

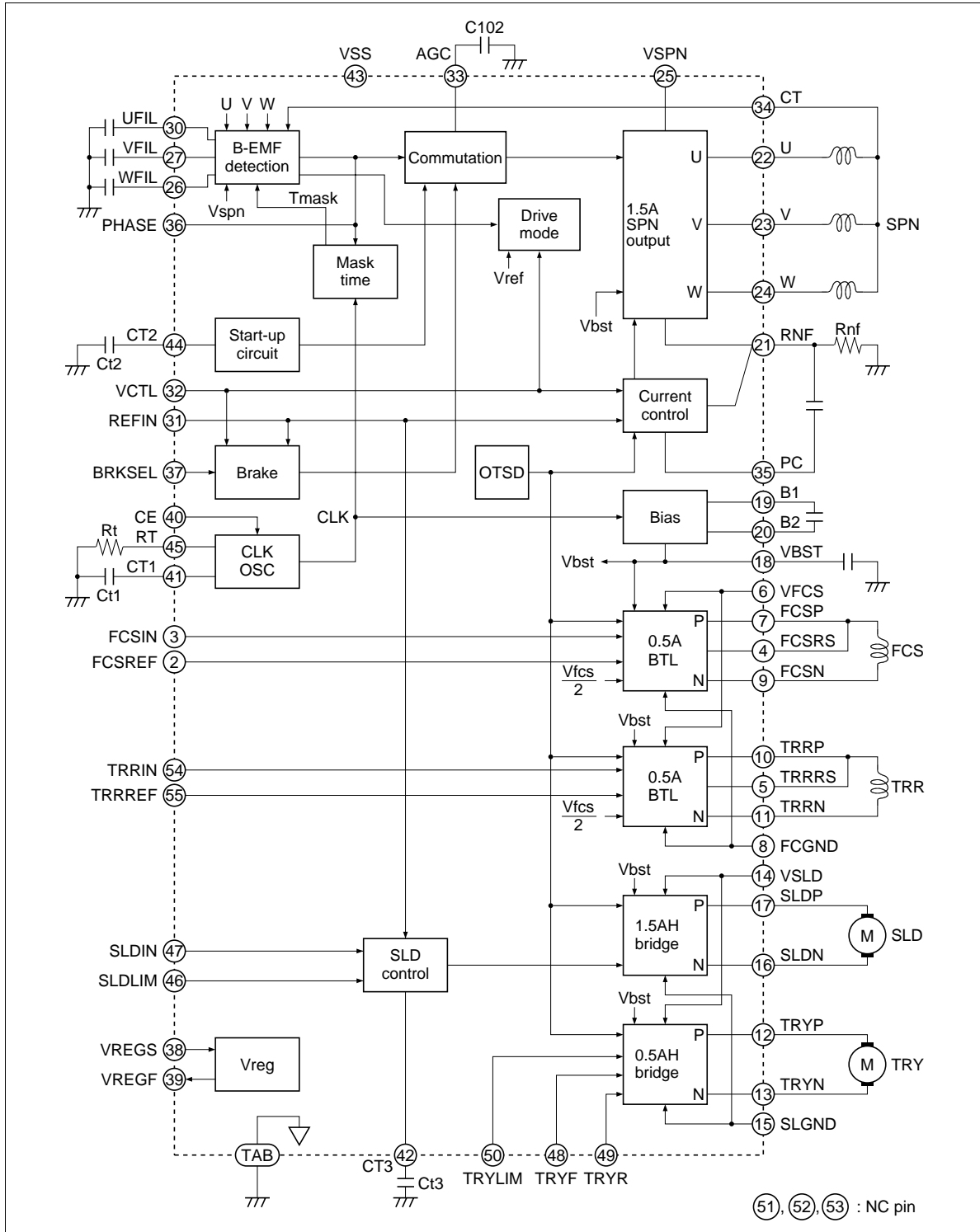| Pin	Name		Pin	Name
1	GND		56	GND
2	FCSREF		55	TRRREF
3	FCSIN		54	TRRIN
4	FCSRS		53	NC
5	TRRRS		52	NC
6	VFCS		51	NC
7	FCSP		50	TRYLIM
8	FCGND		49	TRYR
9	FCSN		48	TRYF
10	TRRP		47	SLDIN
11	TRRN		46	SLDLIM
12	TRYP		45	RT
13	TRYN		44	CT2
14	VSLD		43	VSS
15	SLGND		42	CT3
16	SLDN		41	CT1
17	SLDP		40	CE
18	VBST		39	VREGF
19	B1		38	VREGS
20	B2		37	BRKSEL
21	RNF		36	PHASE
22	U		35	PC
23	V		34	CT
24	W		33	AGC
25	VSPN		32	VCTL
26	WFIL		31	REFIN
27	VFIL		30	UFIL
28	GND		29	GND

(Top view)

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Pin Description

Pin No.	Pin Name	Function
2	FCSREF	FCS driver block reference voltage
3	FCSIN	FCS control input pin
4	FCSRS	FCS sense pin
5	TRRRS	TRR sense pin
6	VFCS	FCS driver and TRR driver power supply
7	FCSP	FCS driver P output
8	FCGND	FCS driver and TRR driver GND
9	FCSN	FCS driver N output
10	TRRP	TRR driver P output
11	TRRN	TRR driver N output
12	TRYP	TRY driver P output
13	TRYN	TRY driver N output
14	VSLD	SLD driver and TRY driver power supply
15	SLGND	SLD driver and TRY driver GND
16	SLDN	SLD driver N output
17	SLDP	SLD driver P output
18	VBST	Booster output pin. This circuit generates a voltage about 1.5 V above that of the VSPN pin.
19	B1	Booster pumping capacitor connection
20	B2	
21	RNF	Spindle driver current detection
22	U	U phase output
23	V	V phase output
24	W	W phase output
25	VSPN	Spindle and booster power supply
26	WFIL	W phase low pass filter. Connect a filter C to this pin during GND.
27	VFIL	V phase low pass filter. Connect a filter C to this pin during GND.
30	UFIL	U phase low pass filter. Connect a filter C to this pin during GND.
31	REFIN	Reference voltage of spindle and slide
32	VCTL	Spindle control input. Generates forward torque when a DC voltage higher than REFIN is applied, and brake when a DC voltage lower than REF is applied.
33	AGC	For AGC. Holds the level used for IC internal processing fixed even if the B-EMF level fluctuates due to the rotation speed.
34	CT	Spindle center tap
35	PC	Spindle driver phase compensation

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Pin Description (cont)

Pin No.	Pin Name	Function
36	PHASE	Outputs the B-EMF zero cross phase. Open corrector. (See the timing chart)
37	BRKSEL	To select the brake mode. Lo: Short brake, Hi: Reverse full brake (when forward torque input: BRKSEL = H)
38	VREGS	Voltage regulator sense pin (VREGS ≈ 3.3 V output)
39	VREGF	Voltage regulator force pin
40	CE	Chip enable. Input Hi: active
41	CT1	Time constant for clock oscillator circuit. The clock oscillator frequency is determined by the external capacitor and resistor Ct1 and Rt.
42	CT3	Time constant for PWM carrier oscillator. The carrier frequency is determined by the external capacitor and resistor Ct3 and Rt.
43	VSS	Control block power supply. 5 V
44	CT2	Time constant for start-up oscillator. The start-up oscillator frequency is determined by the external capacitor and resistor Ct2 and Rt.
45	RT	Reference voltage (3.3 V). The IC's internal reference current is determined by this voltage and the external resistor Rt.
46	SLDLIM	SLD output maximum duty setting
47	SLDIN	SLD control input pin
48	TRYF	TRY driver forward input
49	TRYR	TRY driver reverese input
50	TRYLIM	TRY output voltage setting pin
51	NC	No connection
52	NC	
53	NC	
54	TRRIN	TRR control input pin
55	TRRREF	TRR driver block reference voltage
1, 28, 29, 56, TAB		GND

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Block Diagram

C102

VSS ⑬ AGC ㉝ VSPN ㉕

CT ㉞

UFIL ㉚
VFIL ㉗
WFIL ㉖

U V W

B-EMF detection

Commutation

1.5A SPN output

U ㉒ U
V ㉓ V — SPN
W ㉔ W

Vspn Tmask

PHASE ㊱

Drive mode

Vref

Mask time

Vbst

RNF ㉑ Rnf

CT2 ㊹ Start-up circuit
Ct2

VCTL ㉜

REFIN ㉛

Current control

PC ㉟

BRKSEL ㊲ Brake

OTSD

Bias
B1 ⑲
B2 ⑳

CE ㊵
RT ㊺
Rt
CT1 ㊶
Ct1

CLK OSC

CLK

Vbst

VBST ⑱

VFCS ⑥
FCSP ⑦
FCSRS ④
FCSN ⑨

FCS

FCSIN ③
FCSREF ②

0.5A BTL

P

Vfcs/2

N

Vbst

TRRP ⑩
TRRRS ⑤
TRRN ⑪

TRR

TRRIN �54
TRRREF �55

0.5A BTL

P

Vfcs/2

N

FCGND ⑧

Vbst

VSLD ⑭
SLDP ⑰

SLDN ⑯

1.5AH bridge

P

N

M SLD

SLDIN ㊼
SLDLIM ㊻

SLD control

Vbst

TRYP ⑫

TRYN ⑬

0.5AH bridge

P

N

M TRY

VREGS ㊳
VREGF ㊴

Vreg

SLGND ⑮

TAB

CT3 ㊷
Ct3

TRYLIM ㊿
TRYF ㊽
TRYR ㊾

㊶, ㊷, ㊸ : NC pin

Timing Chart

1. Start-up

CE

0

Tc2

CT2

Vhct2
Vlct2

0

2Tc2 4Tc2 4Tc2 4Tc2 4Tc2 4Tc2 6Tc2 8Tc2 10Tc2 12Tc2 14Tc2 16Tc2

Output
current
(U phase)

+
0
−

Output
current
(V phase)

+
0
−

Output
current
(W phase)

+
0
−

PHASE 0

B-EMF
Mask period

Synchronous mode

B-EMF mode

Note: Tc2 is as follows.

$$Tc2 = \frac{8\,(Vhct2 - Vlct2)\,Rt\,Ct2}{Vrt}$$

Where, Vhct2 : CT2 pin high voltage (See electrical characteristics)
Vlct2 : CT2 pin low voltage (See electrical characteristics)

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2. Acceleration (switching mode)
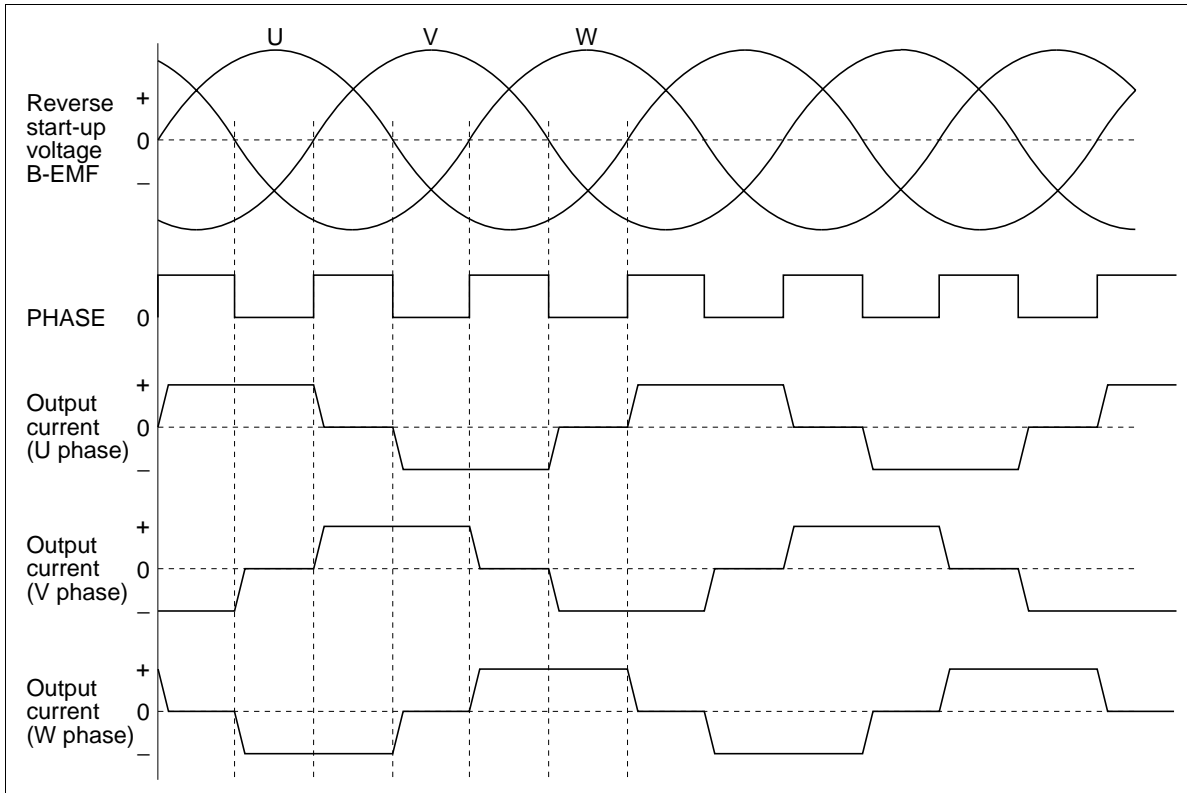
3. Running (soft switching mode)

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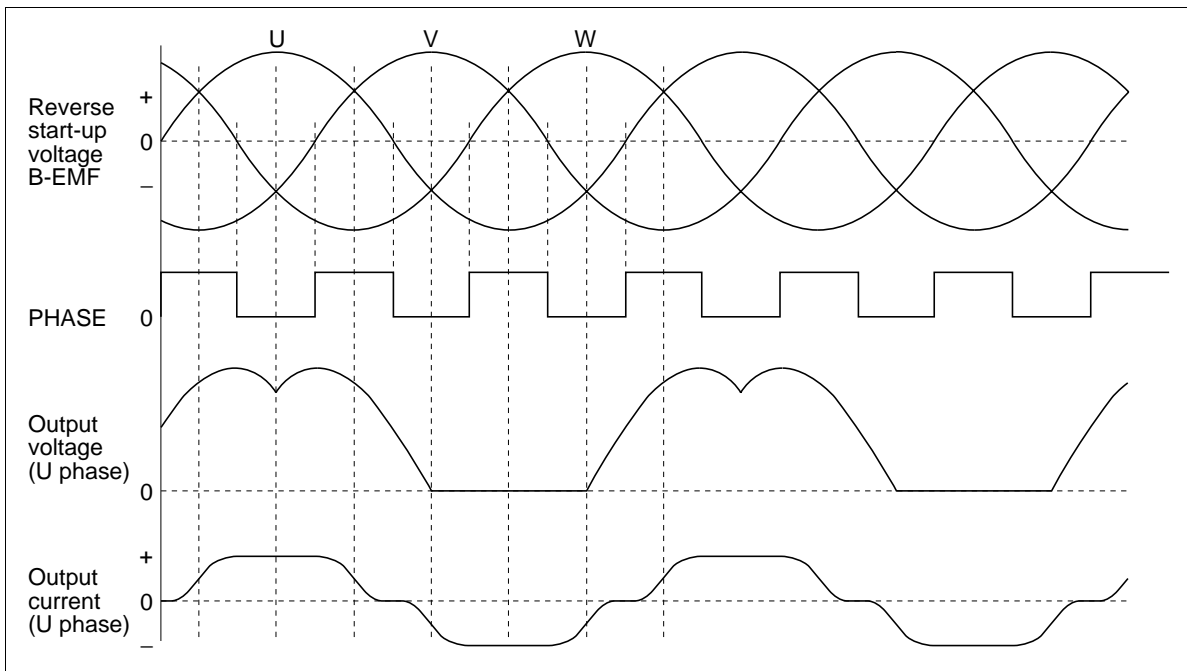
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Truth Table

Table 1   **Overall**

CE	OTSD	SPN Driver	FCS Driver	TRR Driver	SLD Driver	TRY Driver
L	X	Z	Z	Z	Z	Z
H	ON	Z	Z	Z	Z	Z
	OFF	ON	ON	ON	ON	ON

Note: X: Option, Z: Hi impedance

Table 2   **SPN Driver**

BRKSEL	VCTL	SPN Driver
X	> REFIN	Forward torque
	REFIN	Z
L	< REFIN	Short brake
H	REFIN – 0.6 V	Reverse brake

Note: X: Option, Z: Hi impedance

Table 3   **TRY Driver**

TRYF	TRYR	P Output	N Output
L	L	Z	Z
L	H	L	H
H	L	H	L
H	H	H	H

Note: Z: Hi impedance

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Application

1. FCS, TRR voltage drive
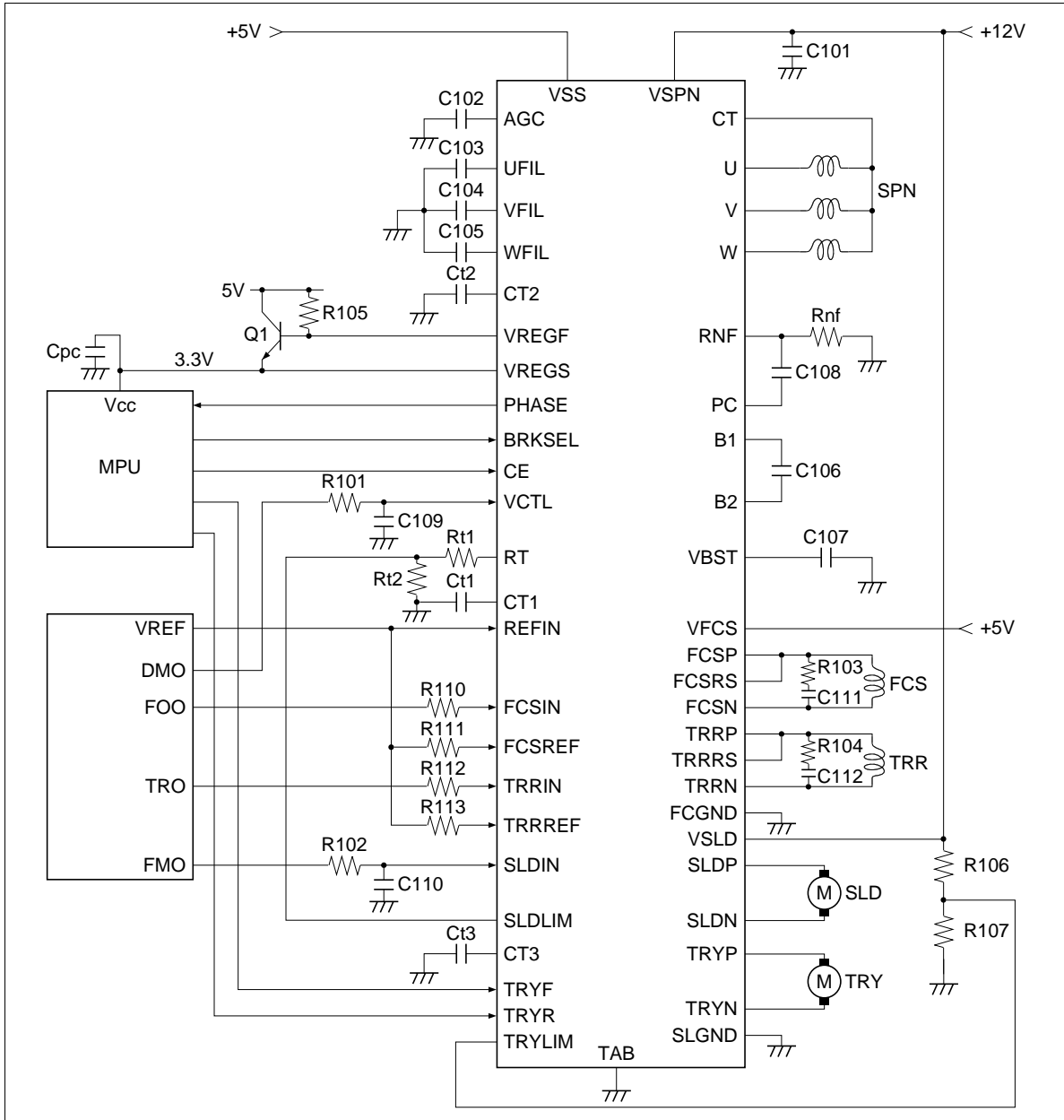
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2. FCS, TRR voltage drive

Note: Other pins have the same connections as those used in application 1.
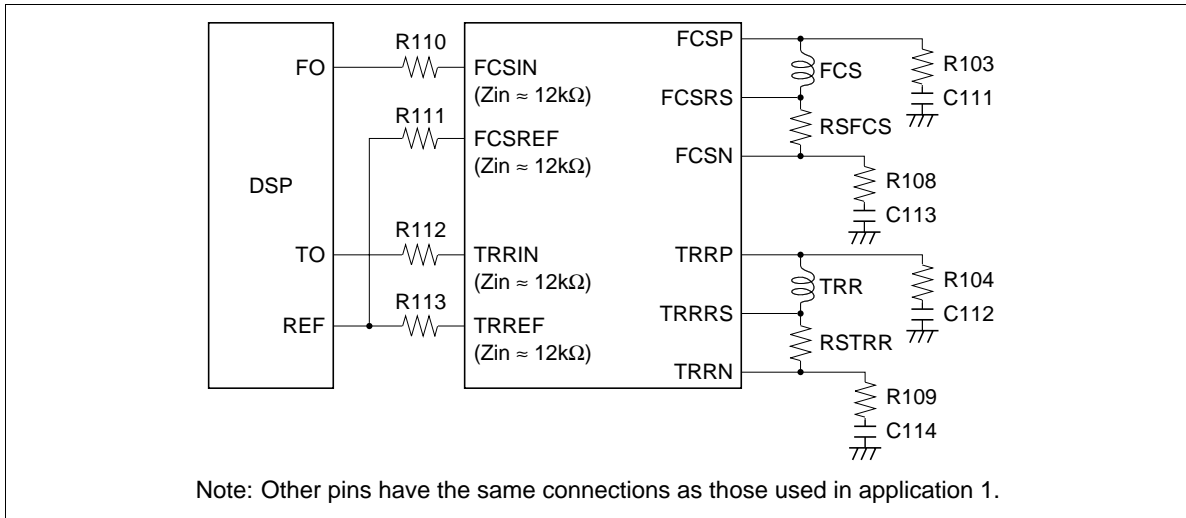
3. When used at a voltage other than 3.3 V with a voltage regulator (Vout = 3.3 to Vcc – 1 V)

Note: Other pins have the same connections as those used in application 1.

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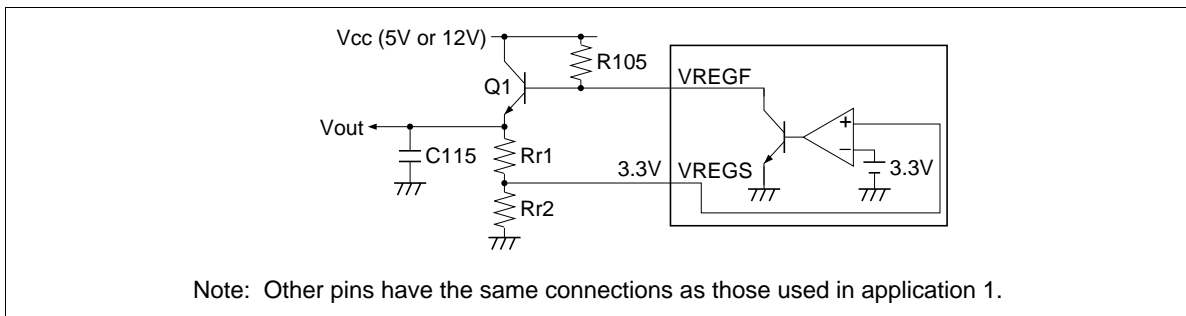
External Components

Parts No.	Reccomended Value	Reccomended Range	Purpose	Note
R101	47 kΩ	≤ 47 kΩ	Filter for SPN driver control input	
R102	47 kΩ	≤ 47 kΩ	Filter for SLD driver control input	
R103	6.8 Ω	—	To stop FCS block oscillation	
R104	6.8 Ω	—	To stop TRR block oscillation	
R105	500 Ω	≥ 100 Ω	for Q1 bias	
R106	20 kΩ	—	for TRY driver output voltage setting	
R107	27 kΩ	—		
R108	6.8 Ω	—	To stop FCS block oscillation	
R109	6.8 Ω	—	To stop TRR block oscillation	
R110 to R113	20 kΩ	—	for BTL gain setting	7
Rnf	0.25 Ω	≥ 0.25 Ω	SPN driver current detection resistor	1
Rt1	1.8 kΩ	Rt1 + Rt2 = 10 kΩ	Reference current setting and SLD driver maximum duty setting	2, 5
Rt2	8.2 kΩ			
RSFCS	1 Ω	≥ 0.33 Ω	for FCS driver current sense	7
RSTRR	1 Ω	≥ 0.33 Ω	for TRR driver current sense	
Rr1	—	—	Voltage regulator division resistor	8
Rr2	—	—		
C101	0.1 μF	≥ 0.1 μF	for Power supply by passing	
C102	0.047 μF		for B-EMF Amplitude AGC	
C103	0.01 μF		for B-EMF filter	6
C104				
C105				
C106	0.22 μF	≥ 0.22 μF	for Booster pumping	
C107	0.47 μF	≥ 0.47 μF	for Booster output smoothing	
C108	0.1 μF		for SPN driver phase compensation	
C109	0.01 μF		Filter for SPN control input	
C110	3300 pF		Filter for SLD control input	
C111	0.01 μF	—	To stop FCS block oscillation	
C112	0.01 μF	—	To stop TRR block oscillation	
C113	0.01 μF	—	To stop FCS block oscillation	
C114	0.01 μF	—	To stop TRR block oscillation	
C115	2.2 μF		for Voltage regulator smoothing	

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External Components (cont)

Parts No.	Reccomended Value	Reccomended Range	Purpose	Note
Ct1	150 pF	≥ 120 pF	Time constant for CLK oscillation. Use a capacitor with good temperature characteristics.	3
Ct2	0.033 μF		Time constant for start-up oscillation. Use a capacitor with good temperature characteristics.	4
Ct3	470 pF	≥ 390 pF	PWM carrier oscillation time constant	5
Q1			Transistor for voltage regulator	

Note: 1. The output current maximum value Iospnmax of SPN driver is controlled according to the following equation. However, Vspncl is the current limiter reference voltage. (See the electrical characteristics)

$$Iospnmax = \frac{Vspncl}{Rnf}$$

2. The maximum duty Dmax of SLD driver output is controlled according to the following equation.

$$Dmax = \frac{Vrt}{Vhct3 - Vlct3}\left(\frac{Rt2}{Rt} - \frac{Vlct3}{Vrt}\right) \times 100 \ (\%)$$

However,

$$Rt = Rt1 + Rt2, \qquad \frac{Rt2}{Rt} \geq \frac{Vlct3}{Vrt}$$

Where, Vrt   : RT pin voltage (See the electrical characteristics)

Vlct3 : CT3 pin low voltage ($\approx$ 1.3 V)

Vhct3 : CT3 pin high voltage ($\approx$ 3.3 V)

Since Vrt $\approx$ Vhct3, Dmax is not limited at 100% when Rt1 = 0 Ω.

3. The CLK oscillation frequency is determined by the following equation.

$$fclk = \frac{Vrt}{8 \ Ct1 \ Rt \ \Delta Vct1}$$

Where, Vrt   : RT pin voltage (See the electrical characteristics)

ΔVct1 : CT1 pin voltage amplitude ($\approx$ 1 V)

4. The Ct2 for start-up oscillation is determined by the following equation.

$$Tc2 = \frac{1}{6} \sqrt{\frac{J}{P \ Kt \ Ispnmax}}$$

$$Ct2 = \frac{Tc2 \ Vrt}{8 \ Rt \ (Vhct2 - Vlct2)}$$

Where, J   : Spindle motor inertia (kg $\cdot$ cm $\cdot$ S^2)

P   : Number of spindle motor poles (Total number of S poles and N poles)

Kt   : Spindle motor torque constant (kg $\cdot$ cm / A)

Vhct2 : CT2 pin high voltage ($\approx$ 3.3 V)

Vlct2 : CT2 pin low voltage ($\approx$ 1.3 V)

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5. The PWM oscillation frequency fpwm is determined by the following equation.

$$fpwm = \frac{Vrt}{8\ Ct3\ Rt\ (Vhct3 - Vlct3)}$$

Where, Vhct3 : CT3 pin high voltage ($\approx$ 3.3 V)

Vlct3 : CT3 pin low voltage ($\approx$ 1.3 V)

6. The C103 to C105 for B-EMF filter are determined by the following equation.

$$\frac{21}{\pi \cdot Rflt \cdot No \cdot P} \leq C103 \leq \frac{35}{\pi \cdot Rflt \cdot No \cdot P}$$

Where, Rfill : B-EMF detection output resistor (See the electrical characteristics)

No : Maximum rotation speed (rpm)

7. The FCS and TRR is determined by the following equation.

Voltage drive:

$$Gv = \frac{R1}{Rin + R2}$$

Current drive:

$$Gm = \frac{R1}{((Rin + R2) \cdot Rs)}$$

Where, R1 : Resistor of IC inside ($\approx$30kΩ)

R2 : Resistor of IC inside ($\approx$7kΩ)

Rin : Resistor value inserted in the input (Ω)
(R110 to R113)

Rs : Current sense resistor (Ω)

8. The output voltage Vout of voltage regulator is determined by the following equation.

$$Vout = 3.3 \left(1 + \frac{Rr1}{Rr2}\right)$$

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Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit	Note
Supplu voltage	Vss	7	V	1
SPN supply voltage	Vspn	15	V	1
FCS & TRR supply voltage	Vfcs	15	V	1
SLD & TRY supply voltage	Vsld	15	V	1
Input voltage	Vin	0 to Vss	V	2
	Vintrylim	Vss to Vsld	V	
SPN output current	Iospn	1.5	A	3
FCS & TRR & TRY output current	Iofcs	0.5	A	3
SLD output current	Iosld	1.5	A	3
Power dissipation	P_T	5	W	4
Junction temperature	Tj	160	°C	1
Storage temperature range	Tstg	−55 to +125	°C	

Note: 1. Operating voltage range is shown below.

Vss = 4.25 to 5.75 V

Vspn = 4.25 to 13.8 V

Vfcs = 4.25 to 13.8 V (However, the output high voltage is clamped at 7 V.)

Vsld = 4.25 to 13.8 V

Tjopr = 0 to +135°C

2. Applied to BRKSEL, VCTL, REFIN, CE, FCSIN, FCSREF, TRRIN, TRRREF, SLDIN, SLDLIM, TRYF and TRYR.

3. ASO (Area of Safety Operation) of each output transistor is shown below (TBD).

ASO of SPN driver | ASO of SLD driver
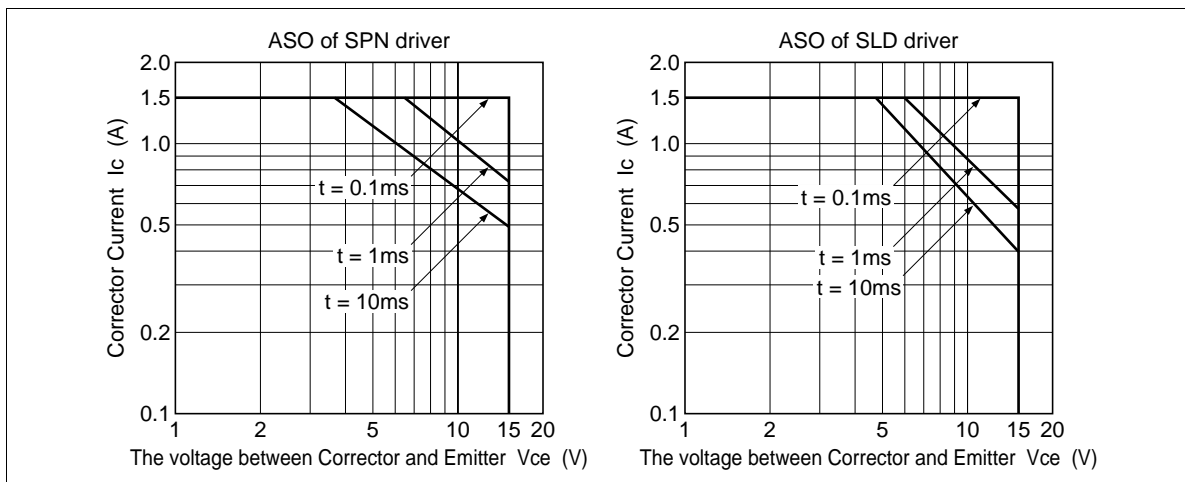
4. Thermal resistance is shown below.

θj-tab ≤ 12°C / W (back side tab soldering area is 70% or more)

θj-a ≤ 25°C / W (mounted on 4 layer multi glass-epoxy board, back side tab soldering area is 70% or more)

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Electrical Characteristics
(Ta = 25°C, Vss = 5 V, Vspn = 12 V, Vfcs = 5 V, Vsld = 12 V)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
Quiescent current		Iss0	—	0.7	0.9	mA	CE = L	VSS	
		Ispn0	—	—	0.2	mA		VSPN	
		Ifcs0	—	—	0.01	mA		VFCS	
		Isld0	—	—	0.01	mA		VSLD	
		Iss1	14	20	25	mA	CE = H, VCTL =	VSS	
		Ispn1	11	15	20	mA	FCSIN = TRRIN =	VSPN	
		Ifcs1	6	10	15	mA	SLDIN = REFIN,	VFCS	
		Isld1	—	—	1.0	mA	TRYF = TRYR = L All load open	VSLD	
		Iss2	20	33	60	mA	CE = H, VCTL =	VSS	
		Ispn2	11	30	50	mA	FCSIN = TRRIN =	VSPN	
		Ifcs2	7	10	15	mA	SLDIN = 5 V,	VFCS	
		Isld2	−15	−1.0	1.0	mA	TRYF, TRYR = H, L, All load open	VSLD	
Logic input	Input current	Iince	0	70	100	μA	Vin = 0 to 5 V	BRKSEL,	
		Iin	—	—	±10	μA		CE, TRYF,	
	Low level voltage	Vil	—	—	0.8	V		TRYR	
	High level voltage	Vih	2.0	—	—	V			
Logic output	Low level voltage	Vol	—	—	0.4	V	Io = 1 mA	PHASE	
	Leak current	Icer1	—	—	±10	μA	Vce = 15 V		
SPN driver	Output saturation voltage	Vsatspn	—	1.25	1.75	V	Iospn = 1.0 A	U, V, W	1
	Leak current	Icer2	1.3	2.2	3	mA	Vce = 15 V		
	Current limiter voltage	Vspncl	238	265	292	mV	Rnf = 0.25 Ω	RNF	2
FCS driver	Input resistance	Rinfcs	9.6	12	14.4	kΩ		FCSIN	
		Rinfcsref	9.6	12	14.4	kΩ			
	Input voltage range	Vinfcs	0	—	5	V			

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Electrical Characteristics
(Ta = 25°C, Vss = 5 V, Vspn = 12 V, Vfcs = 5 V, Vsld = 12 V) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
FCS driver	Output quiescent voltage	Vqfcs	2.375	2.5	2.625	V	FCSIN=FCSREF= 2.5 V, VFCS=5 V	FCSP, FCSN	3
	Output offset voltage	Vosfcs	—	—	±20	mV			
	Output saturation voltage	Vsatfcs	—	1.0	1.4	V	Io = 0.33 A		1
	Voltage gain	Gvfcs	11.6	12.6	13.6	dB			4
	Gain band width	Bfcs	100	—	—	kHz	ΔGv = −3 dB		
TRR driver	Input resistance	Rintrr	9.6	12	14.4	kΩ		TRRIN	
		Rintrrref	9.6	12	14.4	kΩ			
	Input voltage range	Vintrr	0	—	5	V			
	Output quiescent voltage	Vqtrr	2.375	2.5	2.625	V	FCSIN=TRRREF= 2.5 V, VFCS=5 V	TRRP, TRRN	3
	Output offset voltage	Vostrr	—	—	±20	mV	FCSIN = REF		
	Output saturation voltage	Vsattrr	—	1.0	1.4	V	Io = 0.33 A		1
	Voltage gain	Gvtrr	11.6	12.6	13.6	dB			4
	Gain band width	Btrr	100	—	—	kHz	ΔGv = −3 dB		
SLD driver	Output saturation voltage	Vsatsld	—	1.5	2.0	V	Iosld = 0.75 A	SLDP, SLDN	1
	Leak current	Icer3	—	—	±100	μA	Vce = 15 V		
	Penetration current	Iovlap	—	—	100	mA		VSLD	8
	Transient response	tplh1	—	—	5	μs		SLDP,	
	time	tphl1	—	—	5	μs		SLDN	
TRY driver	Output saturation voltage	Vsattry	—	1.0	1.4	V	Iotry = 0.33 A	TRYP, TRYN	1
	Leak current	Icer3	—	—	±100	μA	Vce = 15 V		
	Penetration current	Iovlap	—	—	100	mA		VSLD	8
	Transient response	tplh1	—	—	5	μs		TRYP,	
	time	tphl1	—	—	5	μs		TRYN	
	Input current	Iintrylim	—	—	±5	μA	Vtrylim=7 to VSLD		
	Output voltage	Vlimtry	0.1	0.7	1.0	V	R_L = 16Ω, Vtrylim = 7 V		9

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Electrical Characteristics

(Ta = 25°C, Vss = 5 V, Vspn = 12 V, Vfcs = 5 V, Vsld = 12 V) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
SPN current control	Input current	Iinspn	—	—	±5.0	µA	Vctl = 0 to Vss–1V	VCTL, REFIN	2
	REF voltage range	Vref	1.6	—	3.0	V			
	Dead zone voltage	Vdzspn	±50	—	±120	mV	Vref reference		
	Current control gain	Gctl	—	–12	±1.5	dB		RNF	
Drive mode	Change threshold voltage	Vctl	—	0.5	±0.1	V	Vref reference	VCTL	5
		f_{PHASE}	—	$\geq f_{CT2}$	±50%	Hz	SOFT SW mode	U, V, W	5
	SW ↔ SOFT SW		—	$<f_{CT2}$	–20%	Hz	SW mode		
B-EMF detection	Output resistance	Rflt	—	10	±20%	kΩ		UFIL, VFIL, WFIL	
	Threshold voltage of PHASE occurrence	Viemf	—	40	±50%	mVpp	VSPN ≥ Vss + 3V$_F$	U, V, W	6
			—	28	±50%	mVpp	VSPN ≤ Vss + 3V$_F$		
CLK OSC	RT voltage	Vrt	3.135	3.30	3.465	V		RT	
	CLK oscillation frequency	fclk	210	240	270	kHz	Rt = 10 kΩ, Ct1 = 82 pF	CT1	
Start-up circuit	Start-up oscillation frequency	fct2	437	485	534	Hz	Rt = 10 kΩ, Ct2 = 0.033 µF	CT2	
SLD control	Input current	Iinsld	—	—	±5.0	µA	Vsld = 0 to Vss–1V	SLDIN	
	Input voltage range	Vinsld	0	—	4.0	V			
	Limiter input current	Isldlim	—	—	±5.0	µA		SLDLIM	
	PWM oscillation frequency	fpwm	33	38	42.35	kHz	Rt = 10 kΩ, Ct3 = 470 pF		
	Control gain	D/V	80	90	100	%/V			7
	Offset voltage	Vossld	—	—	20	mV	SLDIN = REFIN		
Voltage regulator	Output sink current	Isinkreg	8.5	12.2	—	mA	VREGS = 4 V, VREGF = 4 V		
	Output voltage	Voutreg	3.135	3.30	3.465	V			
OTSD	Operating temperature	Tsd	135	160	—	°C			8
	Hysteresis	Thys	—	50	—	°C			

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Note: 1. The output saturation voltage is the sum of the upper and lower saturation voltages.

2. See figure 1. Where,

$$Gctl = 20 \log \frac{\Delta Vrnf}{\Delta Vctl}$$
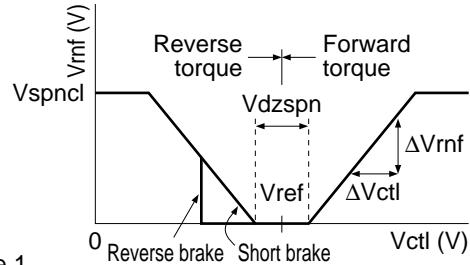
Figure 1

3. Where,

$$Vqfcs = \frac{Vfcsp + Vfcsn}{2}$$

$$Vqtrr = \frac{Vtrrp + Vtrrn}{2}$$

4. See figure 2. Where,

$$Gvfcs = 20 \log \left(\frac{\Delta Vfcsp}{\Delta Vfcsin} \quad \frac{\Delta Vfcsn}{\Delta Vfcsin} \right)$$

$$Gvtrr = 20 \log \left(\frac{\Delta Vtrrp}{\Delta Vtrrin} \quad \frac{\Delta Vtrrn}{\Delta Vtrrin} \right)$$
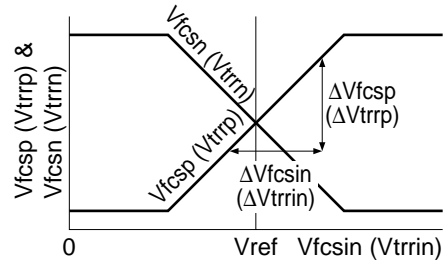
Figure 2

5. The circuit operates in soft switching drive mode only when the control input (Vctl) is lower than f_{CT2} and f_{PHASE} is higher than the threshold voltage. See figure 3.
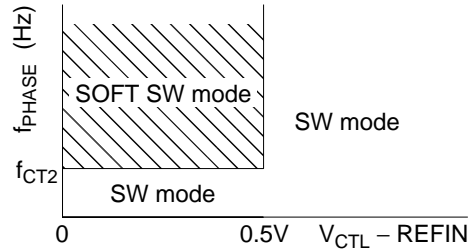
Figure 3

6. PHASE is output only when B-EMF exceeds the threshold voltage.

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7. See figure 4. Where,

$$D/V = \frac{\Delta D}{\Delta Vin}$$
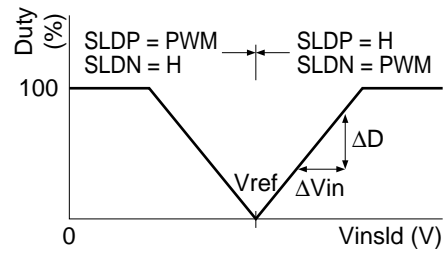
Figure 4

8. Design guide only.
9. Vlimtry = VTRYP – VTRYLIM, or VTRYN – VTRYLIM

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Reference Data

SPN Driver Output Saturation Voltage vs. Output Current

FCS Driver Output Saturation Voltage vs. Output Current

SLD Driver Output Saturation Voltage vs. Output Current

TRR Driver Output Saturation Voltage vs. Output Current

TRY Driver Output Saturation Voltage vs. Output Current

RT Voltage vs. Junction Temperature

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Package Dimensions

Preliminary   Unit: mm

14.0
14.2 Max

56   29

Top view

6.10

1   28

0.50

0.21 +0.04 −0.05
0.19 +0.03 −0.05

⊕ 0.08 (M)

0.65 Max

1.20 Max

△ 0.08

8.10 ± 0.15

0° − 8°

0.17 ± 0.05
0.15 ± 0.04
0.05 ± 0.05

1.0

0.50 ± 0.1

(7.5)

1   28

Under view

(2.8)

56   29

Hitachi Code	TTP-56DT
JEDEC	—
EIAJ	—
Weight (reference value)	0.32 g

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