Data Sheet | February 1999 | File Number 3682.4

Dual, 420MHz, Low Power, Video, Current Feedback Operational Amplifier with Disable

The HFA1245 is a dual, high speed, low power current feedback amplifier built with Intersil's proprietary complementary bipolar UHF-1 process.

The HFA1245 features individual TTL/CMOS compatible disable controls. When pulled low they disable the corresponding amplifier, which reduces the supply current and forces the output into a high impedance state. This feature allows easy implementation of simple, low power video switching and routing systems. Component and composite video systems also benefit from this op amp's excellent gain flatness, and good differential gain and phase specifications.

Multiplexed A/D applications will also find the HFA1245 useful as the A/D driver/multiplexer.

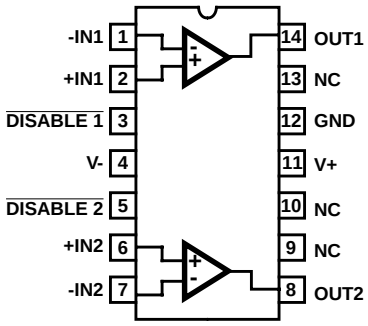
The HFA1245 is a low power, high performance upgrade for the popular Intersil HA5022. For a dual amplifier without disable, in a standard 8 lead pinout, please see the HFA1205 data sheet.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HFA1245IP	-40 to 85	14 Ld PDIP	E14.3
HA5022EVAL	High Speed Op Amp DIP Evaluation Board		

Pinout

HFA1245
(PDIP)
TOP VIEW



Features

- Low Supply Current . . . . . 5.8mA/Op Amp
- High Input Impedance 2MΩ
- Low Crosstalk (5MHz) . . . . . -83dB
- High Off Isolation (5MHz) 65dB
- Wide -3dB Bandwidth (A_V = +2) 420MHz
- Very Fast Slew Rate 1200V/µs
- Gain Flatness (to 50MHz) . . . . . ±0.11dB
- Differential Gain 0.02%
- Differential Phase . . . . . 0.03 Degrees
- Individual Output Enable/Disable
- Output Enable/Disable Time 150ns/30ns
- Pin Compatible Upgrade to HA5022

Applications

- Flash A/D Drivers
- High Resolution Monitors
- Video Multiplexers
- Video Switching and Routing
- Professional Video Processing
- Video Digitizing Boards/Systems
- Multimedia Systems
- RGB Preamps
- Medical Imaging
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications
- High Speed Oscilloscopes and Analyzers

Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage . . . . . V_{SUPPLY}
Differential Input Voltage 8V
Output Current (Note 2) . . . . . Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 600V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)
PDIP Package	100

Maximum Junction Temperature (Die) . . . . . 175^{o}C
Maximum Junction Temperature (Plastic Package) . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C

Operating Conditions

Temperature Range . . . . . -40^{o}C to 85^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.

Electrical Specifications

V_{SUPPLY} = ±5V, A_V = +1, R_F = 560Ω, R_S = 650Ω, R_L = 100Ω, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (^{o}C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	25	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	µV/^{o}C
Input Offset Voltage Common-Mode Rejection Ratio	ΔV_{CM} = ±1.8V	A	25	45	48	-	dB
	ΔV_{CM} = ±1.8V	A	85	43	46	-	dB
	ΔV_{CM} = ±1.2V	A	-40	43	46	-	dB
Input Offset Voltage Power Supply Rejection Ratio	ΔV_{PS} = ±1.8V	A	25	48	52	-	dB
	ΔV_{PS} = ±1.8V	A	85	46	50	-	dB
	ΔV_{PS} = ±1.2V	A	-40	46	50	-	dB
Non-Inverting Input Bias Current		A	25	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	nA/^{o}C
Non-Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.8V	A	25	-	0.5	1	µA/V
	ΔV_{PS} = ±1.8V	A	85	-	0.8	3	µA/V
	ΔV_{PS} = ±1.2V	A	-40	-	0.8	3	µA/V
Non-Inverting Input Resistance	ΔV_{CM} = ±1.8V	A	25	0.8	2	-	MΩ
	ΔV_{CM} = ±1.8V	A	85	0.5	1.3	-	MΩ
	ΔV_{CM} = ±1.2V	A	-40	0.5	1.3	-	MΩ
Inverting Input Bias Current		A	25	-	2	7.5	µA
		A	Full	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	nA/^{o}C
Inverting Input Bias Current Common-Mode Sensitivity	ΔV_{CM} = ±1.8V	A	25	-	3	6	µA/V
	ΔV_{CM} = ±1.8V	A	85	-	4	8	µA/V
	ΔV_{CM} = ±1.2V	A	-40	-	4	8	µA/V
Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.8V	A	25	-	2	5	µA/V
	ΔV_{PS} = ±1.8V	A	85	-	4	8	µA/V
	ΔV_{PS} = ±1.2V	A	-40	-	4	8	µA/V

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 560Ω, R_S = 650Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Inverting Input Resistance		B	25	-	56	-	Ω
Input Capacitance		B	25	-	2.0	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS Tests)		A	25, 85	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	V
Input Noise Voltage Density (Note 6)	f = 100kHz	B	25	-	3.5	-	nV/√Hz
Non-Inverting Input Noise Current Density (Note 6)	f = 100kHz	B	25	-	2.5	-	pA/√Hz
Inverting Input Noise Current Density (Note 6)	f = 100kHz	B	25	-	30	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain (Note 6)		B	25	-	500	-	kΩ
AC CHARACTERISTICS							
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, Note 6)	A_V = +1, $+R_S$ = 650Ω	B	25	-	260	-	MHz
	A_V = +2, R_F = 750Ω	B	25	-	420	-	MHz
	A_V = -1, R_F = 475Ω	B	25	-	280	-	MHz
Full Power Bandwidth (V_{OUT} = 5V_{P-P} at A_V = +2/-1, 4V_{P-P} at A_V = +1, Note 6)	A_V = +1, $+R_S$ = 650Ω	B	25	-	150	-	MHz
	A_V = +2, R_F = 750Ω	B	25	-	115	-	MHz
	A_V = -1, R_F = 475Ω	B	25	-	160	-	MHz
Gain Flatness (A_V = +2, R_F = 750Ω, V_{OUT} = 0.2V_{P-P}, Note 6)	To 25MHz	B	25	-	±0.04	-	dB
	To 50MHz	B	25	-	±0.11	-	dB
Minimum Stable Gain		A	Full	-	1	-	V/V
Crosstalk (A_V = +2, R_F = 750Ω, V_{OUT} = 1V_{P-P}, Notes 4, 6)	5MHz	B	25	-	-83	-	dB
	10MHz	B	25	-	-77	-	dB
OUTPUT CHARACTERISTICS A_V = +2, R_F = 750Ω, Unless Otherwise Specified							
Output Voltage Swing (Note 6)	A_V = -1, R_L = 100Ω	A	25	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V
Output Current (Note 6)	A_V = -1, R_L = 50Ω	A	25, 85	50	60	-	mA
		A	-40	28	42	-	mA
Output Short Circuit Current		B	25	-	90	-	mA
Closed Loop Output Resistance (Note 6)	DC	B	25	-	0.07	-	Ω
Second Harmonic Distortion (V_{OUT} = 2V_{P-P})	10MHz	B	25	-	-50	-	dBc
	20MHz	B	25	-	-45	-	dBc
Third Harmonic Distortion (V_{OUT} = 2V_{P-P})	10MHz	B	25	-	-57	-	dBc
	20MHz	B	25	-	-50	-	dBc
3rd Order Intercept (Note 6)	20MHz	B	25	-	23	-	dBm
Reverse Isolation (S_{12}, Note 6)	65MHz	B	25	-	60	-	dB
TRANSIENT CHARACTERISTICS A_V = +2, R_F = 750Ω, Unless Otherwise Specified							
Rise and Fall Times (V_{OUT} = 0.5V_{P-P})	Rise Time	B	25	-	0.9	-	ns
	Fall Time	B	25	-	1.5	-	ns
Overshoot (V_{OUT} = 0.5V_{P-P}, V_{IN} t_{RISE} = 1ns, Note 5)	+OS	B	25	-	5	-	%
	-OS	B	25	-	10	-	%
Slew Rate (V_{OUT} = 4V_{P-P}, A_V = +1, R_F = 560Ω, $+R_S$ = 650Ω)	+SR	B	25	-	1150	-	V/µs
	-SR (Note 7)	B	25	-	800	-	V/µs

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 560Ω, R_S = 650Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = +2)	+SR	B	25	-	1400	-	V/µs
	-SR (Note 7)	B	25	-	800	-	V/µs
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = -1, R_F = 475Ω)	+SR	B	25	-	2200	-	V/µs
	-SR (Note 7)	B	25	-	1200	-	V/µs
Settling Time (V_{OUT} = +2V to 0V step, Note 6)	To 0.1%	B	25	-	15	-	ns
	To 0.05%	B	25	-	20	-	ns
	To 0.02%	B	25	-	40	-	ns
Overdrive Recovery Time	V_{IN} = ±2V	B	25	-	8.5	-	ns
VIDEO CHARACTERISTICS A_V = +2, R_F = 750Ω, Unless Otherwise Specified							
Differential Gain (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.02	-	%
	R_L = 75Ω	B	25	-	0.03	-	%
Differential Phase (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.03	-	Degrees
	R_L = 75Ω	B	25	-	0.05	-	Degrees
DISABLE CHARACTERISTICS							
Disabled Supply Current	$V_{\overline{DISABLE}}$ = 0V	A	Full	-	3	4	mA/Op Amp
$\overline{DISABLE}$ Input Logic Voltage	Low	A	Full	-	-	0.8	V
	High	A	25, 85	2.0	-	-	V
		A	-40	2.4	-	-	V
$\overline{DISABLE}$ Input Logic Low Current	$V_{\overline{DISABLE}}$ = 0V	A	Full	-	100	200	µA
$\overline{DISABLE}$ Input Logic High Current	$V_{\overline{DISABLE}}$ = 5V	A	Full	-	1	15	µA
Output Disable Time (Note 6)	V_{OUT} = ±1V, $V_{\overline{DISABLE}}$ = 2.4V to 0.4V	B	25	-	30	-	ns
Output Enable Time (Note 6)	V_{OUT} = ±1V, $V_{\overline{DISABLE}}$ = 0.4V to 2.4V	B	25	-	150	-	ns
Disabled Output Capacitance	$V_{\overline{DISABLE}}$ = 0V	B	25	-	4.5	-	pF
Disabled Output Leakage (Note 6)	$V_{\overline{DISABLE}}$ = 0V, V_{IN} = +2V, V_{OUT} = ±3V	A	Full	-	2	10	µA
All Hostile Off Isolation ($V_{DISABLE}$ = 0V, V_{IN} = 1V_{P-P}, A_V = +2, Note 6)	At 5MHz	B	25	-	65	-	dB
	At 10MHz	B	25	-	60	-	dB
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	25	±4.5	-	±5.5	V
Power Supply Current (Note 6)		A	25	5.6	5.8	6.1	mA/Op Amp
		A	Full	5.4	5.9	6.3	mA/Op Amp

NOTES:

3. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
4. The typical use for these amplifiers is in multiplexed configurations, where one amplifier (hostile channel) is enabled, and the passive channel is disabled. The crosstalk data specified is tested in this manner, with the input signal applied to the hostile channel, while monitoring the output of the passive channel. Crosstalk performance with both the hostile and passive channels enabled is typically -63dB at 5MHz, and -58dB at 10MHz.
5. Undershoot dominates for output signal swings below GND (e.g., 0.5V_{P-P}), yielding a higher overshoot limit compared to the V_{OUT} = 0V to 0.5V condition. See the “Application Information“ section for details.
6. See Typical Performance Curves for more information.
7. Slew rates are asymmetrical if the output swings below GND (e.g., a bipolar signal). Positive unipolar output signals have symmetric positive and negative slew rates comparable to the +SR specification. See the “Application Information” section, and the pulse response graphs for details.

Application Information

Relevant Application Notes

The following Application Notes pertain to the HFA1245:

- AN9787-An Intuitive Approach to Understanding Current Feedback Amplifiers
- AN9420-Current Feedback Amplifier Theory and Applications
- AN9663-Converting from Voltage Feedback to Current Feedback Amplifiers

These publications may be obtained from Intersil's web site (http://www.intersil.com) or via our AnswerFAX system.

Optimum Feedback Resistor

Although a current feedback amplifier's bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1245 design is optimized for a 750Ω R_F at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback will cause the same problems due to the feedback impedance decrease at higher frequencies). At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth. For good channel-to-channel gain matching, it is recommended that all resistors (termination as well as gain setting) be ±1% tolerance or better. Note that a series input resistor, on +IN, is required for a gain of +1, to reduce gain peaking and increase stability.

TABLE 1. OPTIMUM FEEDBACK RESISTOR

GAIN (A_V)	R_F (Ω)	BANDWIDTH (MHz)
-1	475	280
+1	560 (+R_S = 650Ω)	260
+2	750	420
+5	200	270
+10	180	140

Channel-To-Channel Frequency Response Matching

The frequency response of channel 1 and channel 2 aren't perfectly matched. For the best channel-to-channel frequency response match in a gain of 2 (see Figure 1), use R_F = 650Ω for channel 1 and R_F = 806Ω for channel 2.

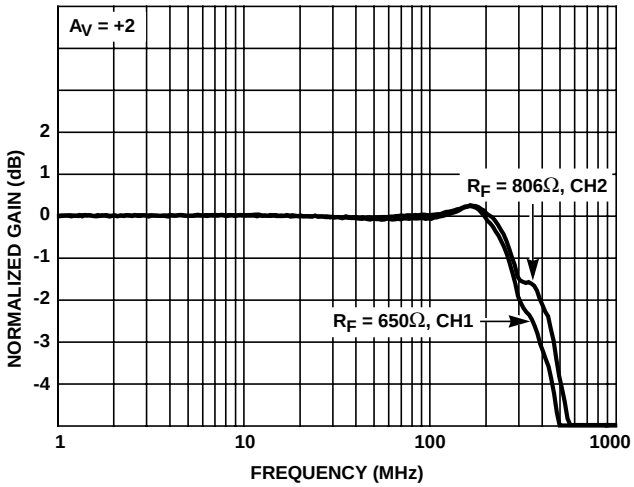


FIGURE 1. CHANNEL 1 AND CHANNEL 2 MATCHED FREQUENCY RESPONSE

Non-inverting Input Source Impedance

For best operation, the DC source impedance seen by the non-inverting input should be ≥50Ω. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

Pulse Undershoot and Asymmetrical Slew Rates

The HFA1245 utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pulldown transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased undershoot on the negative portion of the output waveform (see Figures 7, 11, 15, and 19). This undershoot isn't present for small bipolar signals, or large positive signals. Another artifact of the composite device is asymmetrical slew rates for output signals with a negative voltage component. The slew rate degrades as the output signal crosses through 0V (see Figures 7, 11, 15, and 19), resulting in a slower overall negative slew rate. Positive only signals have symmetrical slew rates as illustrated in the large signal positive pulse response graphs (see Figures 5, 9, 13, and 17).

$\overline{\text{DISABLE}}$ Input TTL Compatibility

The HFA1245 derives an internal GND reference for the digital circuitry as long as the power supplies are symmetrical about GND. With symmetrical supplies the digital switching threshold ($V_{TH} = (V_{IH} + V_{IL})/2 = (2.0 + 0.8)/2$) is 1.4V, which ensures the TTL compatibility of the $\overline{\text{DISABLE}}$ input. If asymmetrical supplies (e.g., +10V, 0V) are utilized, the switching threshold becomes:

$$V_{TH} = \frac{V+ + V-}{2} + 1.4V,$$

and the V_{IH} and V_{IL} levels will be V_{TH} ±0.6V, respectively.

Optional GND Pin for TTL Compatibility

Pin 12 is an optional GND reference used to ensure the TTL compatibility of the $\overline{\text{DISABLE}}$ inputs. With symmetrical supplies the GND pin may be unconnected, or connected directly to GND. If asymmetrical supplies (e.g., +10V, 0V) are utilized, and TTL compatibility is desired, the GND pin must be connected to GND. With an external GND, the $\overline{\text{DISABLE}}$ input is TTL compatible regardless of supply voltage utilized.

PC Board Layout

The HFA1245's frequency response depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground at the amplifier's inverting input (-IN), as this capacitance causes gain peaking, pulse overshoot, and if large enough, instability. To reduce this capacitance, the designer should remove the ground plane under traces connected to -IN, and keep connections to -IN as short as possible.

An example of a good high frequency layout is the HA5022 evaluation board discussed below.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 2 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 260MHz (for A_V = +1). By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth still decreases as the load capacitance increases. For example, at A_V = +1, R_S = 45Ω, C_L = 40pF, the overall bandwidth is 185MHz, but the bandwidth drops to 85MHz at A_V = +1, R_S = 9Ω, C_L = 330pF.

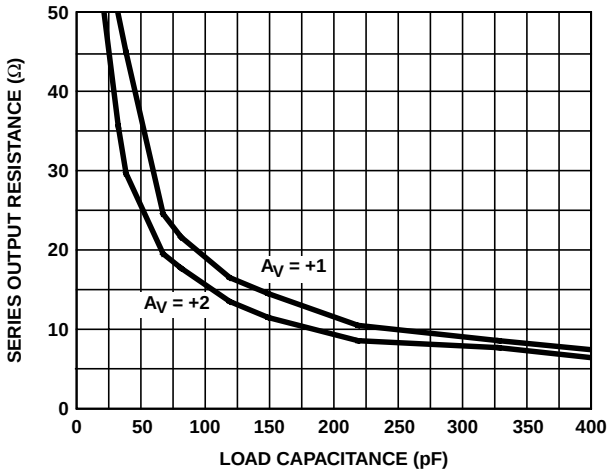


FIGURE 2. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Evaluation Board

Evaluate the HFA1245's performance using the HA5022 evaluation board (part number HA5022EVAL). Please contact your local sales office for ordering information. The feedback and gain setting resistors must be replaced with the appropriate value (see "Optimum Feedback Resistor" table) for the gain being evaluated. Also, replace the two 0Ω series output resistors (R_S) with 50Ω resistors.

The modified schematic of the board is shown in Figure 3.

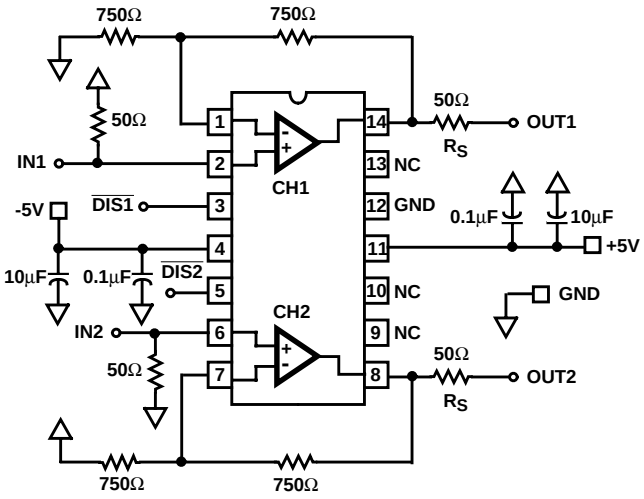


FIGURE 3. EVALUATION BOARD SCHEMATIC MODIFIED FOR A_V = +2

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified

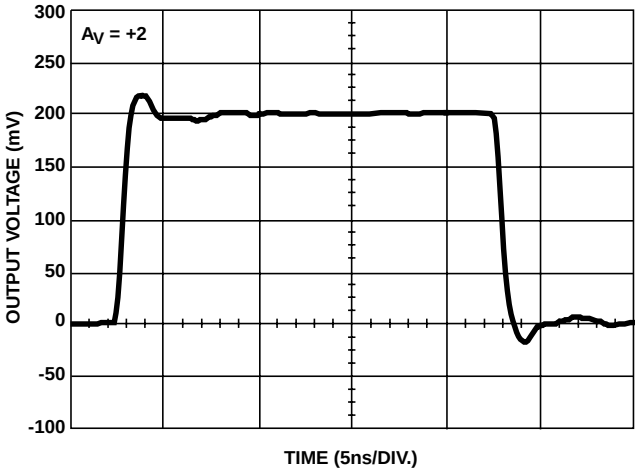


FIGURE 4. SMALL SIGNAL POSITIVE PULSE RESPONSE

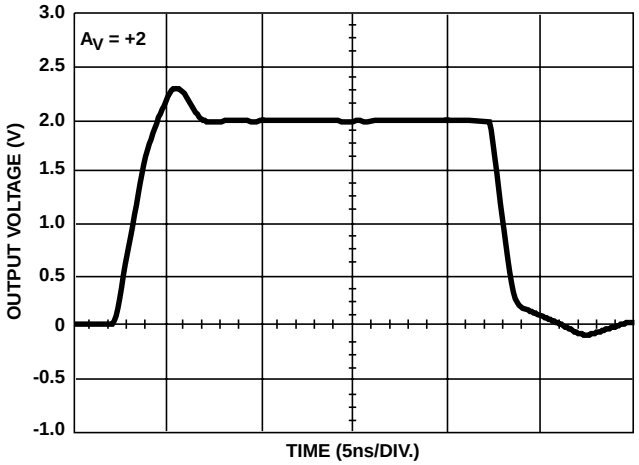


FIGURE 5. LARGE SIGNAL POSITIVE PULSE RESPONSE

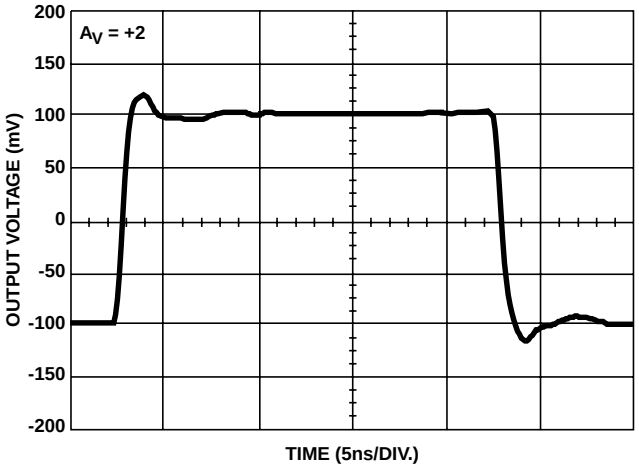


FIGURE 6. SMALL SIGNAL BIPOLAR PULSE RESPONSE

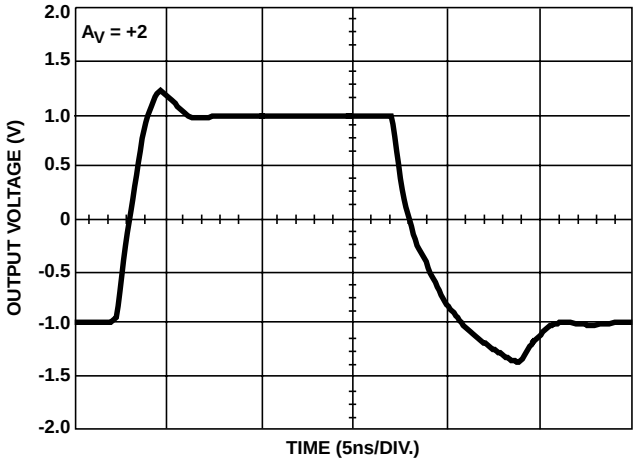


FIGURE 7. LARGE SIGNAL BIPOLAR PULSE RESPONSE

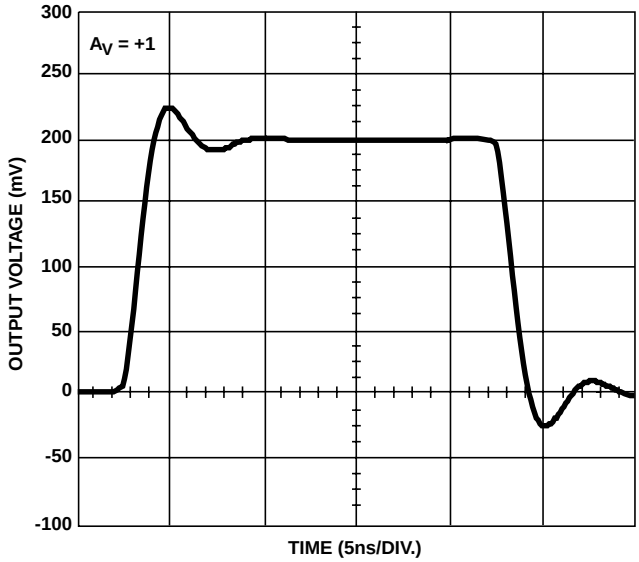


FIGURE 8. SMALL SIGNAL POSITIVE PULSE RESPONSE

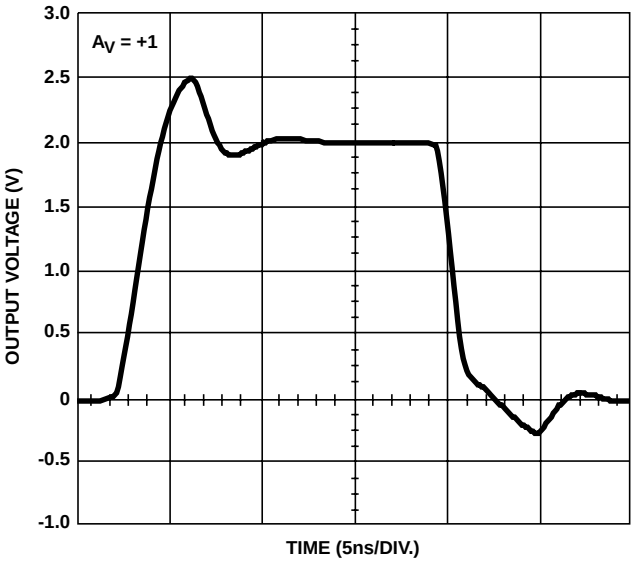


FIGURE 9. LARGE SIGNAL POSITIVE PULSE RESPONSE

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

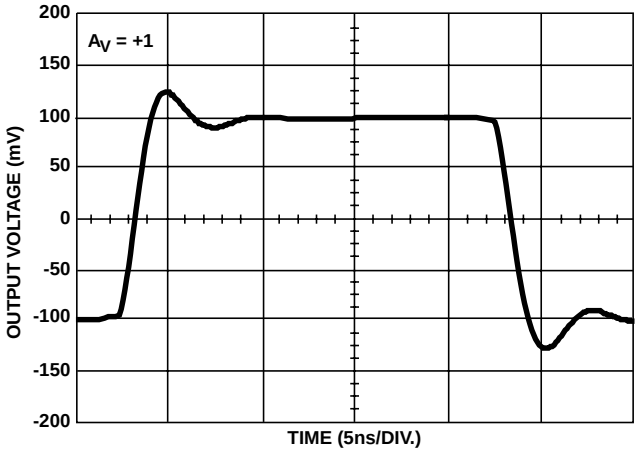


FIGURE 10. SMALL SIGNAL BIPOLAR PULSE RESPONSE

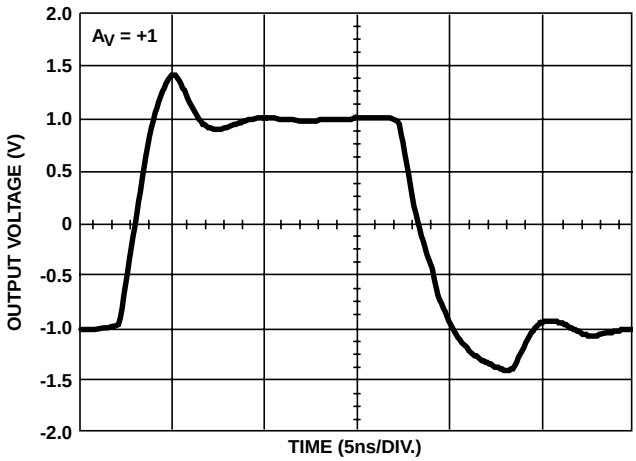


FIGURE 11. LARGE SIGNAL BIPOLAR PULSE RESPONSE

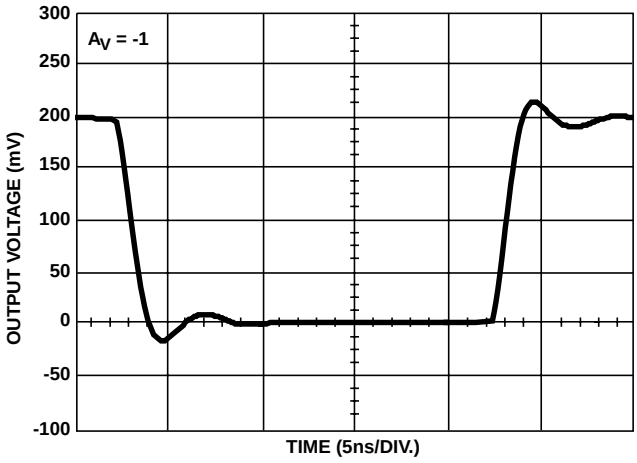


FIGURE 12. SMALL SIGNAL POSITIVE PULSE RESPONSE

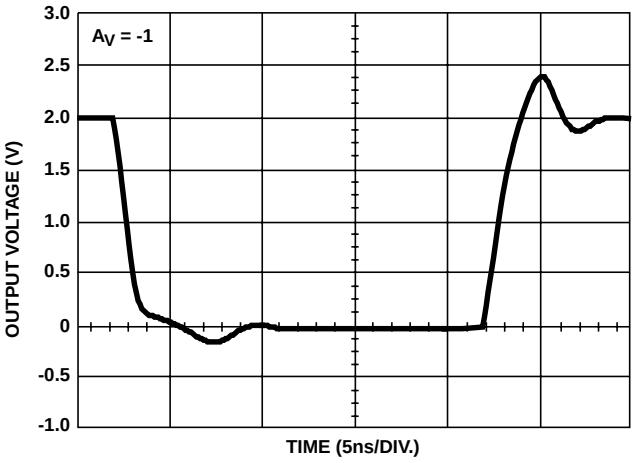


FIGURE 13. LARGE SIGNAL POSITIVE PULSE RESPONSE

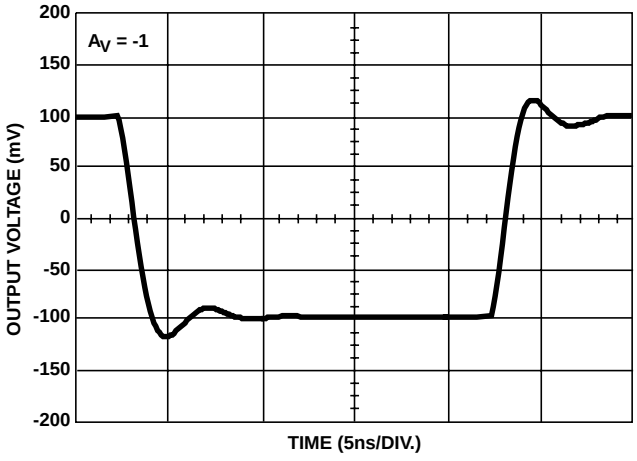


FIGURE 14. SMALL SIGNAL BIPOLAR PULSE RESPONSE

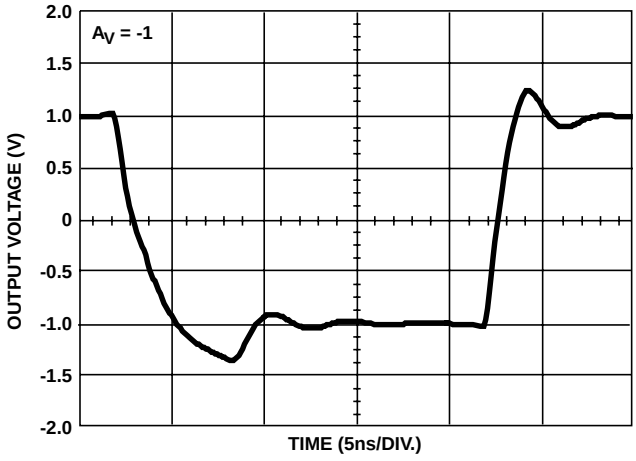


FIGURE 15. LARGE SIGNAL BIPOLAR PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^0C$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

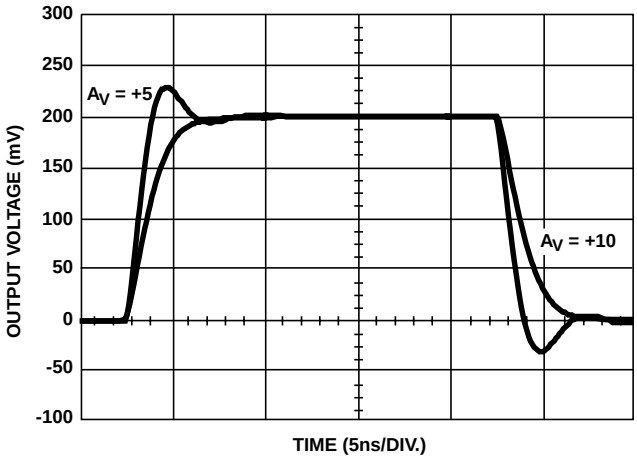


FIGURE 16. SMALL SIGNAL POSITIVE PULSE RESPONSE

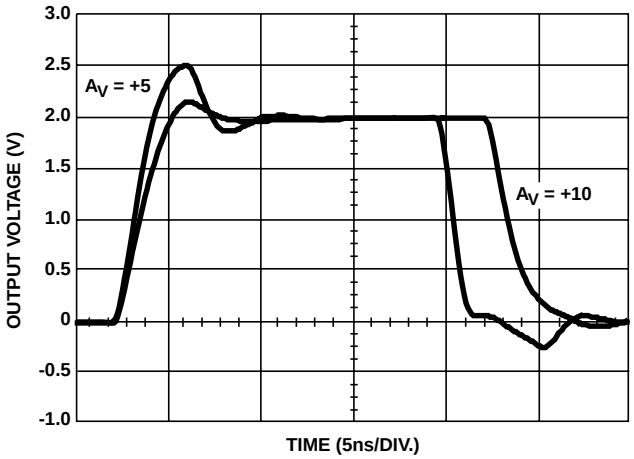


FIGURE 17. LARGE SIGNAL POSITIVE PULSE RESPONSE

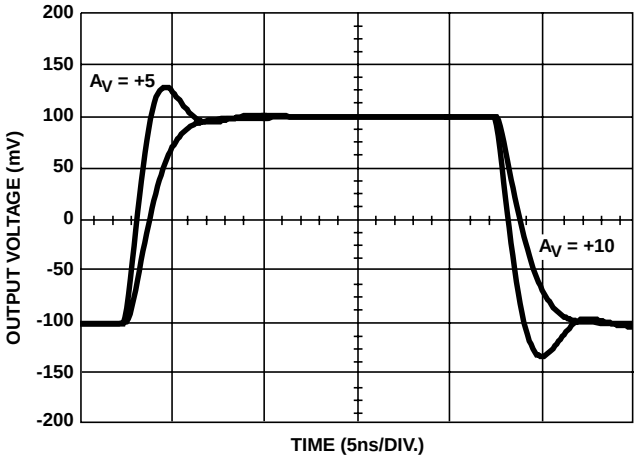


FIGURE 18. SMALL SIGNAL BIPOLAR PULSE RESPONSE

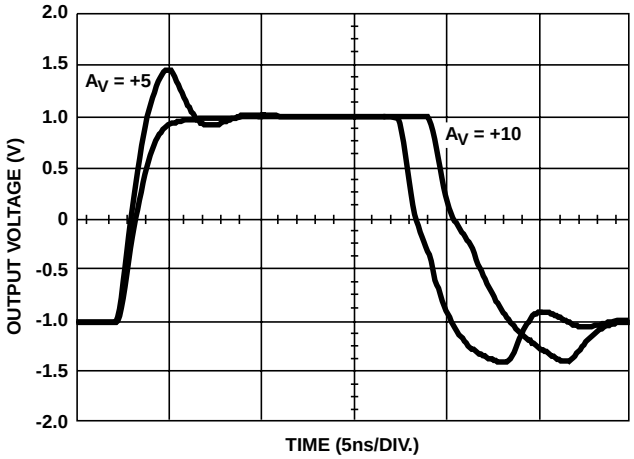


FIGURE 19. LARGE SIGNAL BIPOLAR PULSE RESPONSE

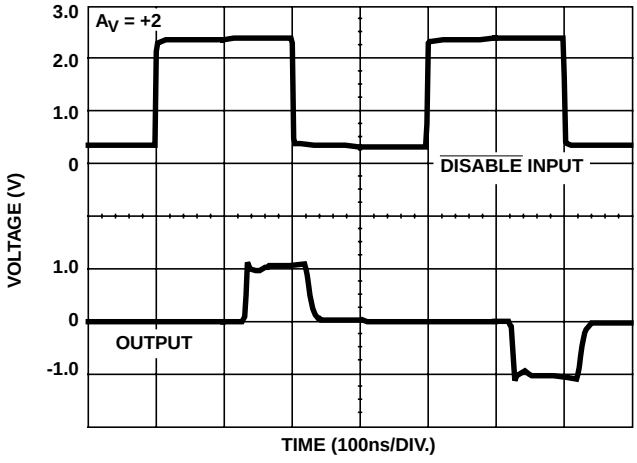


FIGURE 20. OUTPUT DISABLE / ENABLE RESPONSE

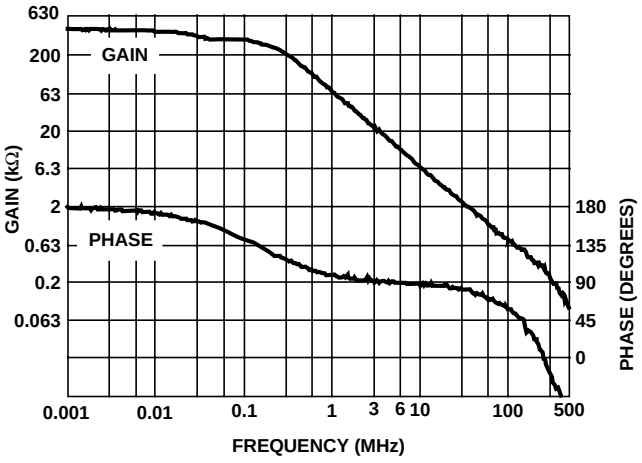


FIGURE 21. OPEN LOOP TRANSIMPEDANCE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^0C$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

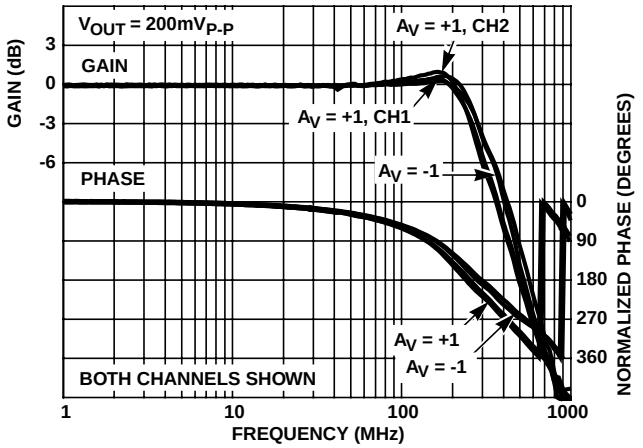


FIGURE 22. FREQUENCY RESPONSE

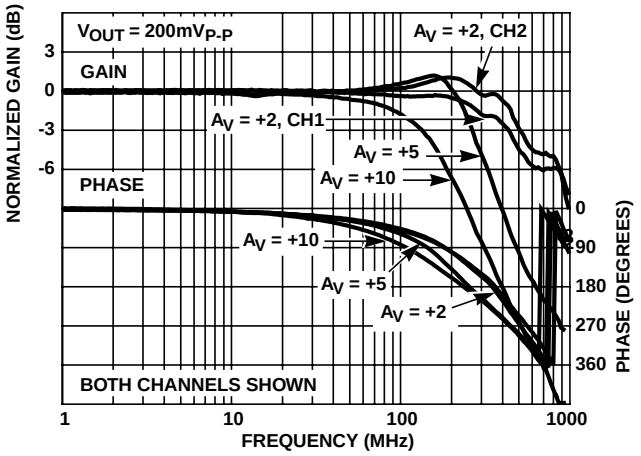


FIGURE 23. FREQUENCY RESPONSE

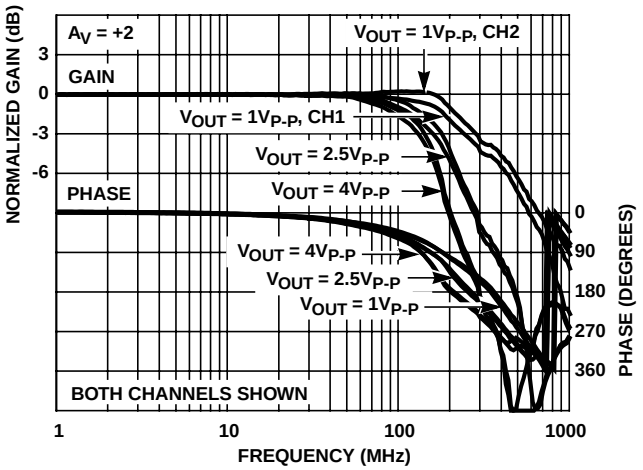


FIGURE 24. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

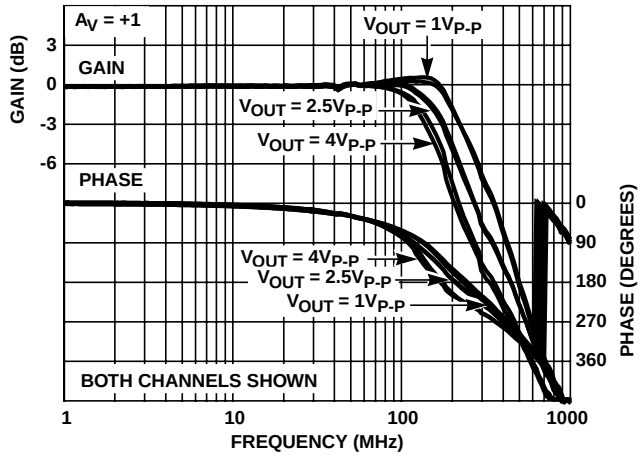


FIGURE 25. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

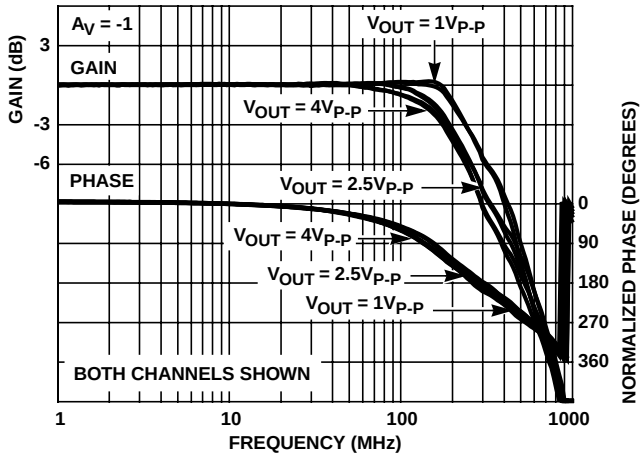


FIGURE 26. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

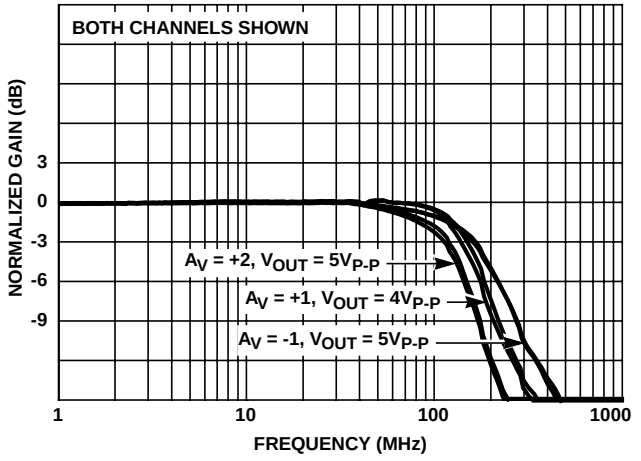


FIGURE 27. FULL POWER BANDWIDTH

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^0C$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

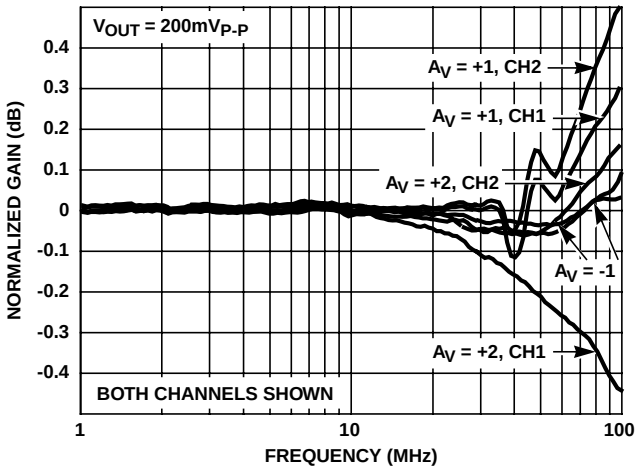


FIGURE 28. GAIN FLATNESS

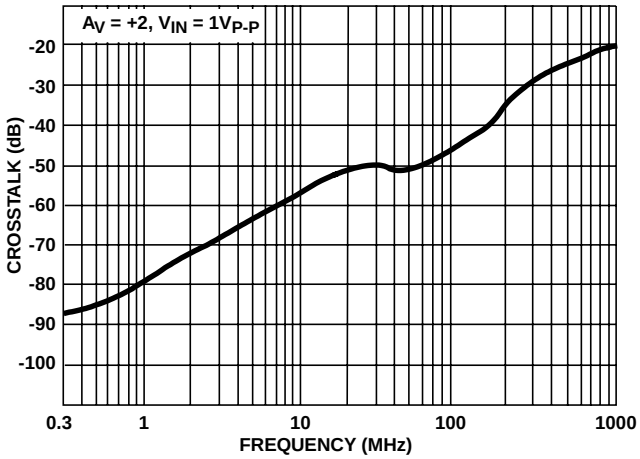


FIGURE 29. CROSSTALK (PASSIVE CHANNEL ENABLED)

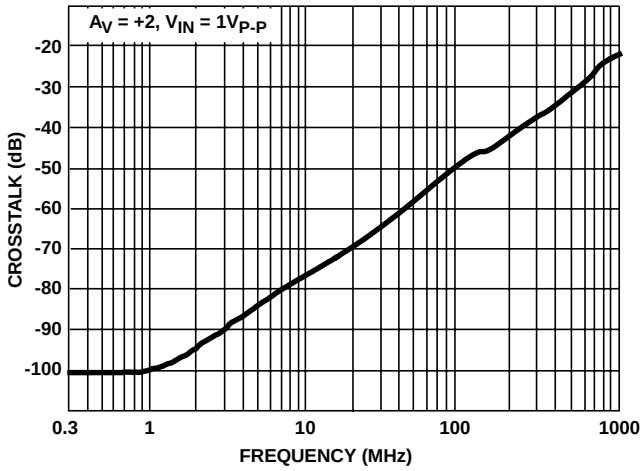


FIGURE 30. CROSSTALK (PASSIVE CHANNEL DISABLED)

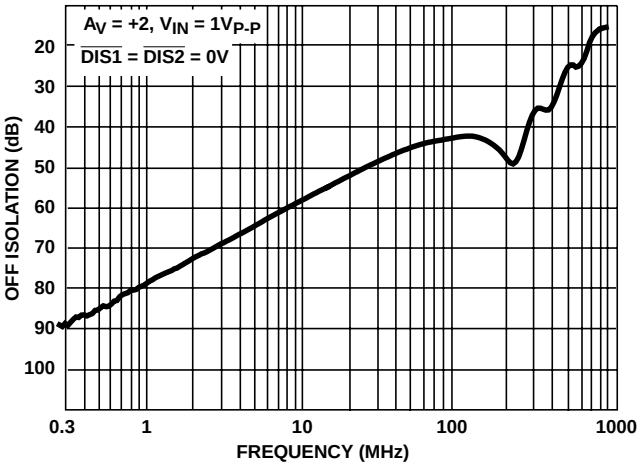


FIGURE 31. ALL HOSTILE OFF ISOLATION

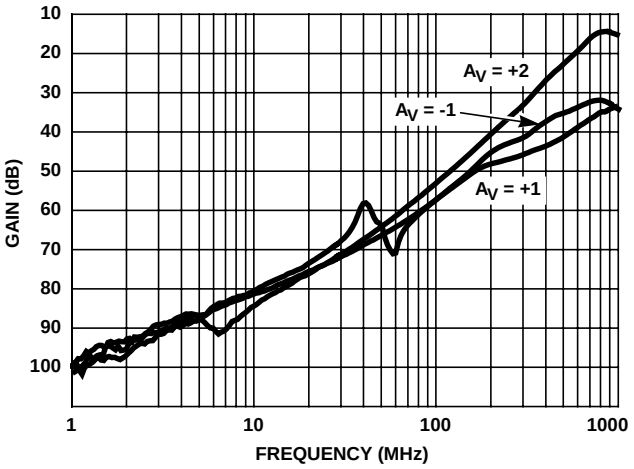


FIGURE 32. REVERSE ISOLATION

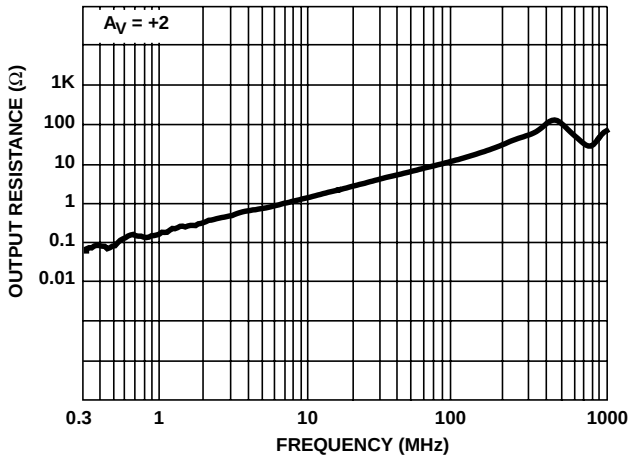


FIGURE 33. ENABLED OUTPUT RESISTANCE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

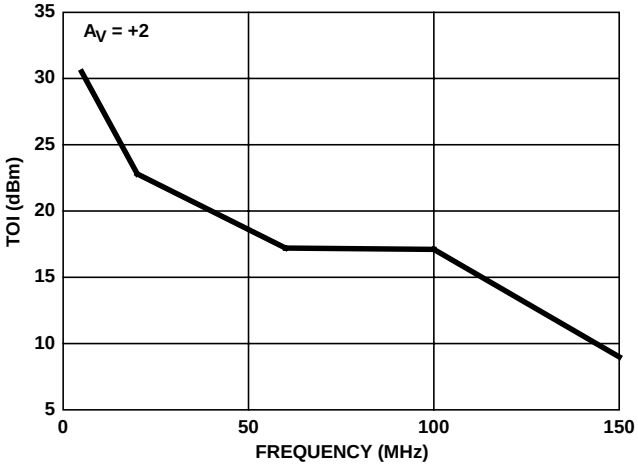


FIGURE 34. 3rd ORDER INTERCEPT vs FREQUENCY

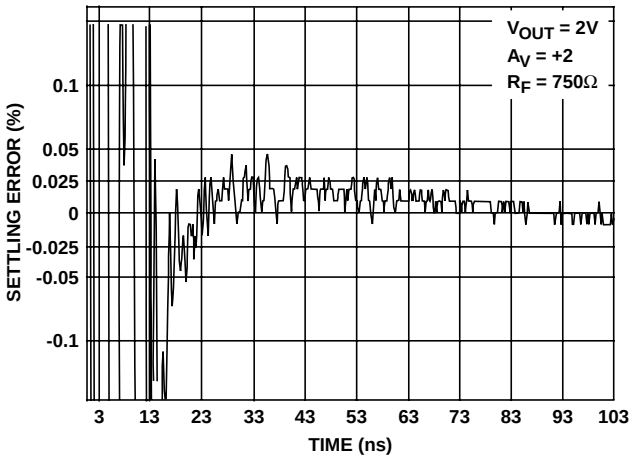


FIGURE 35. SETTLING TIME RESPONSE

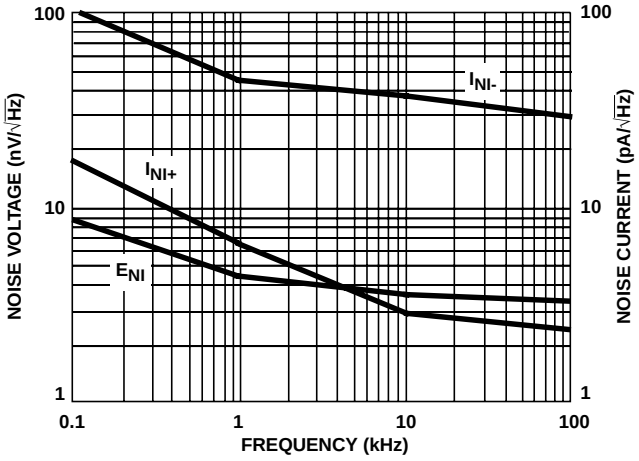


FIGURE 36. INPUT NOISE CHARACTERISTICS

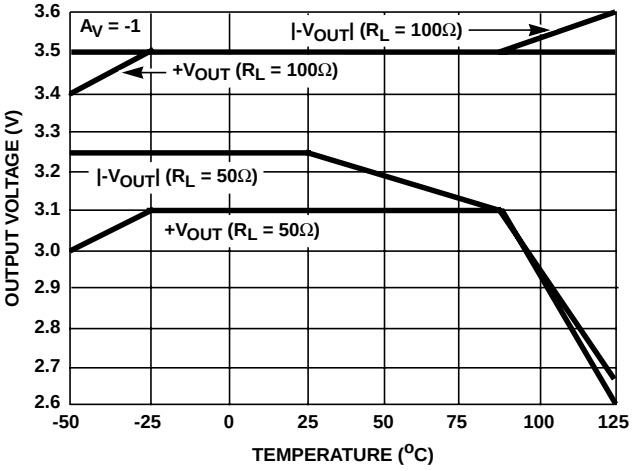


FIGURE 37. OUTPUT VOLTAGE vs TEMPERATURE

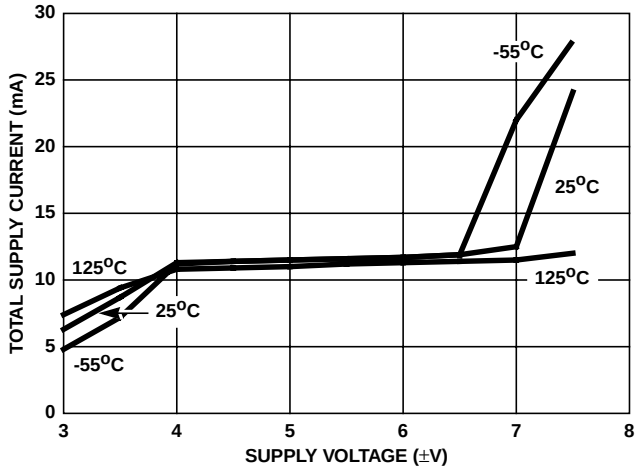


FIGURE 38. SUPPLY CURRENT vs SUPPLY VOLTAGE

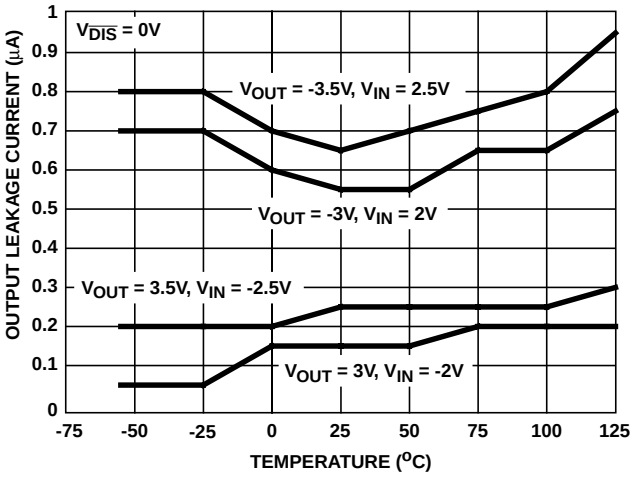


FIGURE 39. DISABLED OUTPUT LEAKAGE vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

69 mils x 92 mils x 19 mils
1750µm x 2330µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ
Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (POWERED UP):

Floating (Recommend Connection to V-)

PASSIVATION:

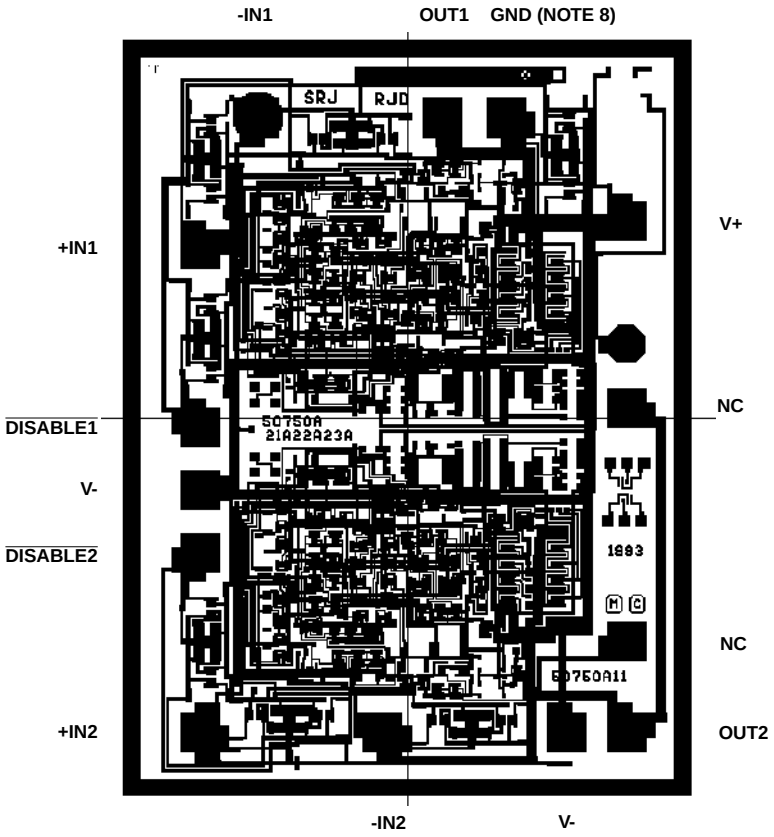
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

180

Metallization Mask Layout

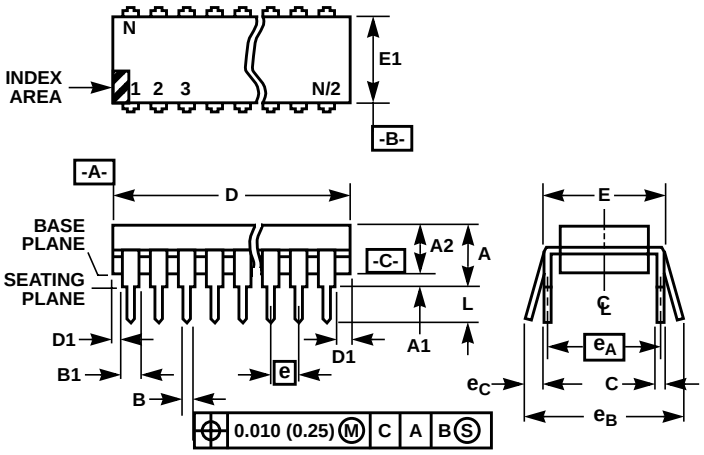
HFA1245



NOTE:

8. This is an optional GND pad. Users may set a GND reference, via this pad, to ensure the TTL compatibility of the $\overline{\text{DISABLE}}$ inputs when using asymmetrical supplies (e.g., V+ = 10V, V- = 0V). See the “Application Information” section for details.

Dual-In-Line Plastic Packages (PDIP)



E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

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