

Radiation Hardened, High Speed, Low Power Current Feedback Amplifier with Programmable Output Limiting

The HS-1135RH is a radiation hardened, high speed, low power current feedback amplifier built with Intersil's proprietary complementary bipolar UHF-1 (DI bonded wafer) process. They are QML approved and processed in full compliance with MIL-PRF-38535. This amplifier features user programmable output limiting, via the V_H and V_L pins.

The HS-1135RH is the ideal choice for high speed, low power applications requiring output limiting (e.g., flash A/D drivers), especially those requiring fast overdrive recovery times. The limiting function allows the designer to set the maximum and minimum output levels to protect downstream stages from damage or input saturation. The sub-nanosecond overdrive recovery time ensures a quick return to linear operation following an overdrive condition.

Component and composite video systems also benefit from this op amp's performance, as indicated by the gain flatness, and differential gain and phase specifications.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-96767. A "hot-link" is provided on our homepage for downloading.
<http://www.intersil.com/spacedefense/space.htm>

Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (°C)
5962F9676701VPA	HS7-1135RH-Q	-55 to 125
5962F9676701VPC	HS7B-1135RH-Q	-55 to 125
HS7-1135RH/PROTO	HS7-1135RH/PROTO	-55 to 125

Features

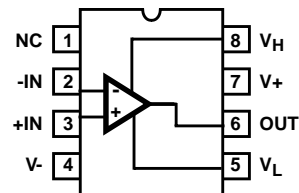
- Electrically Screened to SMD # 5962-96767
- QML Qualified per MIL-PRF-38535 Requirements
- User Programmable Output Voltage Limiting
- Fast Overdrive Recovery <1ns (Typ)
- Low Supply Current 6.9mA (Typ)
- Wide -3dB Bandwidth. 360MHz (Typ)
- High Slew Rate. 1200V/μs (Typ)
- High Input Impedance 2MΩ (Typ)
- Excellent Gain Flatness (to 50MHz). ±0.07dB (Typ)
- Total Gamma Dose. 300kRAD(Si)
- Latch Up None (DI Technology)

Applications

- Flash A/D Driver
- Video Switching and Routing
- Pulse and Video Amplifiers
- Wideband Amplifiers
- RF/IF Signal Processing
- Imaging Systems

Pinout

**HS-1135RH
 GDIP1-T8 (CERDIP)
 OR CDIP2-TI (SBDIP)
 TOP VIEW**



Clamp Operation

General

The HS-1135RH features user programmable output clamps to limit output voltage excursions. Clamping action is obtained by applying voltages to the V_H and V_L terminals (pins 8 and 5) of the amplifier. V_H sets the upper output limit, while V_L sets the lower clamp level. If the amplifier tries to drive the output above V_H , or below V_L , the clamp circuitry limits the output voltage at V_H or V_L (the clamp accuracy), respectively. The low input bias currents of the clamp pins allow them to be driven by simple resistive divider circuits, or active elements such as amplifiers or DACs.

Clamp Circuitry

Figure 1 shows a simplified schematic of the HS-1135RH input stage, and the high clamp (V_H) circuitry. As with all current feedback amplifiers, there is a unity gain buffer (Q_{X1} - Q_{X2}) between the positive and negative inputs. This buffer forces $-IN$ to track $+IN$, and sets up a slewing current of $(V_{IN} - V_{OUT})/R_F$. This current is mirrored onto the high impedance node (Z) by Q_{X3} - Q_{X4} , where it is converted to a voltage and fed to the output via another unity gain buffer. If no clamping is utilized, the high impedance node may swing within the limits defined by Q_{P4} and Q_{N4} . Note that when the output reaches its quiescent value, the current flowing through $-IN$ is reduced to only that small current ($-I_{BIAS}$) required to keep the output at the final voltage.

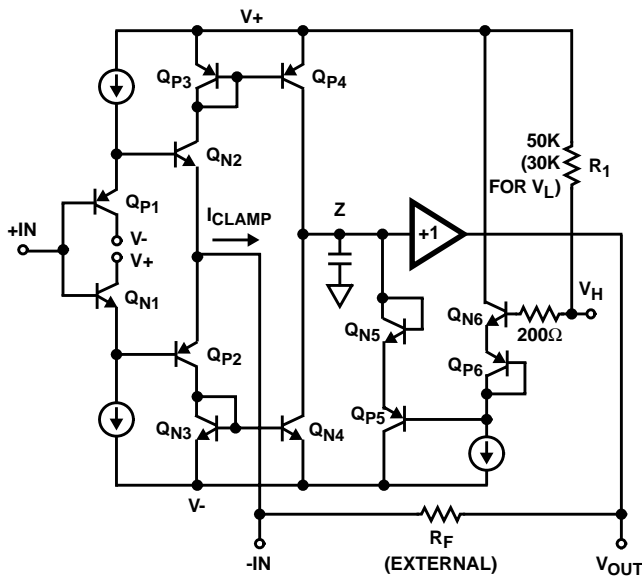


FIGURE 1. HS-1135RH SIMPLIFIED V_H CLAMP CIRCUITRY

Tracing the path from V_H to Z illustrates the effect of the clamp voltage on the high impedance node. V_H decreases by $2V_{BE}$ (Q_{N6} and Q_{P6}) to set up the base voltage on Q_{P5} . Q_{P5} begins to conduct whenever the high impedance node reaches a voltage equal to Q_{P5} 's base + $2V_{BE}$ (Q_{P5} and Q_{N5}). Thus, Q_{P5} clamps node Z whenever Z reaches V_H . R_1 provides a pull-up network to ensure functionality with

the clamp inputs floating. A similar description applies to the symmetrical low clamp circuitry controlled by V_L .

When the output is clamped, the negative input continues to source a slewing current (I_{CLAMP}) in an attempt to force the output to the quiescent voltage defined by the input. Q_{P5} must sink this current while clamping, because the $-IN$ current is always mirrored onto the high impedance node. The clamping current is calculated as $(V_{-IN} - V_{OUT})/R_F$. As an example, a unity gain circuit with $V_{IN} = 2V$, $V_H = 1V$, and $R_F = 510\Omega$ would have $I_{CLAMP} = (2-1)/510\Omega = 1.96mA$. Note that I_{CC} will increase by I_{CLAMP} when the output is clamp limited.

Clamp Accuracy

The clamped output voltage will not be exactly equal to the voltage applied to V_H or V_L . Offset errors, mostly due to V_{BE} mismatches, necessitate a clamp accuracy parameter which is found in the device specifications. Clamp accuracy is a function of the clamping conditions. Referring again to Figure 1, it can be seen that one component of clamp accuracy is the V_{BE} mismatch between the Q_{X6} transistors, and the Q_{X5} transistors. If the transistors always ran at the same current level there would be no V_{BE} mismatch, and no contribution to the inaccuracy. The Q_{X6} transistors are biased at a constant current, but as described earlier, the current through Q_{X5} is equivalent to I_{CLAMP} . V_{BE} increases as I_{CLAMP} increases, causing the clamped output voltage to increase as well. I_{CLAMP} is a function of the overdrive level $(V_{-IN} - V_{OUTCLAMPED})$ and R_F , so clamp accuracy degrades as the overdrive increases, or as R_F decreases. As an example, the specified accuracy of $\pm 60mV$ for a 2X overdrive with $R_F = 510\Omega$ degrades to $\pm 220mV$ for $R_F = 240\Omega$ at the same overdrive, or to $\pm 250mV$ for a 3X overdrive with $R_F = 510\Omega$.

Consideration must also be given to the fact that the clamp voltages have an effect on amplifier linearity. The "Nonlinearity Near Clamp Voltage" curve in the data sheet illustrates the impact of several clamp levels on linearity.

Clamp Range

Unlike some competitor devices, both V_H and V_L have usable ranges that cross 0V. While V_H must be more positive than V_L , both may be positive or negative, within the range restrictions indicated in the specifications. For example, the HS-1135RH could be limited to ECL output levels by setting $V_H = -0.8V$ and $V_L = -1.8V$. V_H and V_L may be connected to the same voltage (GND for instance) but the result won't be in a DC output voltage from an AC input signal. A 150 - 200mV AC signal will still be present at the output.

Recovery from Overdrive

The output voltage remains at the clamp level as long as the overdrive condition remains. When the input voltage drops below the overdrive level (V_{CLAMP}/A_{VCL}) the amplifier will return to linear operation. A time delay, known as the Overdrive Recovery Time, is required for this resumption of linear operation. The plots of "Unclamped Performance" and "Clamped Performance" highlight the HS-1135RH's

subnanosecond recovery time. The difference between the unclamped and clamped propagation delays is the overdrive recovery time. The appropriate propagation delays are 4.0ns for the unclamped pulse, and 4.8ns for the clamped (2X overdrive) pulse yielding an overdrive recovery time of 800ps. The measurement uses the 90% point of the output transition to ensure that linear operation has resumed. Note: The propagation delay illustrated is dominated by the fixturing. The delta shown is accurate, but the true HS-1135RH propagation delay is 500ps.

Use of Die in Hybrid Applications

This amplifier is designed with compensation to negate the package parasitics that typically lead to instabilities. As a result, the use of die in hybrid applications results in overcompensated performance due to lower parasitic capacitances. Reducing R_F below the recommended values for packaged units will solve the problem. For $A_V = +2$ the recommended starting point is 300Ω, while unity gain applications should try 400Ω.

PC Board Layout

The frequency performance of this amplifier depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value chip (0.1μF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to pin 2, and connections to pin 2 should be kept as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

Evaluation Board

An evaluation board is available for the HS-1135RH, (HFA11XXEVAL). Please contact your local sales office for information.

The layout and schematic of the board are shown here:

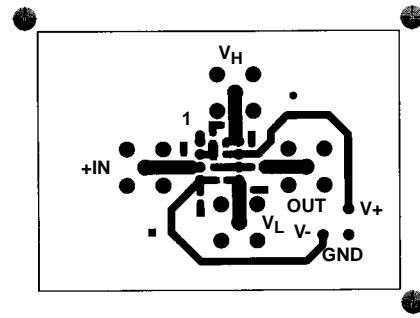


FIGURE 2A. TOP LAYOUT

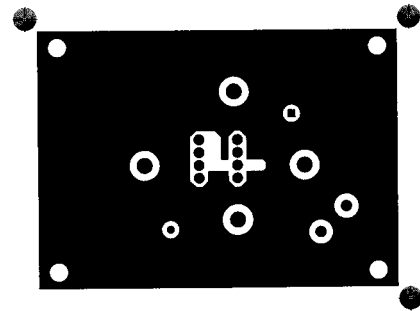


FIGURE 2B. BOTTOM LAYOUT

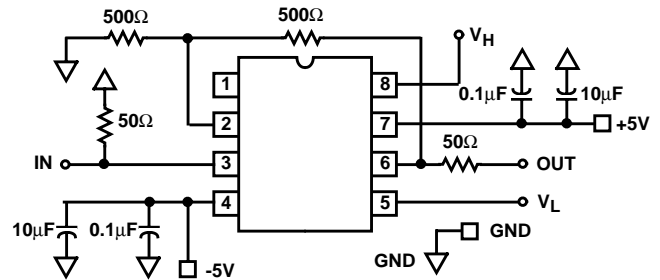
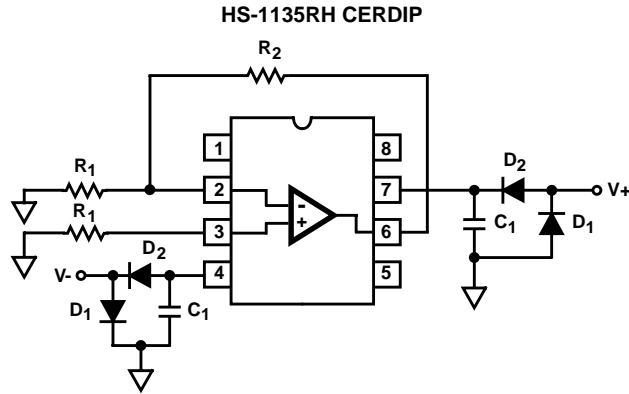


FIGURE 2C. SCHEMATIC

FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT

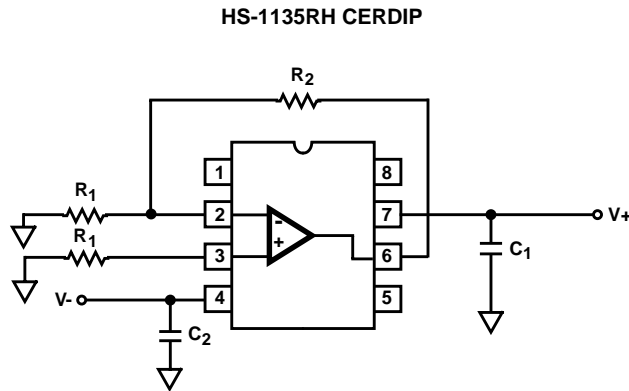
Burn-In Circuit



NOTES:

1. $R_1 = 1k\Omega, \pm 5\%$ (Per Socket)
2. $R_2 = 10k\Omega, \pm 5\%$ (Per Socket)
3. $C_1 = 0.01\mu F$ (Per Socket) or $0.1\mu F$ (Per Row) Minimum
4. $D_1 = 1N4002$ or Equivalent (Per Board)
5. $D_2 = 1N4002$ or Equivalent (Per Socket)
6. $V+ = +5.5V \pm 0.5V$
7. $V- = -5.5V \pm 0.5V$

Irradiation Circuit



NOTES:

8. $R_1 = 1k\Omega, \pm 5\%$
9. $R_2 = 10k\Omega, \pm 5\%$
10. $C_1 = C_2 = 0.01\mu F$
11. $V+ = +5.0V \pm 0.5V$
12. $V- = -5.0V \pm 0.5V$

Die Characteristics

DIE DIMENSIONS:

59 mils x 58.2 mils x 19 mils ±1 mil
 1500µm x 1480µm x 483µm ±25.4µm

INTERFACE MATERIALS:

Glassivation:

Type: Nitride
 Thickness: 4kÅ ±0.5kÅ

Top Metallization:

Type: Metal 1: AlCu(2%)/TiW
 Thickness: Metal 1: 8kÅ ±0.4kÅ
 Type: Metal 2: AlCu(2%)
 Thickness: Metal 2: 16kÅ ±0.8kÅ

Substrate:

UHF-1, Bonded Wafer, DI

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Floating

ADDITIONAL INFORMATION:

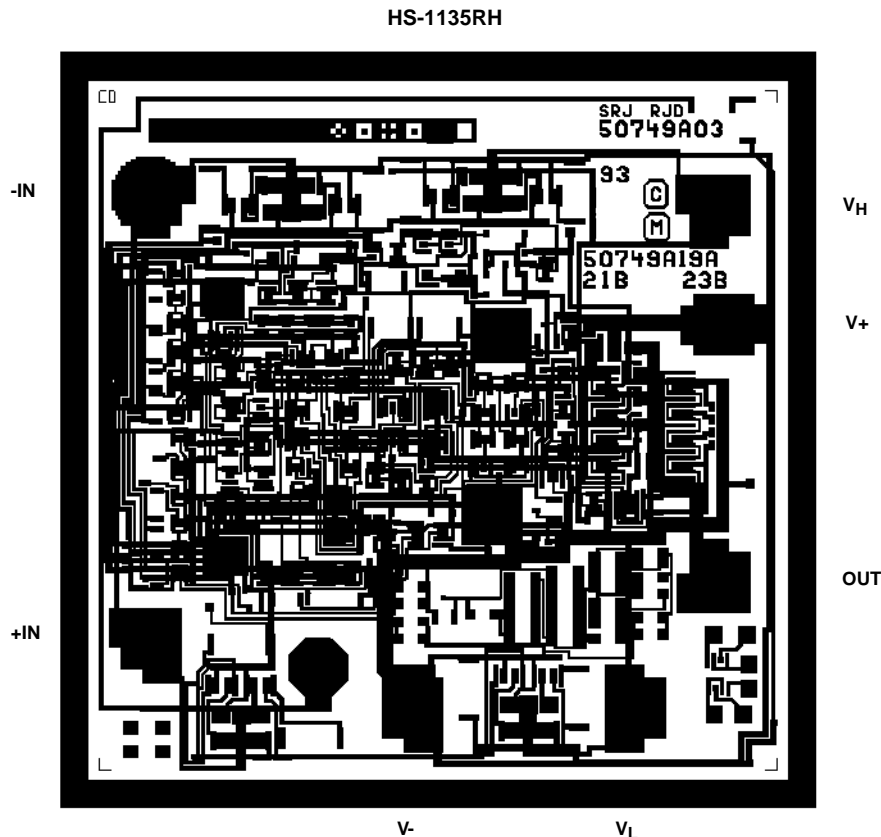
Worst Case Current Density:

< 2 x 10⁵A/cm²

Transistor Count:

89

Metallization Mask Layout



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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