

## Radiation Hardened 8K x 8 CMOS PROM

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil HS-6664RH-T is a radiation hardened 64K CMOS PROM, organized in an 8K word by 8-bit format. The chip is manufactured using a radiation hardened CMOS process, and utilizes synchronous circuit design techniques to achieve high speed performance with very low power dissipation.

On-chip address latches are provided, allowing easy interfacing with microprocessors that use a multiplexed address/data bus structure. The output enable control ( $\bar{G}$ ) simplifies system interfacing by allowing output data bus control in addition to the chip enable control ( $\bar{E}$ ). All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

## Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

**Detailed Electrical Specifications for the HS-666s4RH-T are contained in SMD 5962-95626.** For more information, visit our website at: [www.intersil.com/](http://www.intersil.com/)

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.

[www.intersil.com/](http://www.intersil.com/)

## Ordering Information

ORDERING INFORMATION	PART NUMBER	TEMP. RANGE (°C)
5962R9562601TXC	HS1-6664RH-T	-55 to 125
HS1-6664RH/Proto	HS1-6664RH/Proto	-55 to 125
5962R9562601TYC	HS9-6664RH-T	-55 to 125
HS9-6664RH/Proto	HS9-6664RH/Proto	-55 to 125

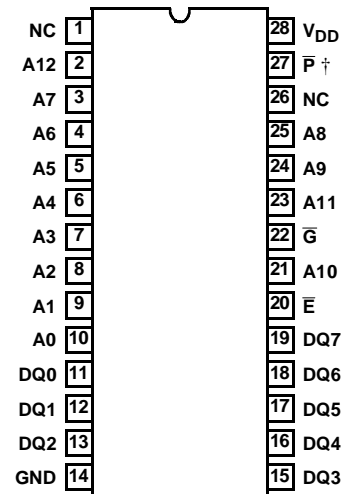
NOTE: **Minimum order quantity for -T is 150 units through distribution, or 450 units direct.**

## Features

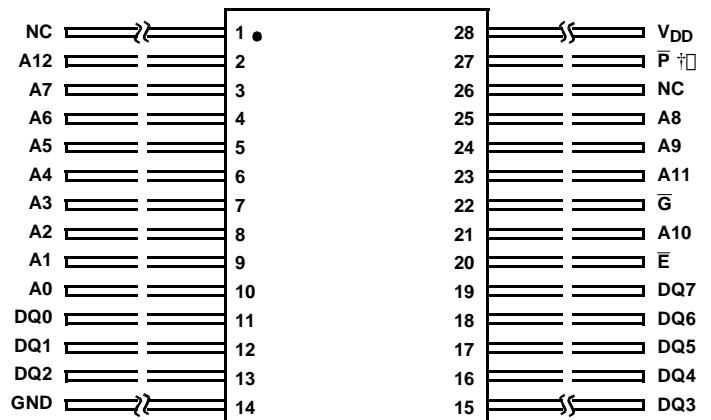
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose ( $\gamma$ )  $1 \times 10^5$  RAD(Si)
  - No Latch-Up, SEU LET  $>100$ MeV/mg/cm<sup>2</sup>
- Transient Output Upset  $>5 \times 10^8$  RAD (Si)/s
- Fast Access Time - 35ns (Typical)
- Single 5V Power Supply, Synchronous Operation
- Single Pulse 10V Field Programmable NiCr Fuses
- On-Chip Address Latches, Three-State Outputs
- Low Standby Current  $<500\mu$ A (Pre-Rad)
- Low Operating Current  $<15$ mA/MHz

## Pinouts

**HS1-6664RH-T (SBDIP), CDIP2-T28**  
TOP VIEW

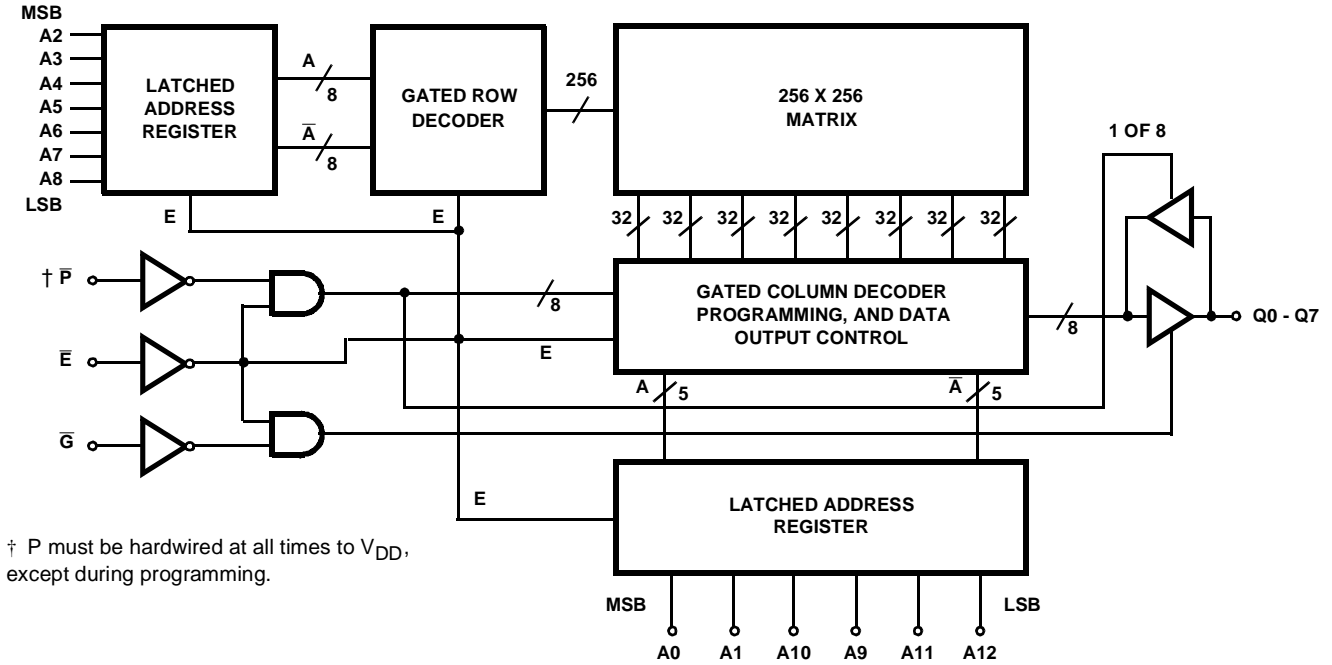


**HS9-6664RH-T (FLATPACK), CDFP3-F28**  
TOP VIEW



†  $\bar{P}$  must be hardwired at all times to  $V_{DD}$ , except during programming.

Functional Diagram



† P must be hardwired at all times to V<sub>DD</sub>, except during programming.

TRUTH TABLE

$\bar{E}$	$\bar{G}$	MODE
0	0	Enabled
0	1	Output Disabled
1	X	Disabled

Timing Waveform

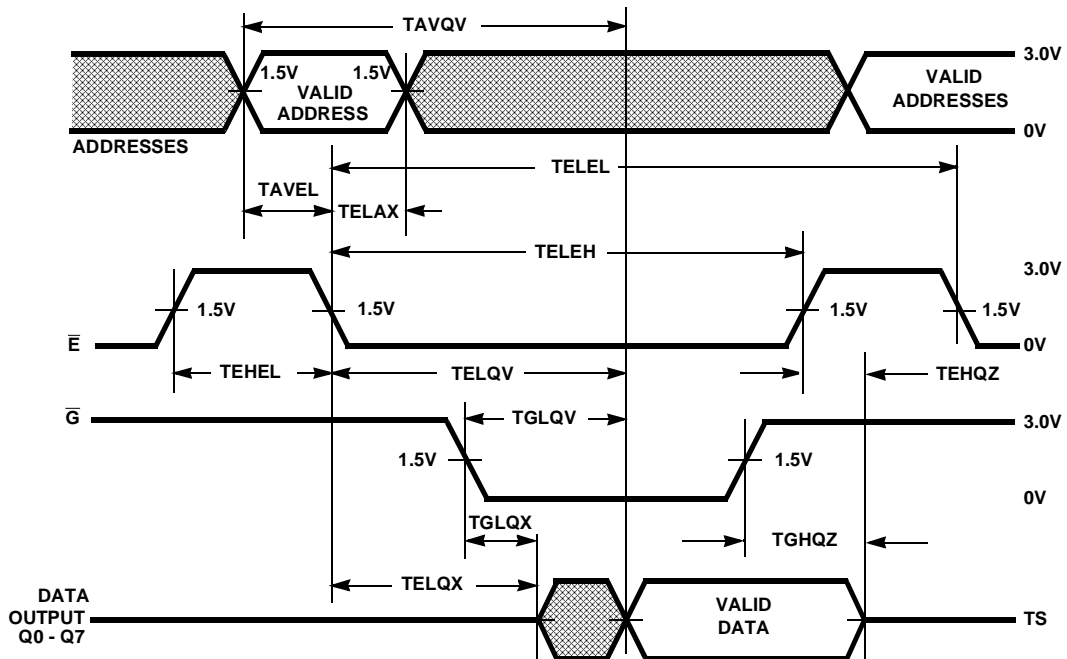


FIGURE 1. READ CYCLE

**Die Characteristics**

**DIE DIMENSIONS:**

(6883 $\mu$ m x 7798 $\mu$ m x 483 $\mu$ m  $\pm$ 25.4 $\mu$ m)  
 271 x 307 x 19mils  $\pm$ 1mil

**METALLIZATION:**

M1: 6k $\text{\AA}$   $\pm$ 1k $\text{\AA}$  Si/Al/Cu  
 2k $\text{\AA}$   $\pm$ 500 $\text{\AA}$  TiW  
 M2: 10k $\text{\AA}$   $\pm$ 2k $\text{\AA}$  Si/Al/Cu

**SUBSTRATE POTENTIAL:**

V<sub>DD</sub>

**BACKSIDE FINISH:**

Silicon

**PASSIVATION:**

Type: Silox (SiO<sub>2</sub>)  
 Thickness: 8k $\text{\AA}$   $\pm$ 1k $\text{\AA}$

**WORST CASE CURRENT DENSITY:**

< 2.0e5 A/cm<sup>2</sup>

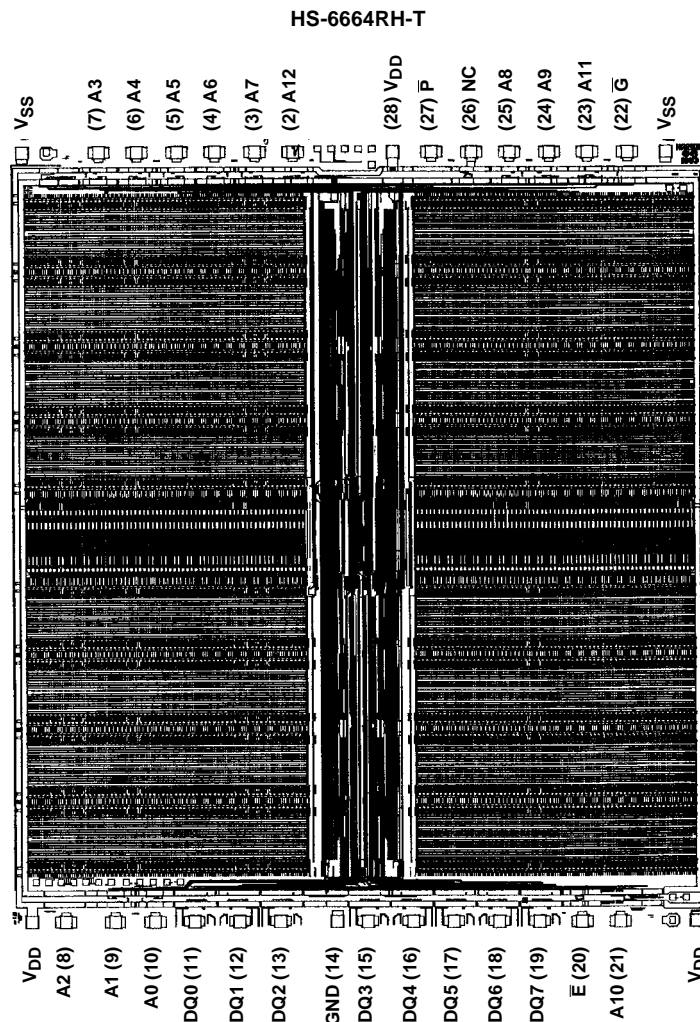
**TRANSISTOR COUNT:**

110, 874, (27,719 Gates)

**PROCESS:**

AVLSI

**Metallization Mask Layout**



All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.  
 Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

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