Demo Kit Available

High Voltage Ring Generator

Ordering Information

Operating Voltage	Package Options
V_{PP1}-V_{NN1}	SOW-20
325V	HV430WG

Features

- ❏ 105Vrms ring signal
- ❏ Output over current protection
- ❏ 5.0V CMOS logic control
- ❏ Logic enable/disable to save power
- ❏ Adjustable deadband in single-control mode
- ❏ Power-on reset
- ❏ Fault output for problem detection

Applications

- ❏ Line access cards
- ❏ Set-top/Street box

Absolute Maximum Ratings

$V_{PP1} – V_{NN1}$, power supply voltage	+340V
V_{PP1}, positive high voltage supply	+220V
V_{PP2}, positive gate voltage supply	+220V
V_{NN1}, negative high voltage supply	-220V
V_{NN2}, negative gate voltage supply	-220V
V_{DD}, logic supply	+7.5V
Storage temperature	-65°C to +150°C
Power dissipation	600mW

General Description

The Supertex HV430 is a high voltage PWM ring generator integrated circuit. The high voltage outputs, V_{PGATE} and V_{NGATE}, are used to drive the gates of external high voltage P-channel and N-channel MOSFETs in a push-pull configuration. Over current protection is implemented for both the P-channel and N-channel MOSFETs. External sense resistors set the over-current trip point.

The RESET input functions as a power-on reset when connected to an external capacitor.

The $\overline{\text{FAULT}}$ output indicates an over-current condition and is cleared after 4 consecutive cycles with no overcurrent condition. A logic low on RESET or ENABLE clears the $\overline{\text{FAULT}}$ output. It is active-low and open-drain to allow wire OR'ing of multiple drivers.

P_{gate} and N_{gate} are controlled independently by logic inputs P_{IN} and N_{IN} when the MODE pin is at logic high. A logic high on P_{IN} will turn on the external P-channel MOSFET. Similarly, a logic high on N_{IN} will turn on the external N-channel MOSFET. Lockout circuitry prevents the N and P switches from turning on simultaneously. A pulse width limiter restricts pulse widths to no less than 100-200ns.

For applications where a single control input is desired, the MODE pin should be connected to SGND. The PWM control signal is then input to the N_{IN} pin. A user-adjustable deadband in the control logic ensures break-before-make on the outputs, thus avoiding cross conduction on the high voltage output during switching. A logic high on N_{IN} will turn the external P-Channel MOSFET on and the N-Channel off, and vice versa. The IC can be powered down by applying a logic low on the ENABLE pin, placing both external MOSFETs in the off state.

Electrical Characteristics

(Over operating supply voltage unless otherwise specified, T_A = -40°C to +85°C.)

External Supplies

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{PP1}	High voltage positive supply	50		200	V	
I_{PP1Q}	V_{PP} quiescent current		250	500	μA	P_{IN}=N_{IN}=0V
I_{PP1}	V_{PP} operating current			2.0	mA	No load V_{OUTP} and V_{OUTN} switching at 100kHz
V_{NN1}	High voltage negative supply	V_{PP1}-325		-50	V	
I_{NN1Q}	V_{NN1} quiescent current		250	500	μA	P_{IN}=N_{IN}=0V, R_{DB} =18kΩ
I_{NN1}	V_{NN1} operating current			1.0	mA	No load V_{OUTP} and V_{OUTN} switching at 100kHz
V_{DD}	Logic supply voltage	4.50		5.50	V	
I_{DDQ}	V_{DD} quiescent current		300	400	μA	P_{IN}=N_{IN}=0V, R_{DB} =18kΩ
I_{DD}	V_{DD} operating current			1.0	mA	P_{IN}=N_{IN}=100kHz, R_{DB} =18kΩ

Internal Supplies

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{PP2}	Positive linear regulator output voltage	V_{PP1}-16		V_{PP1}-10	V	
V_{NN2}	Negative linear regulator output voltage	V_{NN1}+10		V_{NN1}+14	V	

Positive High Voltage Output

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{Pgate}	Output voltage swing	V_{PP2}		V_{PP1}	V	No load on V_{Pgate}
$R_{sourceP}$	V_{Pgate} source resistance			12.5	Ω	I_{OUT}=80mA
R_{sinkP}	V_{Pgate} sink resistance			12.5	Ω	I_{OUT}=-80mA
t_{riseP}	V_{Pgate} rise time			50	ns	C_{load}=1.4nF
t_{fallP}	V_{Pgate} fall time			50	ns	C_{load}=1.4nF
$t_{pwp(min)}$	V_{Pgate} minimum pulse width (internally limited)	100	150	200	ns	
t_{delayP}	P_{IN} to Pgate delay time			300	ns	mode=1
V_{Psen}	V_{Pgate} current sense voltage	V_{PP1}-0.85	V_{PP1}-1.0	V_{PP1}-1.15	V	
t_{shortP}	V_{Pgate} current sense off time			150	ns	

Negative High Voltage Output

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{Ngate}	Output voltage swing	V_{NN2}		V_{NN1}	V	No load on V_{Ngate}
$R_{sourceN}$	V_{Ngate} source resistance			15.0	Ω	I_{OUT}=80mA
R_{sinkN}	V_{Ngate} sink resistance			15.0	Ω	I_{OUT}=-80mA
t_{riseN}	V_{Ngate} rise time			50	ns	C_{load}=1.0nF
t_{fallN}	V_{Ngate} fall time			50	ns	C_{load}=1.0nF
$t_{pwn(min)}$	V_{Ngate} minimum pulse width (internally limited)	100	150	200	ns	
t_{delayN}	N_{IN} to V_{Ngate} delay time			300	ns	mode=1
V_{Nsen}	V_{Ngate} current sense voltage	V_{NN1}+0.85	V_{NN1}+1.0	V_{NN1}+1.15	V	
t_{shortN}	V_{Ngate} current sense OFF time			150	ns	

Control Circuitry

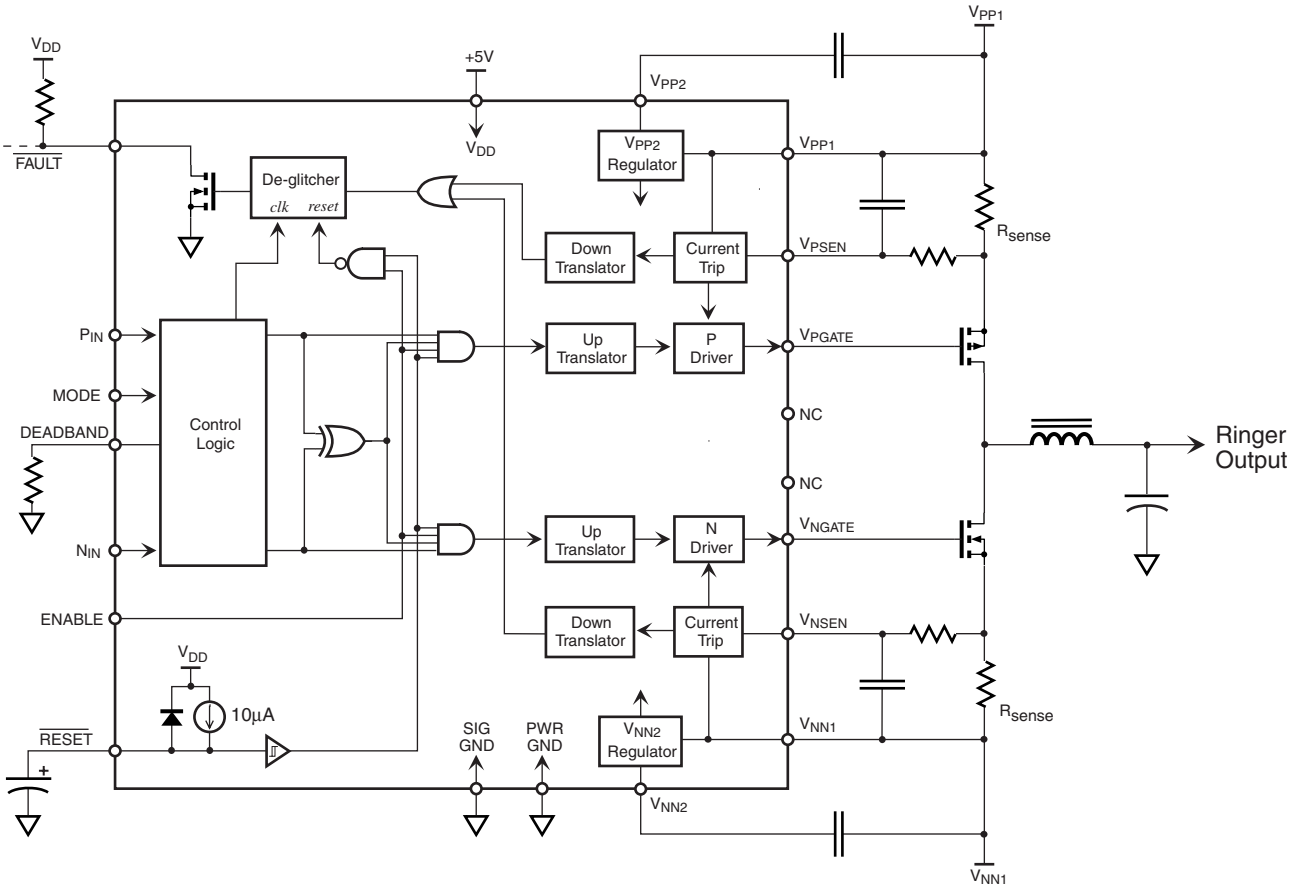
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IL}	Logic input low voltage	0		0.60	V	V_{DD}=5.0V
V_{IH}	Logic input high voltage	2.7		5.0	V	V_{DD}=5.0V
I_{INdn}	Input pull-down current	0.5	1	5	μA	P_{IN}, N_{IN}, ENABLE
R_{up}	Input pull-up resistance	100	200	300	kΩ	MODE
V_{OL}	Logic output low voltage			0.50	V	V_{DD}=5.0V, I_{OUT}=-0.5mA
V_{OH}	Logic output high voltage	4.50			V	V_{DD}=5.0V, I_{OUT}=0.5mA
$V_{RST(OFF)}$	Reset voltage, device off	3.2		3.5	V	V_{DD}=5.0V
$V_{RST(ON)}$	Reset voltage, device on	3.7		4.0	V	V_{DD}=5.0V
$V_{RST(HYS)}$	Reset hysteresis voltage	0.3			V	V_{DD}=5.0V
I_{reset}	Reset pull-up current	7	10	13	μA	V_{RESET}=0-4.5V
$t_{RST(ON)}$	RESET on delay			1.0	μs	
$t_{RST(OFF)}$	RESET off delay			1.0	μs	
$t_{EN(ON)}$	ENABLE on delay	50	100	150	μs	
$t_{EN(OFF)}$	ENABLE off delay			1.0	μs	
$t_{FLT(HOLD)}$	FAULT hold time		4		N_{IN}/P_{IN} cycles	ENABLE=1
t_{DB}	Deadband time	35	50	70	ns	Mode=0, Rdb=5.6kΩ
		105	140	175	ns	Mode=0, Rdb=18kΩ
$t_{delay(N-P)}$	N-off to P-on transistion delay			300	ns	Mode=0, Rdb<27kΩ
$t_{delay(P-N)}$	P-off to N-on transistion delay			300	ns	Mode=0, Rdb<27kΩ
$\Delta t_{delay(N-P)}$	Delay difference $t_{delayN(off)}$ - $t_{delayP(on)}$	-80	0	80	ns	Mode=1
$\Delta t_{delay(P-N)}$	Delay difference $t_{delayP(off)}$ - $t_{delayN(on)}$	-80	0	80	ns	Mode=1

Truth Table

Logic Inputs*					Output	
N_{IN}	P_{IN}	mode	EN	RESET	External N-Channel MOSFET	External P-Channel MOSFET
L	L	H	H	> $V_{reset(on)}$	OFF	OFF
L	H	H	H	> $V_{reset(on)}$	OFF	ON
H	L	H	H	> $V_{reset(on)}$	ON	OFF
H	H	H	H	> $V_{reset(on)}$	OFF	OFF
H	X	L	H	> $V_{reset(on)}$	OFF	ON
L	X	L	H	> $V_{reset(on)}$	ON	OFF
X	X	X	L	X	OFF	OFF
X	X	X	X	< $V_{reset(off)}$	OFF	OFF

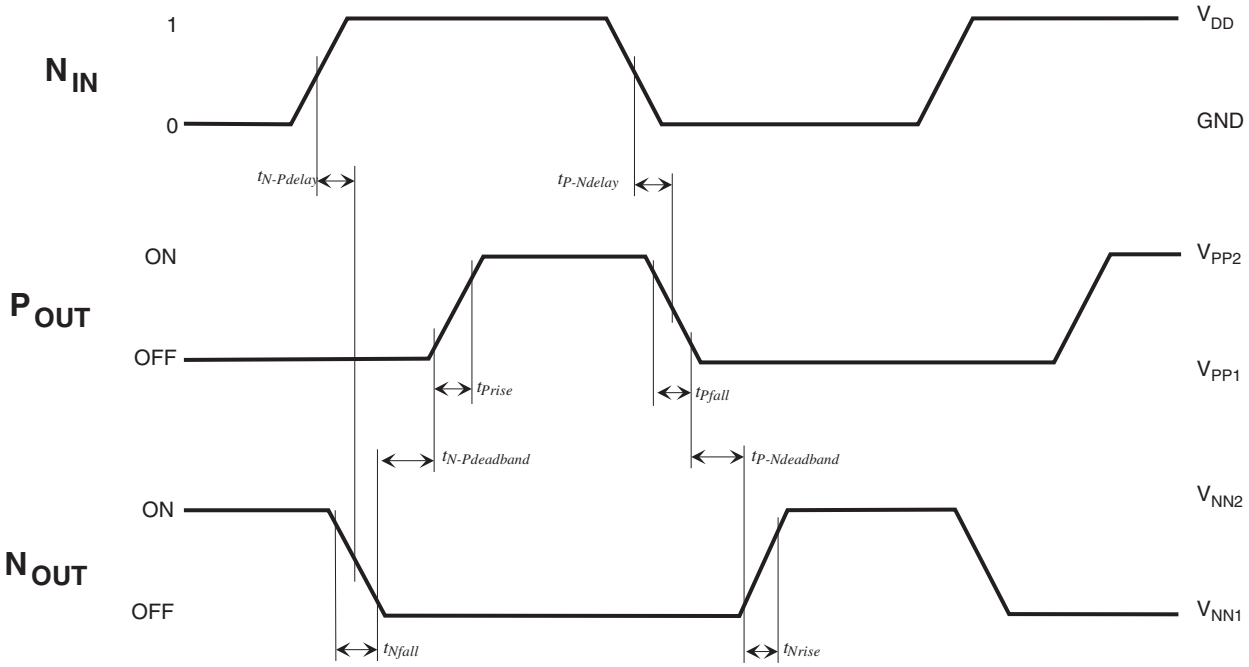
* Unused logic inputs should be connected to V_{DD} or GND.

Block Diagram and Application Circuit

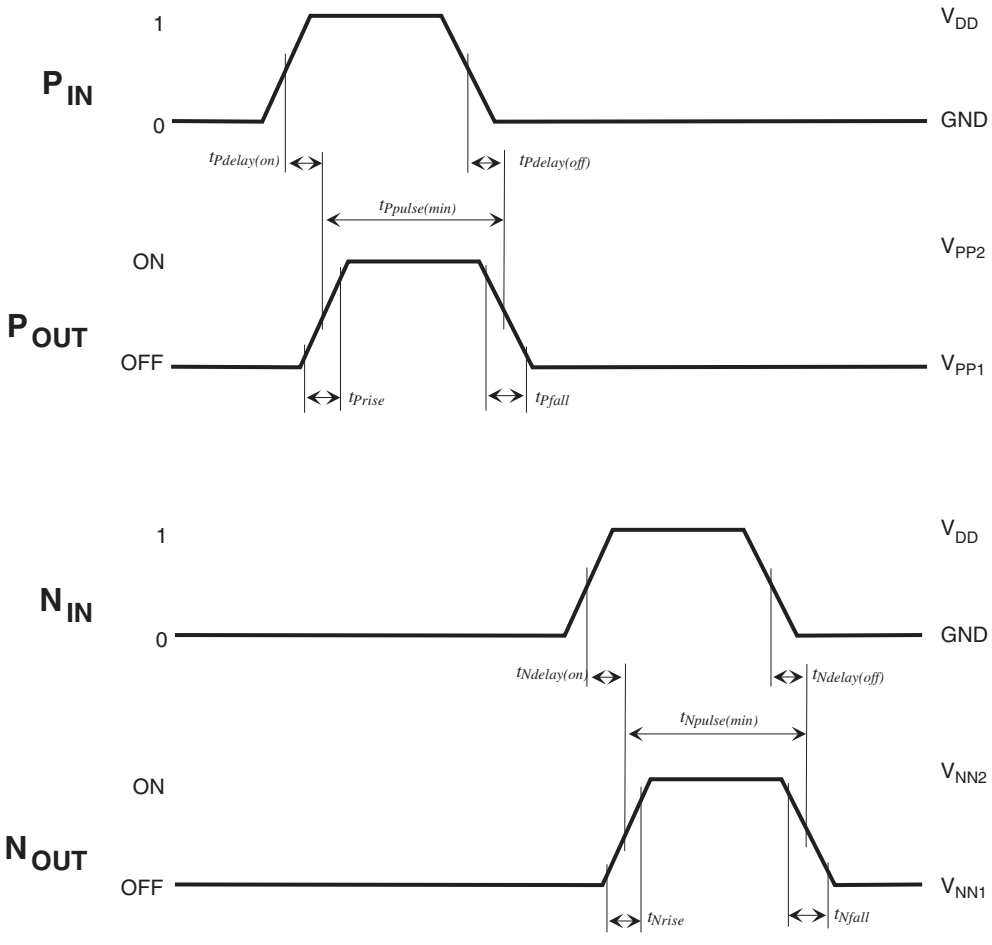


Note: P_{IN}, N_{IN}, and ENABLE are internally pulled low. MODE is internally pulled high.
A Reset capacitor in the range of 1-10µF will yield a couple-second turn-on delay. Tantalum is recommended.

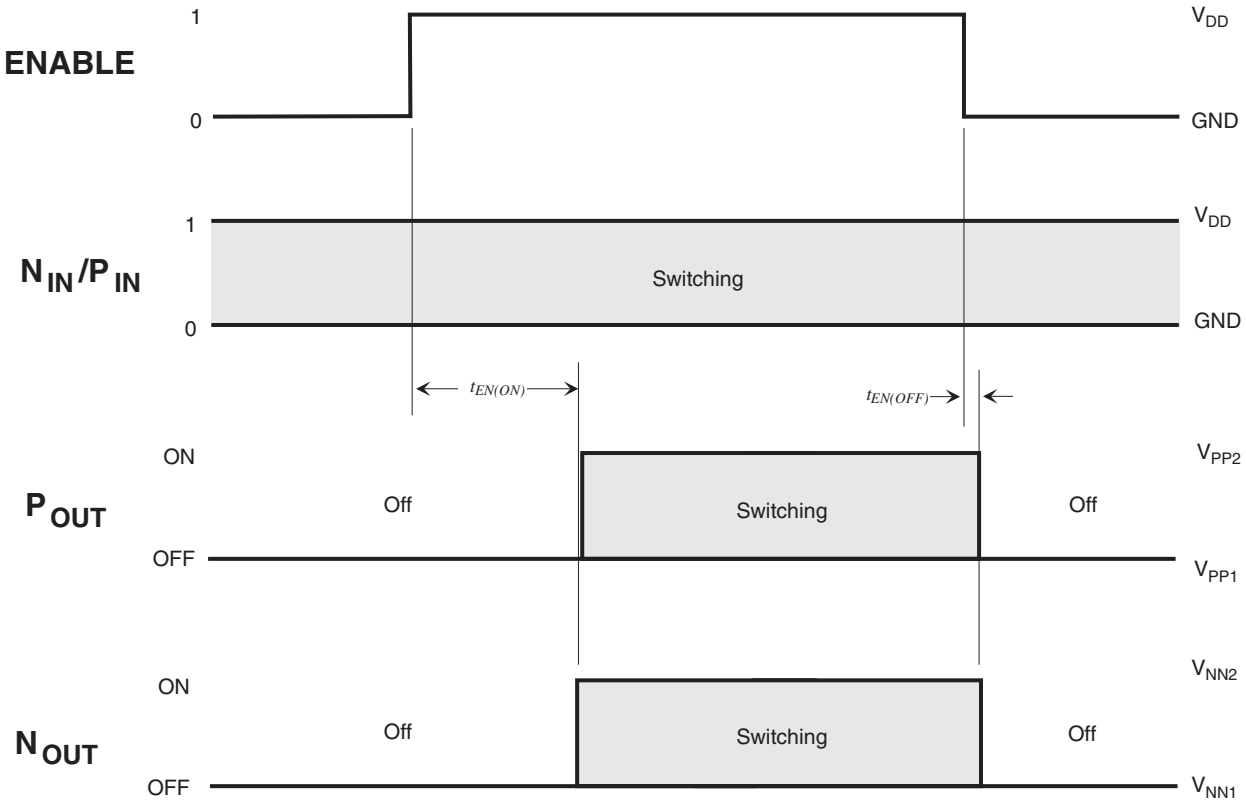
Single-Control Mode Timing



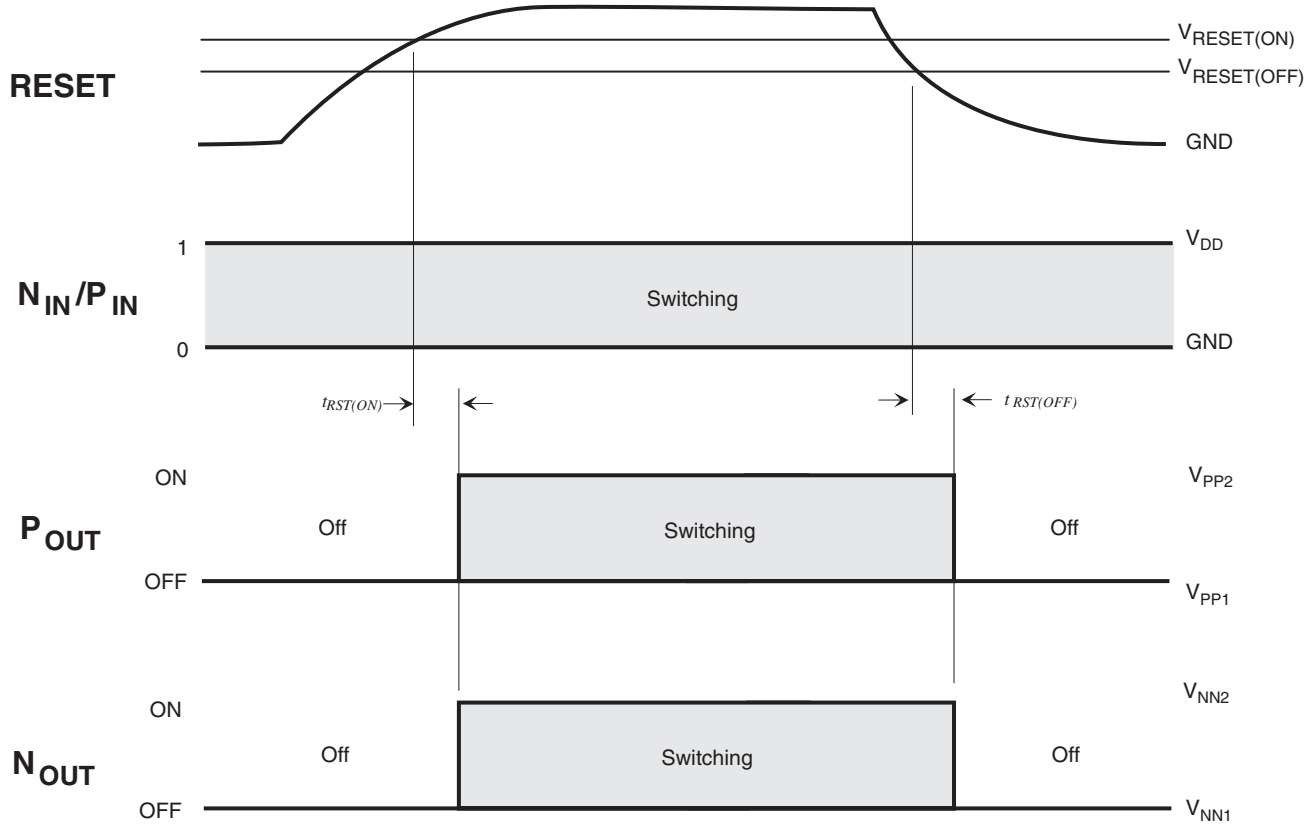
Dual-Control Mode Timing



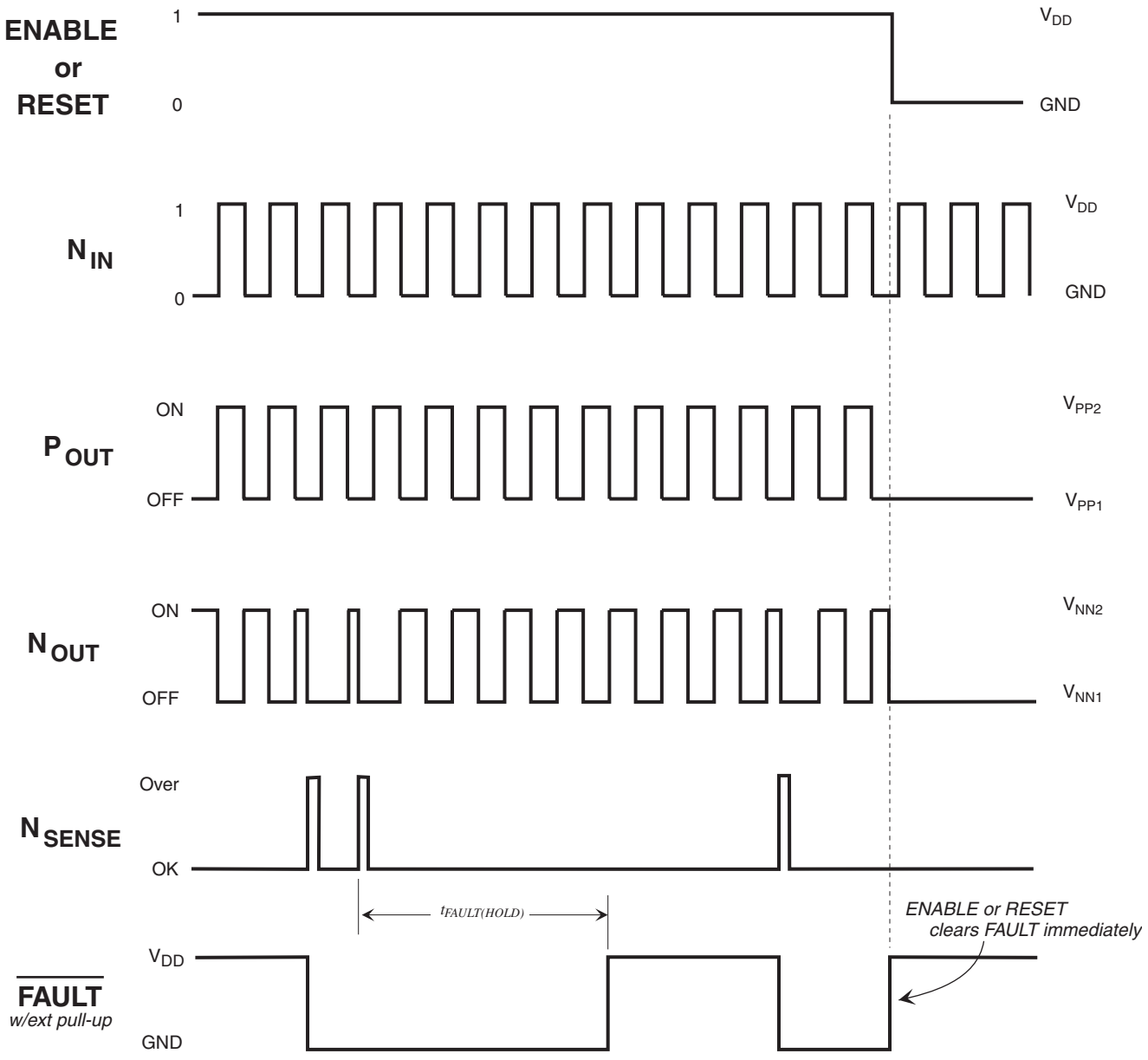
ENABLE Timing



RESET Timing



FAULT Timing

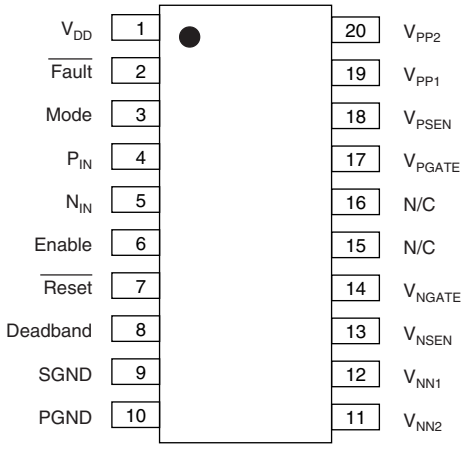


Note: N_{sense} overcurrent shown. P_{sense} operates identically.

Pin Description

V_{PP1}	Positive high voltage supply.
V_{PP2}	Positive gate voltage supply. Generated by an internal linear regulator. A 25V, 100nF capacitor should be connected between V_{PP2} and V_{PP1}.
V_{NN1}	Negative high voltage supply.
V_{NN2}	Negative gate voltage supply. Generated by an internal linear regulator. A 25V, 100nF capacitor should be connected between V_{NN2} and V_{NN1}.
V_{DD}	Logic supply voltage.
SGnd	Low voltage logic ground.
PGnd	High voltage power ground.
P_{IN}	Logic control input. When mode is high, logic input high turns ON the external high voltage P-channel MOSFET. Internally pulled low.
N_{IN}	Logic control input. When mode is high, logic input high turns ON the external high voltage N-channel MOSFET. Internally pulled low.
ENABLE	Logic enable input. Logic high enables IC. Internally pulled low.
MODE	Logic mode input. 0=single-control; 1=dual-control. When MODE is high, N_{IN} and P_{IN} independently control N_{OUT} and P_{OUT}, respectively. When MODE is low, N_{IN} controls both outputs in a complementary manner. (See Truth Table)
$\overline{\text{FAULT}}$	Logic output. Fault is at logic low when either current limit sense pin, V_{Psen} or V_{Nsen}, is activated. Remains active until overcurrent condition clears or ENABLE=0 or RESET=0.
$\overline{\text{RESET}}$	Power-on reset. A capacitor connected between this pin and ground determines the delay time between application of V_{DD} and when the device outputs are enabled. Low leakage tantalum recommended.
DEADBAND	A resistor between this pin and ground sets the 'break-before-make' time between output transitions. Applicable only in single-control mode. For minimum deadtime, a 5.6kΩ resistor to ground should be used. For dual-input mode, tie to Vdd.
V_{Pgate}	Gate drive for external P-channel MOSFET.
V_{Ngate}	Gate drive for external N-channel MOSFET.
V_{Psen}	Pulse by pulse over current sensing for P-Channel MOSFET.
V_{Nsen}	Pulse by pulse over current sensing for N-Channel MOSFET.

Pin Configuration



top view

SOW 20

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