# 8-Channel Serial to Parallel Converter with High Voltage Push-Pull Outputs, POL, Hi-Z, and Short Circuit Detect

## Features

❏ HVCMOS, technology

❏ Operating output voltage of 250V

❏ Low power level shifting from 5V to 250V

❏ Shift register speed 8MHz @ $V_{DD}$=5V

❏ 8 latch data outputs

❏ Output polarity and blanking

❏ CMOS compatible inputs

❏ Output short circuit detect

❏ Output high-Z control

## Applications

❏ Piezoelectric transducer driver

❏ Weaving applications

❏ Braille

❏ Printers

❏ MEMs

❏ Displays

## General Description

The HV513 is a low voltage serial to high voltage parallel converter with 8 high voltage push-pull outputs. This device has been designed to drive small capacitve loads such as piezoelectric transducers. It can also be used in any application requiring multiple high voltage outputs, with medium current source and sink capabilities.

The device consists of an 8-bit shift register, 8 latches, and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the shift register on the low to high transition of the clock. A data output buffer is provided for cascading devices. Operation of the shift register is not affected by the /LE, /BL, /POL, or the /HI-Z control inputs. Transfer of data from the shift register to the latch occurs when the /LE is high. The data in the latch is stored when /LE is low. A high-Z, /HI-Z, pin is provided to set all the outputs in a high-Z state.

All outputs have short circuit protection that detects if the outputs have reached the required output state. If output does not track the required state, then the /SHORT pin will be low. This output will pulse low during the output transistion period under normal operation; see SC Timing Diagram for details.

All outputs will have a break-before-make circuitry to reduce cross-over current during output state changes.

Note: All logic control inputs have internal 20k-ohm pull-up resistors.

## Top Block Diagram
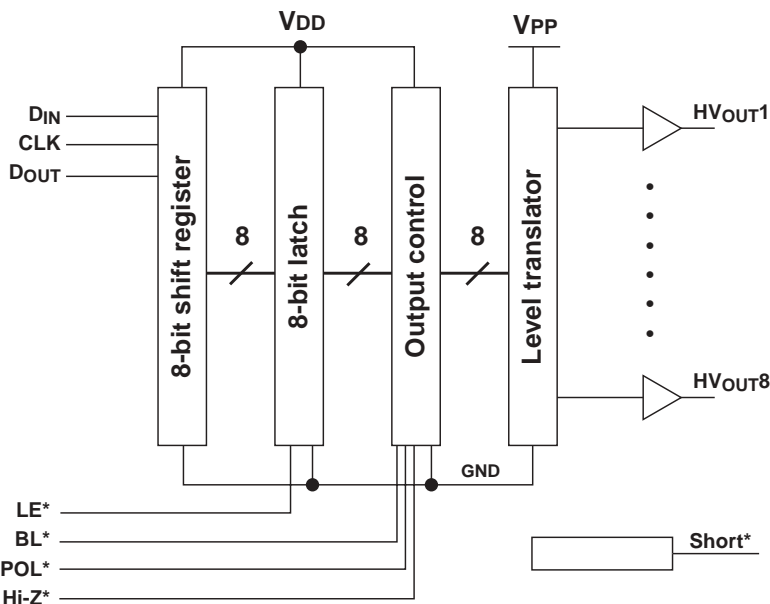
## DC Electrical Characteristics (Over operating supply voltages unless otherwise noted)

| Symbol | Parameter | | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ | $V_{DD}$ supply current | | | | 4 | mA | $f_{CLK}$=8MHz, LE*=LOW |
| $I_{DDQ}$ | Quiescent $V_{DD}$ supply current | | | | 0.1 | mA | All $V_{IN}$=$V_{DD}$ |
| | | | | | 2.0 | | All $V_{IN=}$0V |
| $I_{PP}$ | $V_{PP}$ supply current | | | | 100 | µA | $V_{PP}$=250V, $f_{OUT}$=300Hz, no load |
| $I_{PPQ}$ | Quiescent $V_{PP}$ supply current | | | | 100 | µA | $V_{PP}$=240V, outputs static |
| $I_{IH}$ | High-level logic input current | | | | 10 | µA | $V_{IH}$=$V_{DD}$ |
| $I_{IL}$ | Low-level logic input current | | | | -10 | µA | $V_{IL}$=0V |
| | | | | | -350 | | $V_{IL}$=0V, for inputs w/pull-up resistors |
| $V_{OH}$ | High-level output | $H_{VOUT}$ | 140 | | | V | $V_{PP}$ =200V, $I_{HVOUT}$=-20mA |
| | | Data out | $V_{DD}$-1V | | | | $I_{DOUT}$=-0.1mA |
| $V_{OL}$ | Low-level output | $H_{VOUT}$ | | | 60 | V | $V_{DD}$ =4.5V, $I_{HVOUT}$=20mA |
| | | Data out | | | 1.0 | | $I_{DOUT}$=0.1mA |

## DC Electrical Characteristics (Over operating supply voltages unless otherwise noted)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $f_{CLK}$ | Clock frequency | 0 | | 8 | MHz | |
| $f_{OUT}$ | Output switching frequency (SOA limited) | | 300 | | Hz | $C_L$=50nF, $V_{PP}$=200V |
| $t_W$ | Clock width high and low | 62 | | | ns | |
| $t_{SU}$ | Data setup time before clock rises | 15 | | | ns | |
| $t_H$ | Data hold time after clock rises | 30 | | | ns | |
| $t_{WLE}$ | Width of latch enable pulse | 80 | | | ns | |
| $t_{DLE}$ | /LE delay time after rising edge of clock | 35 | | | ns | |
| $t_{SLE}$ | /LE setup time before rising edge of clock | 40 | | | ns | |
| $t_{OR}$, $t_{OF}$ | Rise/fall time of $HV_{OUT}$ | | | 1000 | µs | $C_L$=100nF, $V_{PP}$=200V |
| $t_{d\ ON/OFF}$ | Delay time for output to start rise/fall | | | 500 | ns | |
| $t_{DHL}$ | Delay time clock to $D_{OUT}$ high to low | | | 110 | ns | $C_L$=15pF |
| $t_{DLH}$ | Delay time clock to $D_{OUT}$ low to high | | | 110 | ns | $C_L$=15pF |
| $t_R$, $t_F$ | All logic inputs | | | 5 | ns | |
| $t_{SD}$ | Output short circuit detection | | | 500 | ns | Short to output fall of /SHORT, $C_L$=15pF |
| $t_{SC}$ | Output short circuit clear | | | 1000 | ns | Short clear to output rise of /SHORT |
| $t_{HI-Z}$ | Output high-Z state | | | 500 | ns | |

# Absolute Maximum Ratings*

| | |
|---|---|
| Supply Voltage, $V_{DD}$ | -0.5V to 6V |
| Supply Voltage, $V_{PP}$ | $V_{DD}$ to 275V |
| Logic input levels | -0.5V to $V_{DD}$+0.5V |
| Ground current | 0.3A |
| High voltage supply current | 0.25A |
| Continuous total power dissipation | 750mW |
| Operating temperature range | -40°C to +85°C |
| Storage temperature range | -65°C +150°C |

* All voltages are referenced to device ground.

# Ordering Information

| Device | Part Number | Package |
|---|---|---|
| HV513 | HV513WG | 24 Lead SOW |

## Operating Supply Voltages

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|--------|-----------|-----|-----|-----|-------|------------|
| $V_{DD}$ | Logic supply voltage | 4.5 | 5.0 | 5.5 | V | |
| $V_{PP}$ | High voltage supply | 30 | | 250 | V | Note 1 |
| $V_{IH}$ | High-level input voltage | $V_{DD}$-0.9 | | $V_{DD}$ | V | |
| $V_{IL}$ | Low-level input voltage | 0 | | 0.9 | V | |
| $T_A$ | Operating free-air temperature | -40 | | +85 | ° C | |

**Notes:**

1.  Below minimum $V_{PP}$ the output may not switch.

2.  **Power-up sequence should be the following:**

    1.  Connect ground.
    2.  Apply $V_{DD}$.
    3.  Set all inputs (Data, CLK, Enable, etc.) to a known state.
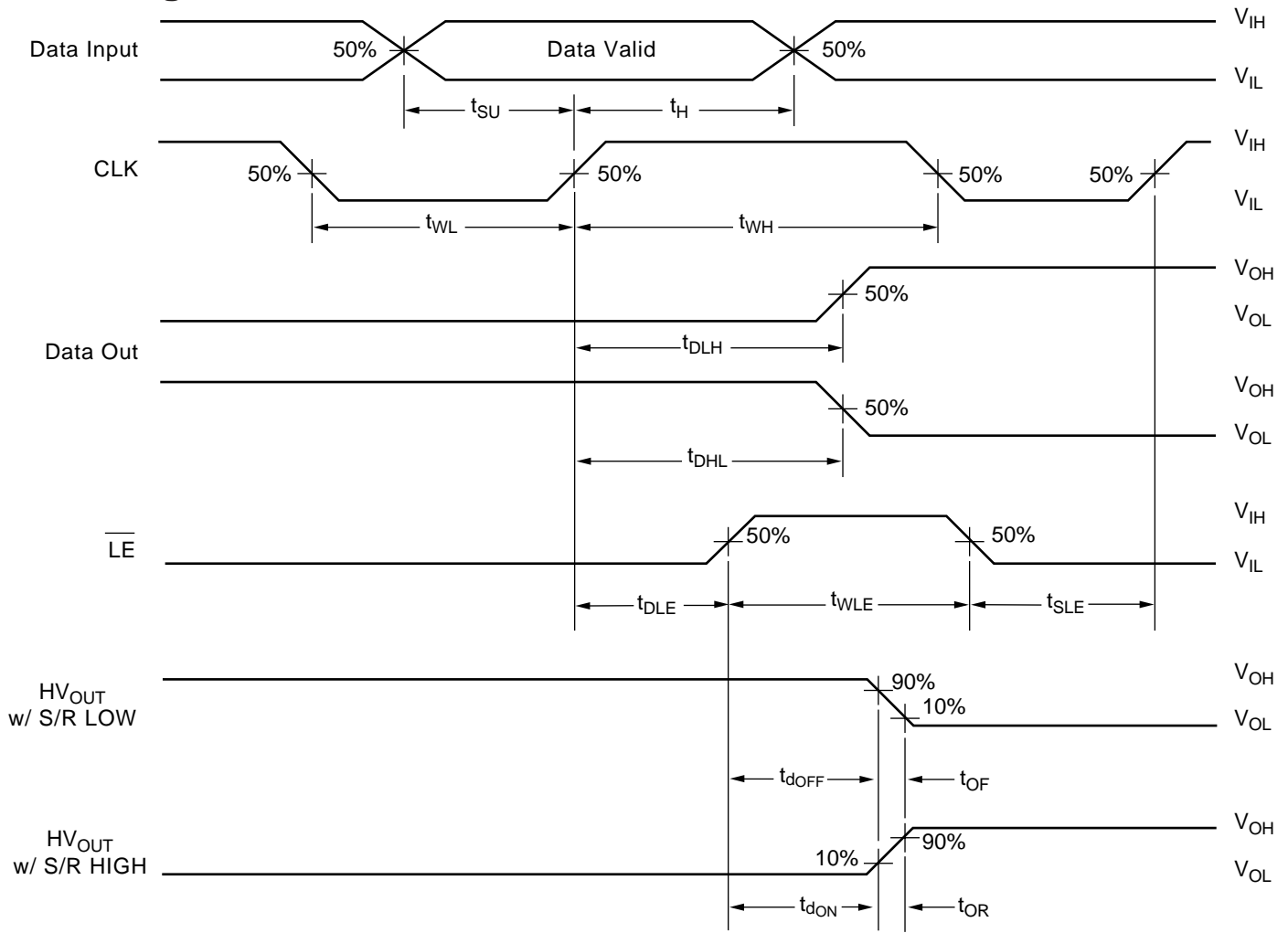    4.  Apply $V_{PP}$.

    Power-down sequence should be the reverse of the above.
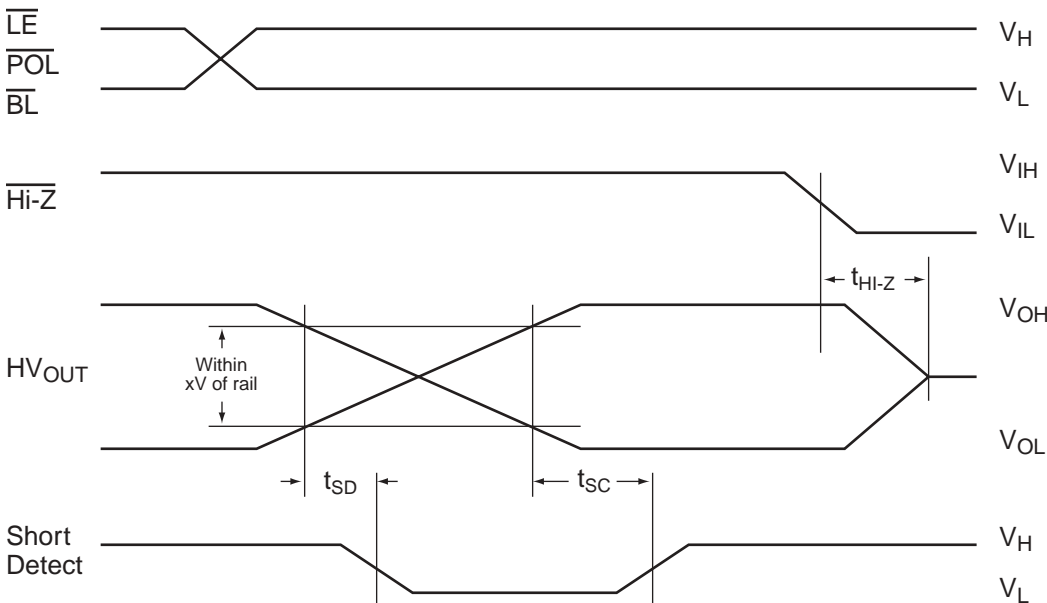
# Input and Output Equivalent Circuits



Logic Inputs

Logic Data Output

High Voltage Outputs

*  $\overline{POL}$, $\overline{BL}$, $\overline{LE}$, and $\overline{HI\text{-}Z}$
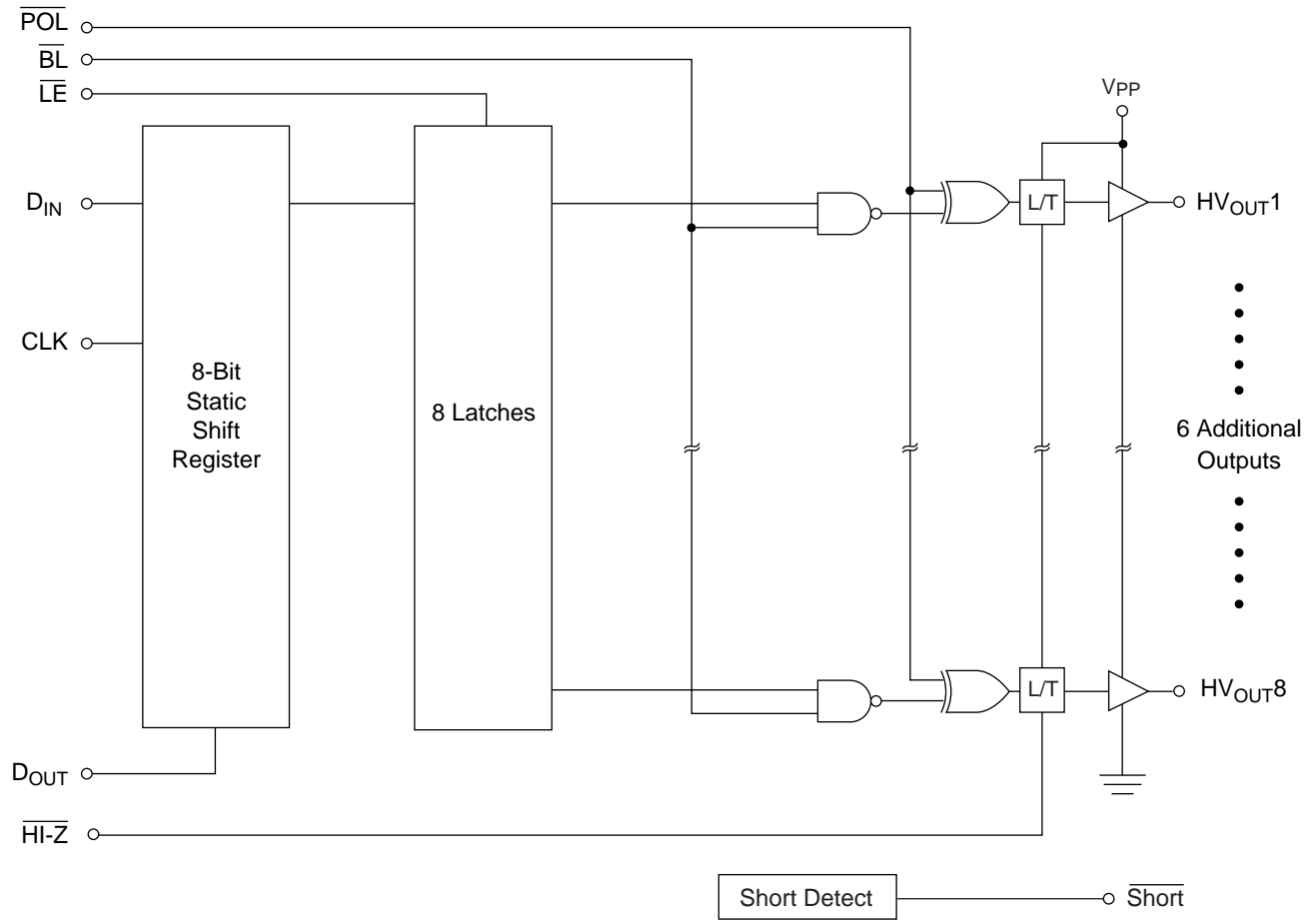
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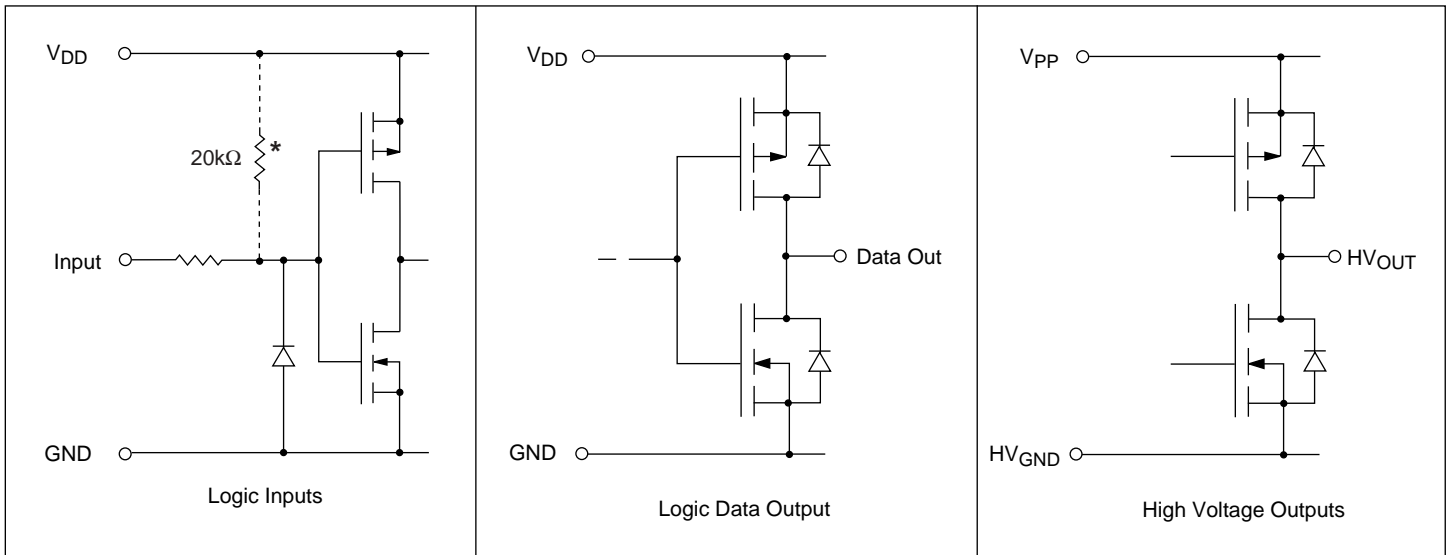
## Switching Waveforms



## Short Circuit Detect Detail Timing (HV513)



If the output is not within 5V to 10V of the desired output state, the SHORT signal goes LOW.

# Functional Block Diagram



$\overline{POL}$, $\overline{BL}$, $\overline{LE}$, and $\overline{HI\text{-}Z}$ have internal 20kΩ pull-up resistors.
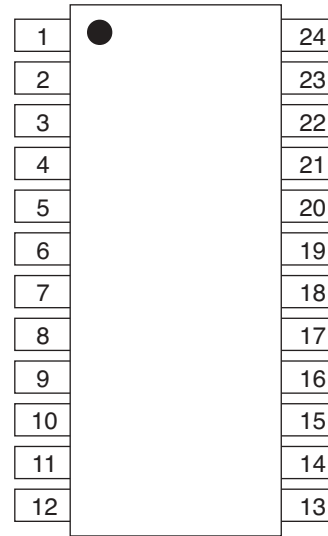
# Function Table

| Function | Inputs | | | | | | Outputs | | |
|---|---|---|---|---|---|---|---|---|---|
| | Data | CLK | /LE | /BL | /POL | /HI-Z | Shift Reg<br>1  2…8 | HV Outputs<br>1  2..8 | Data Out<br>* |
| All on | X | X | X | L | L | H | *  *…* | H  H…H | * |
| All off | X | X | X | L | H | H | *  *…* | L  L…L | * |
| Invert mode | X | X | L | H | L | H | *  *…* | *  *…* (b) | * |
| Load S/R | H or L | ⬆ | L | H | H | H | H or L *…* | *  *…* | * |
| Store Data in latches | X | X | L | H | H | H | *  *…* | *  *…* | * |
| | X | X | L | H | L | H | *  *…* | *  *…* (b) | * |
| Transparent mode | L | ⬆ | H | H | H | H | L  *…* | L  *…* | * |
| | H | ⬆ | H | H | H | H | H  *…* | H  *…* | * |
| Outputs High-Z | X | X | X | X | X | L | *  *…* | High impedance<br>outputs | * |
| Outputs ON | X | X | X | X | X | H | *  *…* | *  *…* | * |

# Pin Configuration

| Pin | Function |
|-----|----------|
| 1 | N/C |
| 2 | $V_{DD}$ |
| 3 | $D_{OUT}$ |
| 4 | $\overline{BL}$ |
| 5 | $\overline{POL}$ |
| 6 | CLK |
| 7 | $\overline{LE}$ |
| 8 | $\overline{SHORT}$ |
| 9 | $\overline{HI\text{-}Z}$ |
| 10 | $D_{IN}$ |
| 11 | LGND |
| 12 | N/C |
| 13 | HVGND |
| 14 | HVGND |
| 15 | $HV_{out}1$ |
| 16 | $HV_{out}2$ |
| 17 | $HV_{out}3$ |
| 18 | $HV_{out}4$ |
| 19 | $HV_{out}5$ |
| 20 | $HV_{out}6$ |
| 21 | $HV_{out}7$ |
| 22 | $HV_{out}8$ |
| 23 | $V_{PP}$ |
| 24 | $V_{PP}$ |

# Package Outline



24-Lead SOW Package (WG)
(Wide Body)

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