DESCRIPTION

The HY62256A/ HY62256A-I is a high-speed, low power and 32,786 x 8-bits CMOS Static Random Access Memory fabricated using Hyundai's high performance CMOS process technology. The HY62256A/ HY62256A-I has a data retention mode that guarantees data to remain valid at the minimum power supply voltage of 2.0 volt. Using the CMOS technology, supply voltages from 2.0 to 5.5volt has little effect on supply current in the data retention mode. The HY62256A/HY62256A-I is suitable for use in low voltage operation and battery back-up application.

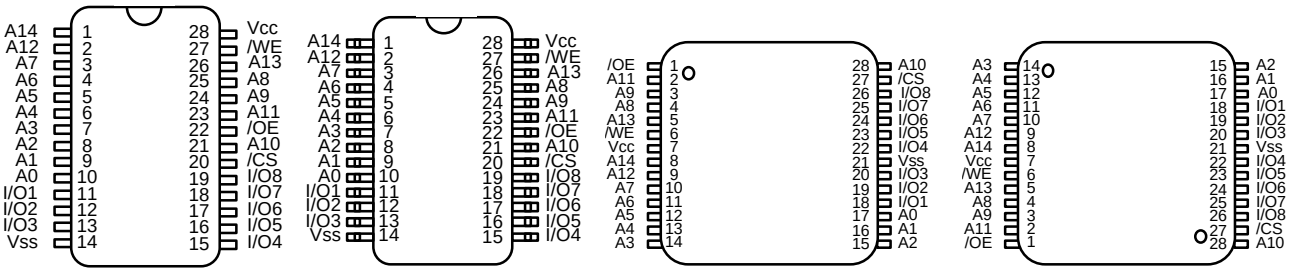
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Low power consumption
- Battery backup(L/LL-part)
  - 2.0V(min.) data retention
- Standard pin configuration
  - 28 pin 600 mil PDIP
  - 28 pin 330mil SOP
  - 28 pin 8x13.4 mm TSOP-I (Standard and Reversed)

Product No.	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA)			Temperature (¡É)
					L	LL	
HY62256A	5.0	55/70/85	50	1mA	100	25	0~70(Normal)
HY62256A-I	5.0	55/70/85	50	1mA	100	-	-40~85(E.T.)

Note 1. E.T. : Extended Temperature, Normal : Normal Temperature
2. Current value is max.

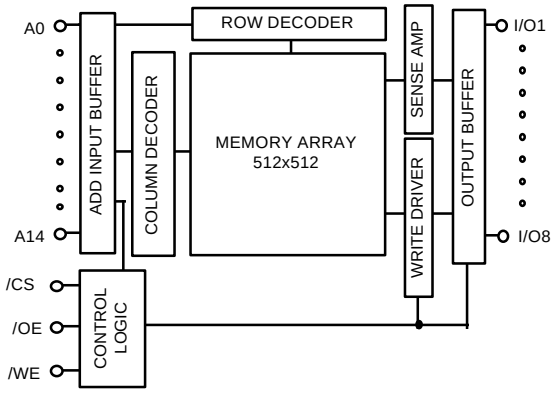
PIN CONNECTION



PIN DESCRIPTION

Pin Name	Pin Function
/CS	Chip Select
/WE	Write Enable
/OE	Output Enable
A0 ~ A14	Address Inputs
I/O1 ~ I/O8	Data Input/Output
Vcc	Power(+5.0V)
Vss	Ground

BLOCK DIAGRAM



ORDERING INFORMATION

Part No.	Speed	Power	Temp.	Package
HY62256AP	55/70/85			PDIP
HY62256ALP	55/70/85	L-part		PDIP
HY62256ALLP	55/70/85	LL-part		PDIP
HY62256AJ	55/70/85			SOP
HY62256ALJ	55/70/85	L-part		SOP
HY62256ALLJ	55/70/85	LL-part		SOP
HY62256AT1	55/70/85			TSOP-I Standard
HY62256ALT1	55/70/85	L-part		TSOP-I Standard
HY62256ALLT1	55/70/85	LL-part		TSOP-I Standard
HY62256AR1	55/70/85			TSOP-I Reversed
HY62256ALR1	55/70/85	L-part		TSOP-I Reversed
HY62256ALLR1	55/70/85	LL-part		TSOP-I Reversed
HY62256AP-I	55/70/85		E.T.	PDIP
HY62256ALP-I	55/70/85	L-part	E.T.	PDIP
HY62256AJ-I	55/70/85		E.T.	SOP
HY62256ALJ-I	55/70/85	L-part	E.T.	SOP
HY62256AT1-I	55/70/85		E.T.	TSOP-I
HY62256ALT1-I	55/70/85	L-part	E.T.	TSOP-I
HY62256AR2-I	55/70/85		E.T.	TSOP-I Reversed
HY62256ALR2-I	55/70/85	L-part	E.T.	TSOP-I Reversed

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit	Remark
Vcc, V_{IN}, V_{OUT}	Power Supply, Input/Output Voltage	-0.5 to 7.0	V	
T_A	Operating Temperature	0 to 70	¡É	HY62256A
		-40 to 85	¡É	HY62256A-I
T_{STG}	Storage Temperature	-65 to 150	¡É	
P_D	Power Dissipation	1.0	W	
I_{OUT}	Data Output Current	50	mA	
T_{SOLDER}	Lead Soldering Temperature & Time	260•10	¡É•sec	

Note
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

T_A=0°C to 70°C / T_A= -40°C to 85°C(E.T.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	Vcc+0.5	V
V_{IL}	Input Low Voltage	-0.5(1)	-	0.8	V

Note
1. V_{IL} = -3.0V for pulse width less than 30ns

TRUTH TABLE

/CS	/WE	/OE	MODE	I/O OPERATION
H	X	X	Standby	High-Z
L	H	H	Output Disabled	High-Z
L	H	L	Read	Data Out
L	L	X	Write	Data In

Note :
1. H=V_{IH}, L=V_{IL}, X=Don't Care

DC CHARACTERISTICS

Vcc = 5V¡¾10%, T_A = 0¡É to 70¡É(Normal)/ -40¡É to 85¡É(E.T.) unless otherwise specified

Symbol	Parameter		Test Condition		Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current		Vss ¡Â V_{IN} ¡Â Vcc		-1	-	1	uA
I_{LO}	Output Leakage Current		Vss ¡Â V_{OUT} ¡Â Vcc, /CS = V_{IH} or /OE = V_{IH} or /WE = V_{IL}		-1	-	1	uA
Icc	Operating Power Supply Current		/CS = V_{IL}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA		-	30	50	mA
I_{CC1}	Average Operating Current		/CS = V_{IL}, Min. Duty Cycle = 100%, $I_{I/O}$ = 0mA		-	40	70	mA
I_{SB}	TTL Standby Current (TTL Inputs)		/CS= V_{IH} V_{IN} = V_{IH} or V_{IL}		-	0.4	2	mA
I_{SB1}	CMOS Standby Current (CMOS Inputs)	HY62256A	/CS ¡Ã Vcc - 0.2V V_{IN} ≤ 0.2V or V_{IN} ¡Ã Vcc - 0.2V		-	-	1	mA
				L	-	2	100	uA
				LL	-	1	25	uA
		HY62256A-I			-	-	1	mA
				L	-	2	100	uA
V_{OL}	Output Low Voltage		I_{OL} = 2.1mA		-	-	0.4	V
V_{OH}	Output High Voltage		I_{OH} = -1mA		2.4	-	-	V

Note : Typical values are at Vcc =5.0V, T_A = 25¡É

AC CHARACTERISTICS

Vcc = 5V¡¾10%, TA = 0¡É to 70¡É(Normal)/ -40¡É to 85¡É(E.T.) unless otherwise specified.

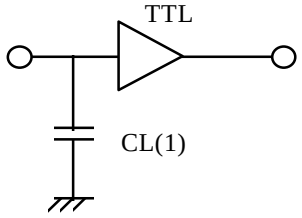
#	Symbol	Parameter	-55		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	55	-	70	-	85	-	ns
2	tAA	Address Access Time	-	55	-	70	-	85	ns
3	tACS	Chip Select Access Time	-	55	-	70	-	85	ns
4	tOE	Output Enable to Output Valid	-	30	-	35	-	45	ns
5	tCLZ	Chip Select to Output in Low Z	5	-	5	-	5	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
7	tCHZ	Chip Deselection to Output in High Z	0	20	0	30	0	30	ns
8	tOHZ	Out Disable to Output in High Z	0	20	0	30	0	30	ns
9	tOH	Output Hold from Address Change	5	-	5	-	5	-	ns
	WRITE CYCLE								
10	tWC	Write Cycle Time	55	-	70	-	85	-	ns
11	tCW	Chip Selection to End of Write	50	-	65	-	75	-	ns
12	tAW	Address Valid to End of Write	50	-	65	-	75	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	40	-	50	-	55	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	20	0	30	0	30	ns
17	tDW	Data to Write Time Overlap	25	-	35	-	40	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	5	-	ns

AC TEST CONDITIONS

TA = 0¡É to 70¡É(Normal) / -40¡É to 85¡É(E.T.) unless otherwise specified.

PARAMETER		VALUE
Input Pulse Level		0.8V to 2.4V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Levels		1.5V
Output Load	70/85/100ns	CL = 100pF + 1TTL Load
	55ns	CL = 50pF + 1TTL Load

AC TEST LOADS



Note : Including jig and scope capacitance

CAPACITANCE

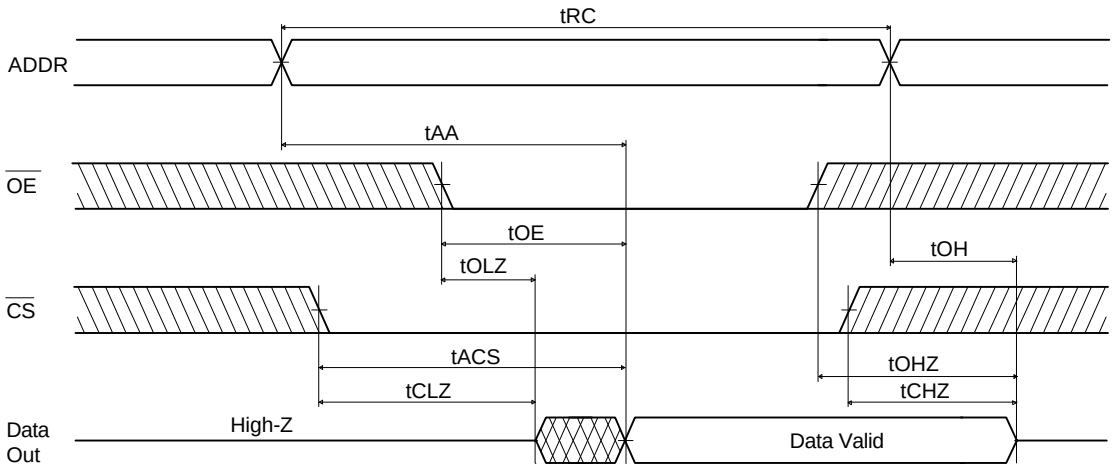
T_A = 25¡É, f = 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input /Output Capacitance	$V_{I/O}$ = 0V	8	pF

Note : These parameters are sampled and not 100% tested

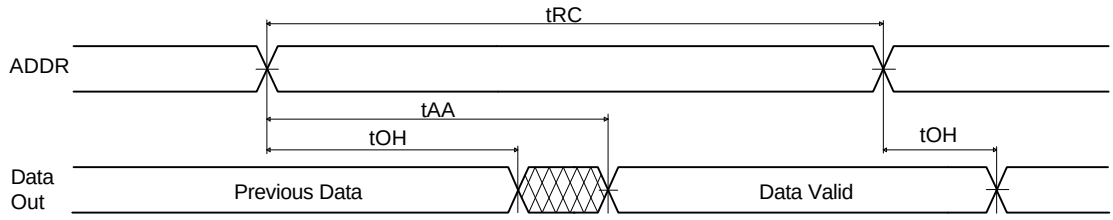
TIMING DIAGRAM

READ CYCLE 1



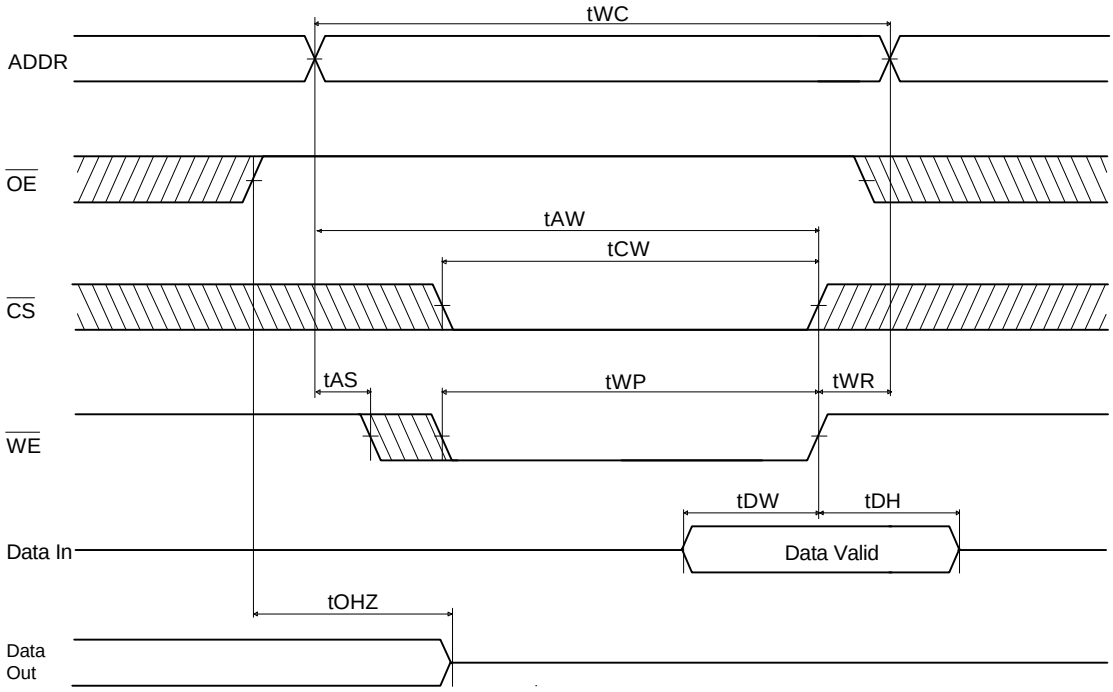
Note(READ CYCLE):
1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{CHZ} max. is less than t_{CLZ} min. both for a given device and from device to device.
3. /WE is high for the read cycle.

READ CYCLE 2

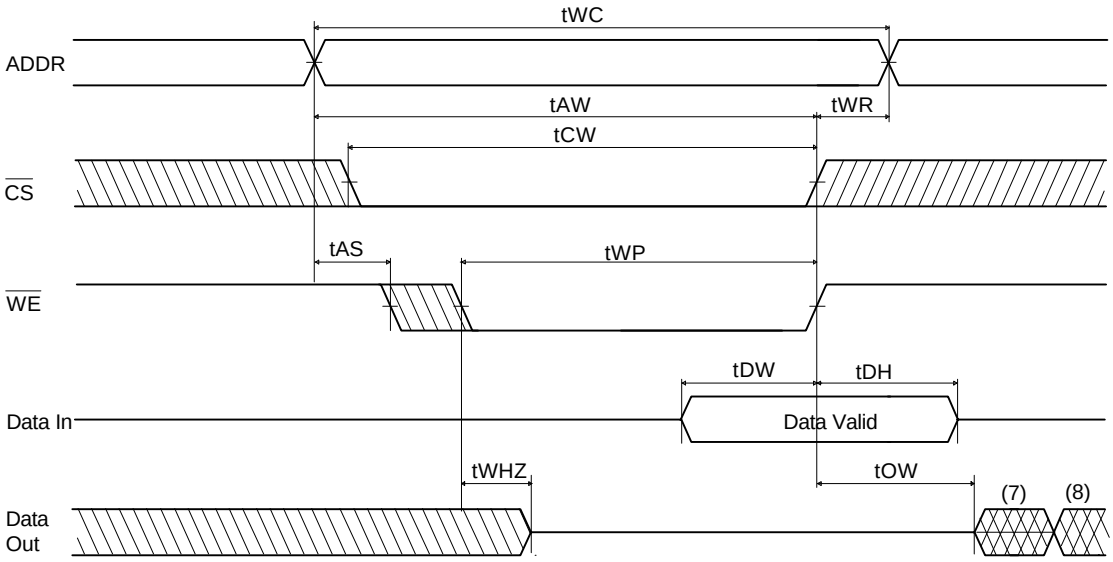


Note(READ CYCLE):
1. /WE is high for the read cycle.
2. Device is continuously selected /CS= V_{IL}.
3. /OE =V_{IL}.

WRITE CYCLE 1(/OE Clocked)



WRITE CYCLE 2 (/OE Low Fixed)



Notes(WRITE CYCLE):

1. A write occurs during the overlap of a low /CS and a low /WE. A write begins at the latest transition among /CS going low and /WE going low: A write ends at the earliest transition among /CS going high and /WE going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of /CS going low to the end of write .
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends as /CS, or /WE going high.
5. If /OE and /WE are in the read mode during this period, and the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS goes low simultaneously with /WE going low, or after /WE going low, the outputs remain in high impedance state.
7. D_{OUT} is the same phase of latest written data in this write cycle.
8. D_{OUT} is the read data of the new address.

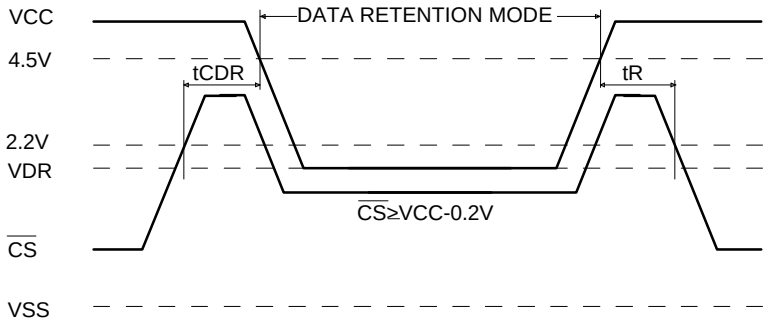
DATA RETENTION CHARACTERISTIC

TA=0°C to 70°C (normal)/-40°C to 85°C(E.T.)

Symbol	Parameter		Test Condition		Min	Typ	Max	Unit
V_{DR}	Vcc for Data Retention		/CS ¡ÃVcc-0.2V,Vss ¡ÂVIN ¡ÂVcc		2	-	-	V
I_{CCDR}	Data Retention Current	HY62256A	Vcc = 3.0V, /CS ¡ÃVcc -0.2V	L	-	1	50	uA
				LL	-	1	15(2)	uA
		HY62256A-I	Vss ¡ÂVIN ¡ÂVcc	L	-	1	50	uA
tCDR	Chip Disable to Data Retention Time		See Data Retention Timing Diagram		0	-	-	ns
tR	Operating Recovery Time				tRC(3)	-	-	ns

Notes
1. Typical values are under the condition of T_A = 25¡É.
2. 3uA max. at T_A=0¡É to 40 ¡É.
3. tRC is read cycle time.

Data Retention Timing Diagram

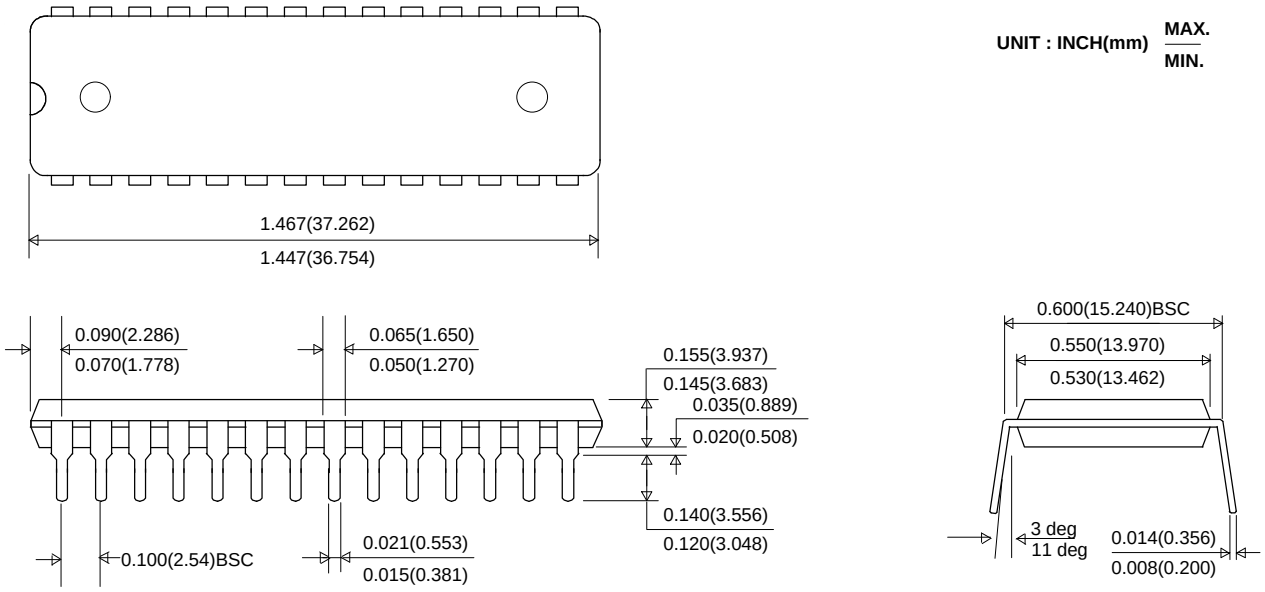


RELIABILITY SPEC.

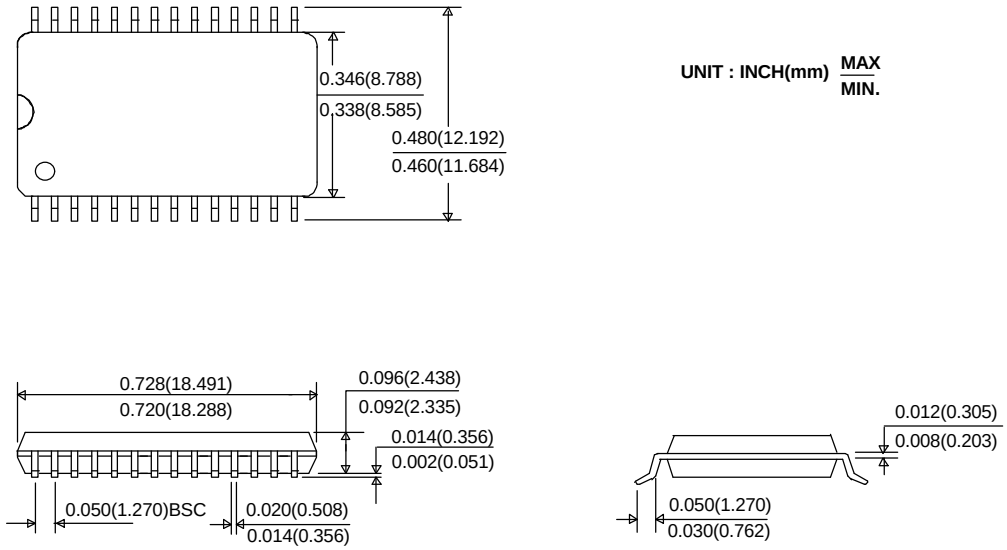
TEST MODE		TEST SPEC.
ESD	HBM	¡Ã 2000V
	MM	¡Ã 250V
LATCH - UP		¡Â -100mA
		¡Ã100mA

PACKAGE INFORMATION

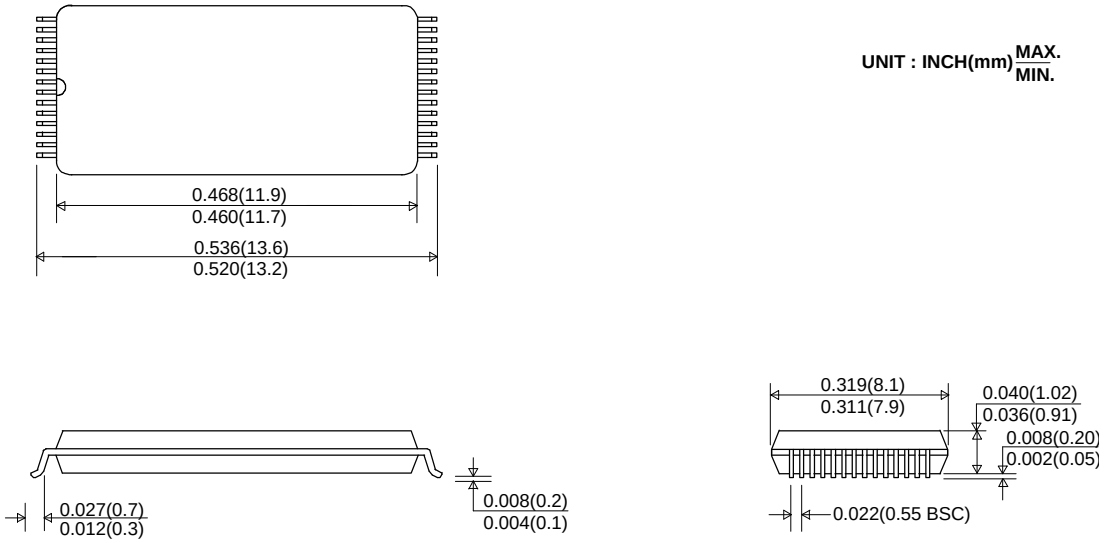
28pin 600mil Dual In-Line Package(P)



28pin 330mil Small Outline Package(J)



28pin 8x13.4mm Thin Small Outline Package Standard(T1)



28pin 8x13.4mm Thin Small Outline Package Reversed(R1)