



3.3V CMOS QUADRUPLE 2-INPUT POSITIVE-AND GATE WITH 5 VOLT TOLERANT I/O

IDT74LVC08A

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.65mm pitch SSOP and 0.65mm pitch TSSOP packages
- Extended commercial range of - 40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range
- V_{CC} = 2.3V to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC08A:

- High Output Drivers: ±24mA
- Reduced system switching noise

DESCRIPTION:

This quadruple 2-input positive-AND gate is built using advanced dual metal CMOS technology. The LVC08A device performs the Boolean function $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

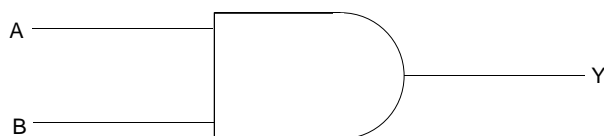
The LVC08A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

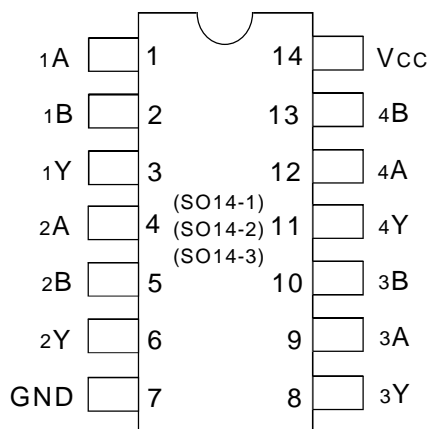
APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ SSOP/ TSSOP
TOP VIEW

FUNCTION TABLE (each gate)⁽¹⁾

| Inputs | | Outputs |
|--------|----|---------|
| xA | xB | xY |
| H | H | H |
| L | X | L |
| X | L | L |

NOTE:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

PIN DESCRIPTION

| Pin Names | Description |
|-----------|--------------|
| xA, xB | Data Inputs |
| xY | Data Outputs |

ABSOLUTE MAXIMUM RATINGS (1)

| Symbol | Description | Max. | Unit |
|------------------------------------|---|---------------|------|
| V _{TERM} | Terminal Voltage with Respect to GND | - 0.5 to +6.5 | V |
| T _{STG} | Storage Temperature | - 65 to +150 | °C |
| I _{OUT} | DC Output Current | - 50 to +50 | mA |
| I _{IK} I _{OK} | Continuous Clamp Current, V _I < 0 or V _O < 0 | - 50 | mA |
| I _{CC} I _{SS} | Continuous Current through each V _{CC} or GND | ±100 | mA |

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NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHZ)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|------------------|----------------------|-----------------------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 4.5 | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 5.5 | 8 | pF |
| C _{I/O} | I/O Port Capacitance | V _{IN} = 0V | 6.5 | 8 | pF |

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NOTE:

- As applicable to the device type.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = - 40°C to +85°C

| Symbol | Parameter | Test Conditions | | Min. | Typ.(1) | Max. | Unit |
|--|--|---|--|------|---------|-------|------|
| V _{IH} | Input HIGH Voltage Level | V _{CC} = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | V _{CC} = 2.7V to 3.6V | | 2 | — | — | |
| V _{IL} | Input LOW Voltage Level | V _{CC} = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | V _{CC} = 2.7V to 3.6V | | — | — | 0.8 | |
| I _{IH} I _{IL} | Input Leakage Current | V _{CC} = 3.6V | V _I = 0 to 5.5V | — | — | ±5 | µA |
| I _{OZH} I _{OZL} | High Impedance Output Current (3-State Output pins) | V _{CC} = 3.6V | V _O = 0 to 5.5V | — | — | ±10 | µA |
| I _{OFF} | Input/Output Power Off Leakage | V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V | | — | — | ±50 | µA |
| V _{IK} | Clamp Diode Voltage | V _{CC} = 2.3V, I _{IN} = - 18mA | | — | - 0.7 | - 1.2 | V |
| V _H | Input Hysteresis | V _{CC} = 3.3V | | — | 100 | — | mV |
| I _{CC1} I _{CC2} I _{CC3} | Quiescent Power Supply Current | V _{CC} = 3.6V | V _{IN} = GND or V _{CC} | — | — | 10 | µA |
| ΔI _{CC} | Quiescent Power Supply Current Variation | One input at V _{CC} - 0.6V other inputs at V _{CC} or GND | | — | — | 500 | µA |

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NOTE:

- Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Max. | Unit |
|--------|---------------------|--------------------------------|--------------|-----------|------|------|
| VOH | Output HIGH Voltage | VCC = 2.3V to 3.6V | IOH = -0.1mA | VCC - 0.2 | — | V |
| | | VCC = 2.3V | IOH = -6mA | 2 | — | |
| | | VCC = 2.3V | IOH = -12mA | 1.7 | — | |
| | | VCC = 2.7V | | 2.2 | — | |
| | | VCC = 3.0V | | 2.4 | — | |
| | | VCC = 3.0V | IOH = -24mA | 2.2 | — | |
| VOL | Output LOW Voltage | VCC = 2.3V to 3.6V | IOL = 0.1mA | — | 0.2 | V |
| | | VCC = 2.3V | IOL = 6mA | — | 0.4 | |
| | | | IOL = 12mA | — | 0.7 | |
| | | VCC = 2.7V | IOL = 12mA | — | 0.4 | |
| | | VCC = 3.0V | IOL = 24mA | — | 0.55 | |

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NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = -40°C to +85°C.

OPERATING CHARACTERISTICS, TA = 25°C

| Symbol | Parameter | Test Conditions | VCC = 2.5V±0.2V | VCC = 3.3V±0.3V | Unit |
|--------|--|---------------------|-----------------|-----------------|------|
| | | | Typical | Typical | |
| CPD | Power dissipation capacitance per gate | CL = 0pF, f = 10Mhz | — | 10 | pF |

SWITCHING CHARACTERISTICS ⁽¹⁾

| Symbol | Parameter | VCC = 2.7V | | VCC = 3.3V±0.3V | | Unit |
|--------|-------------------------------------|------------|------|-----------------|------|------|
| | | Min. | Max. | Min. | Max. | |
| tPLH | Propagation Delay xA or xB to xY | — | 4.8 | 1 | 4.1 | ns |
| tPHL | | | | | | |
| tSK(0) | Output Skew ⁽²⁾ | — | — | — | 1 | ns |

NOTES:

1. See test circuits and waveforms. TA = -40°C to +85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

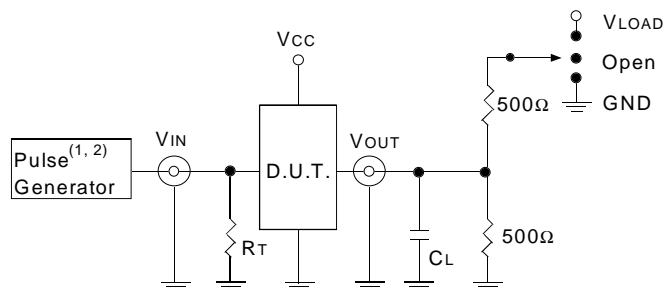
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

| Symbol | V _{cc} (1)= 2.5V ±0.2V | V _{cc} (2)= 3.3V ±0.3V & 2.7V | Unit |
|-------------------|---------------------------------|--|------|
| V _{LOAD} | 2 x V _{cc} | 6 | V |
| V _{IH} | V _{cc} | 2.7 | V |
| V _T | V _{cc} / 2 | 1.5 | V |
| V _{LZ} | 150 | 300 | mV |
| V _{HZ} | 150 | 300 | mV |
| C _L | 30 | 50 | pF |

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

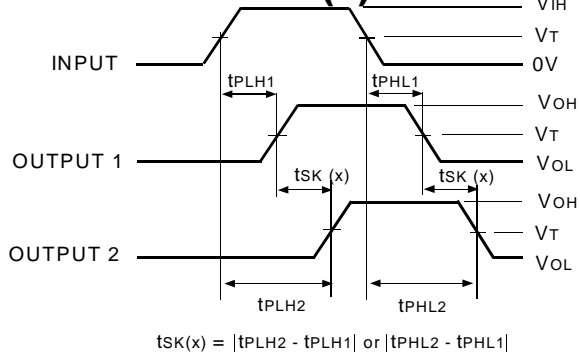
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.

SWITCH POSITION

| Test | Switch |
|---|-------------------|
| Open Drain Disable Low Enable Low | V _{LOAD} |
| Disable High Enable High | GND |
| All Other tests | Open |

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OUTPUT SKEW - t_{SK}(x)

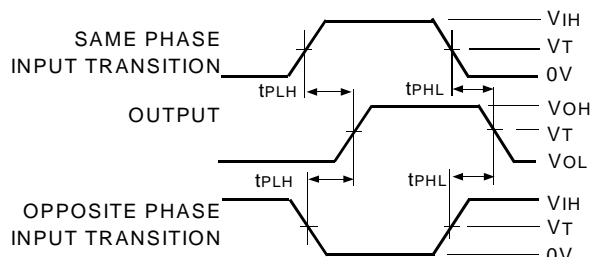


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NOTES:

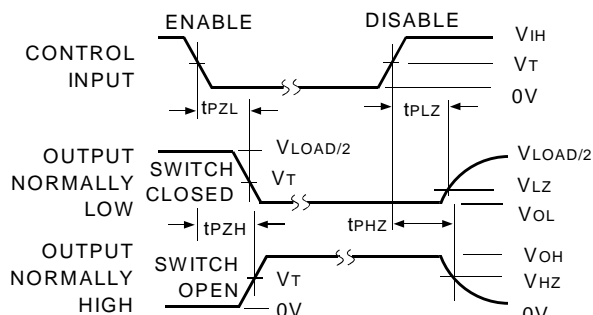
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

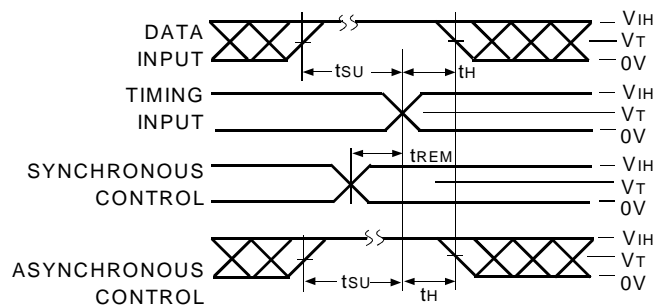


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NOTE:

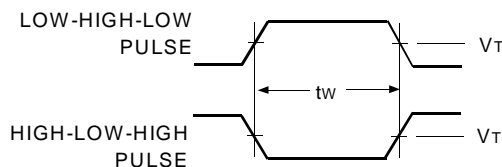
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



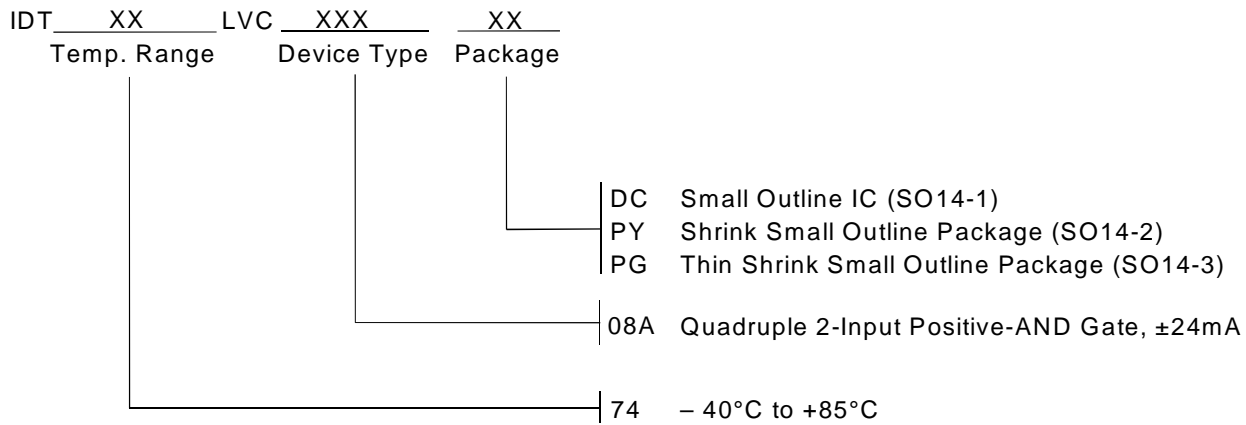
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PULSE WIDTH



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ORDERING INFORMATION



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com*

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