9M and 4.5M Integrated IP Co-Processors (IIPC) with Quad AMCC XSC Interface

Advanced Information
IDT75K62413
IDT75K52413

To request the full application note, please contact your local IDT Sales Representative or call 1-831-754-4555

Introduction

Evolving network speeds require critical functions such as forwarding and classification to migrate towards dedicated hardware devices. The Integrated IP Co-Processor (IIPC) based on IDT's CAM (Content Addressable Memory) technology accelerates search functions required for applications such as Access Control Lists (ACL), Flow Caching and Forwarding in systems using AMCC Network Processors.

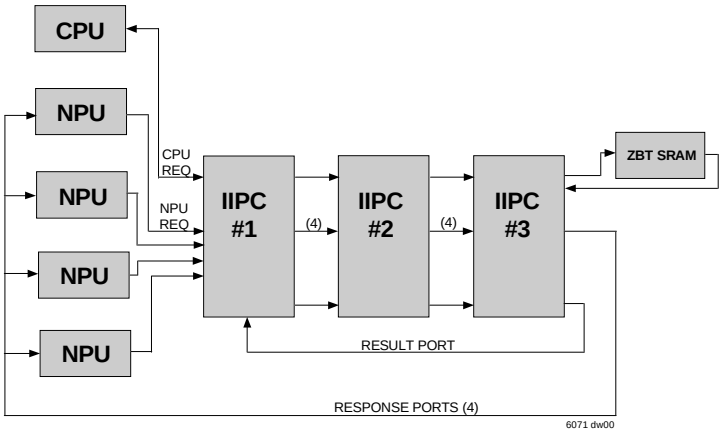
Device Description

The IIPC Quad AMCC XSC interface is intended to work with any AMCC NPU with an external search co-processor interface (XSC). It will operate with multiple NPUs such as the nP3400 and nP7250, or can be used to satisfy the four XSC requirements of the nP7510. The 75K62413 is compliant with the AMCC XSC specification. The 75K62413 device may be optionally expanded up to eight devices deep providing 2 million entries of 32-bit width.

Features

- 128K x 72 (9M) or 64K x 72 (4.5M) Data and Mask cells
- Full Ternary Content Addressable Memory
- Advanced Database Management
  - Selectable Databases
  - Programmable Width per Database
  - Lookup widths from 32 to 512 bits
  - Only the selected Database is powered
- Maintenance Instructions
  - Aging
  - Multi Hit Invalidate
  - Learn per Database
- Support for Multiple Contexts
- Pool of Global Mask Registers
- Control and Management
  - 32-bit Host control port featuring glueless PPC interface
  - Capable of In-Band Control and Management
- Associated Data SRAM is supported through a glueless ZBT® interface
- Lowest Power per Application
- Synchronous Pipeline Operation
- Boundary Scan JTAG Interface
- 1.2V Core Supply
- 3.3V I/O Supply for XSC I/O and ZBT® SRAM

Figure 1.0 AMCC NPU Interface



Note: May be expanded up to 8 IIPC devices

APRIL 2002