International
IOR Rectifier

The IR1210 part number has been updated and changed to IR4426/IR4427/IR4428 Please see new data sheet

Data Sheet No. PD60165-C

IR1210

DUAL LOW SIDE DRIVER

Features

- Gate drive supply range from 6 to 20V
- CMOS Schmitt-triggered inputs with pull-up
- Matched propagation delay for both channels
- Outputs out of phase with inputs

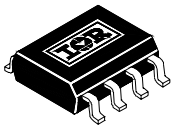
Description

The IR1210 is a low voltage, high speed power MOSFET and IGBT driver. Proprietary latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays between two channels are matched.

Product Summary

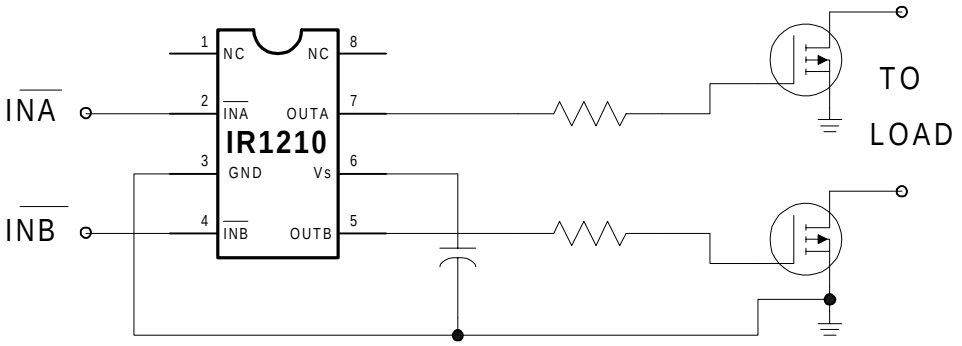
I_O+/-	1.5A / 1.5A
V_{OUT}	6V - 20V
$t_{on/off}$ (typ.)	85 & 65 ns

Package



8 Lead SOIC

Block Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_S	Fixed supply voltage	-0.3	25	V
V_O	Output voltage -0.3	V_S + 0.3		
V_{IN}	Logic input voltage (INA/N & INB/N)	-0.3	V_S + 0.3	
P_D	Package power dissipation @ $T_A \leq +25°C$	—	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient	—	200	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND.

Symbol	Definition	Min.	Max.	Units
V_S	Fixed supply oltage	6	20	V
V_O	Output voltage	0	V_S	
V_{IN}	Logic input voltage (INA/N & INB/N)	0	V_S	
T_A	Ambient temperature	-40	125	°C

DC Electrical Characteristics

V_{BIAS} (V_S) = 15V, T_A = 25°C unless otherwise specified. The V_{IN}, and I_{IN} parameters are referenced to GND and are applicable to input leads: INA/N and INB/N. The V_O and I_O parameters are referenced to GND and are applicable to the output leads: OUTA and OUTB.

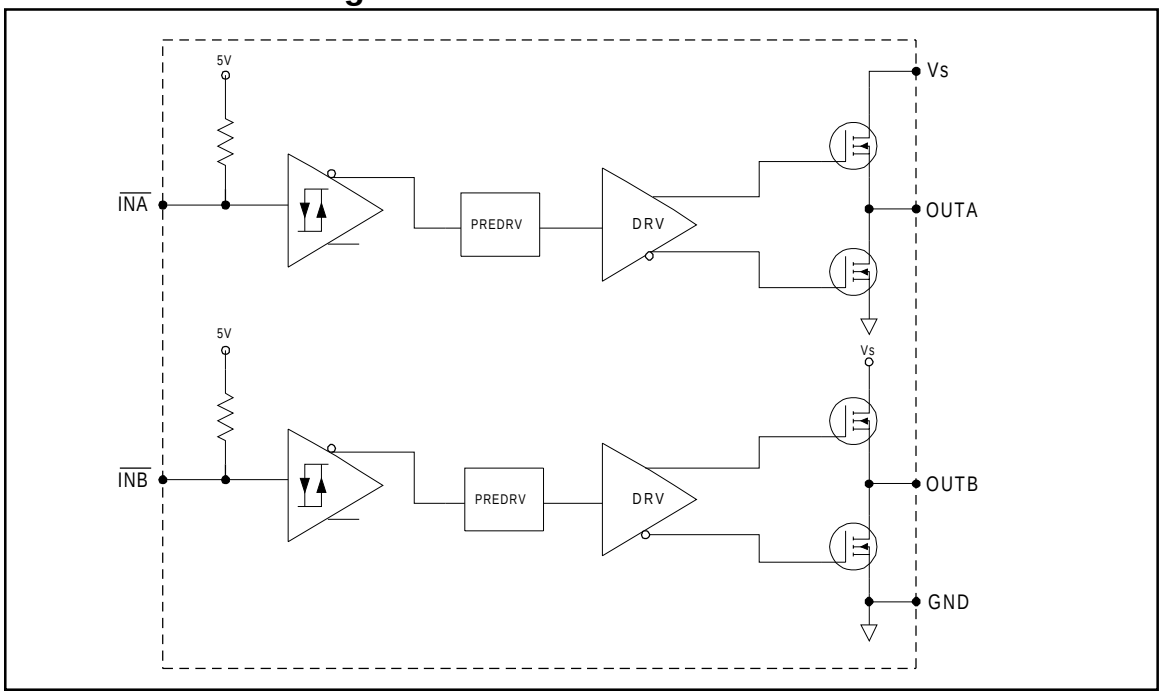
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “0” input voltage (OUT=LO)	2.7	—	—	V	
V_{IL}	Logic “1” input voltage (OUT=HI)	—	—	0.8		
V_{OH}	High level output voltage, V_{BIAS}-V_O	—	—	1.2		
V_{OL}	Low level output voltage, V_O	—	—	0.1		
I_{IN+}	Logic “1” input bias current (OUT=HI)	—	5	15	µA	V_{IN} = 0V
I_{IN-}	Logic “0” input bias current (OUT=LO)	—	-10	-30		V_{IN} = V_S
I_{QS}	Quiescent Vs supply current	—	100	200		V_{IN} = 0V or V_S
I_{O+}	Output high short circuit pulsed current	1.5	2.3	—	A	V_O = 0V, V_{IN} = 0 PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	1.5	3.3	—		V_O = 15V, V_{IN} = V_S PW ≤ 10 µs

Dynamic Electrical Characteristics

V_{BIAS} (V_S) = 15V, C_L = 1000 pF, T_A = 25°C unless otherwise specified.

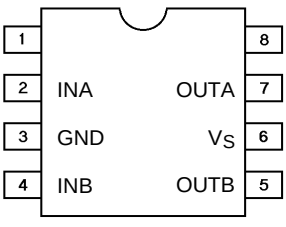
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{d1}	Turn-on propagation delay	—	85	160	ns	figures 2 & 3
t_{d2}	Turn-off propagation delay	—	65	150		
t_r	Turn-on rise time	—	15	35		
t_f	Turn-off fall time	—	10	25		

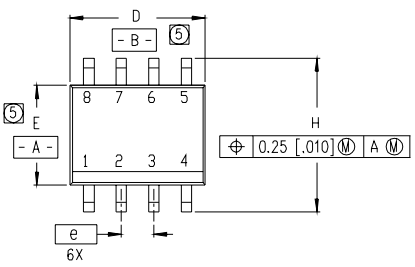
Functional Block Diagram

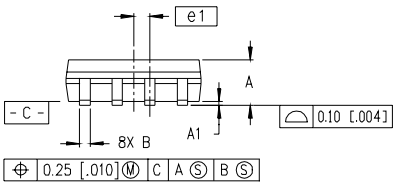


Lead Assignment and Definitions

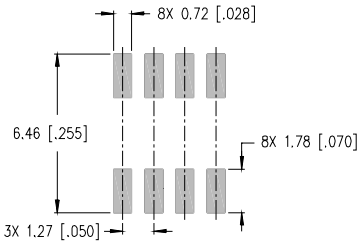
Symbol	Description
V_S	Supply voltage
GND	Ground
INA	Logic input for gate driver output (OUTA), out of phase
INB	Logic input for gate driver output (OUTB), out of phase
OUTA	Gate drive output A
OUTB	Gate drive output B

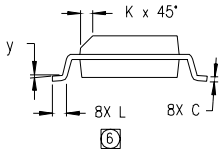






RECOMMENDED FOOTPRINT





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

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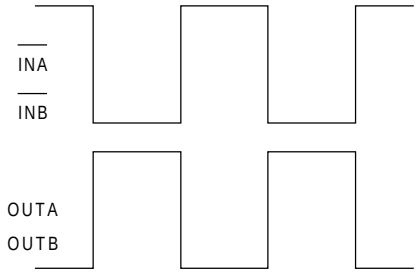

Figure 1. Timing Diagram

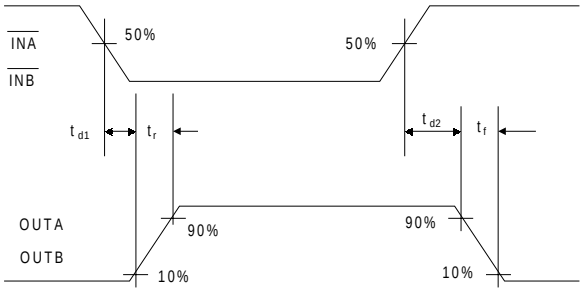

Figure 2. Switching Time Waveforms

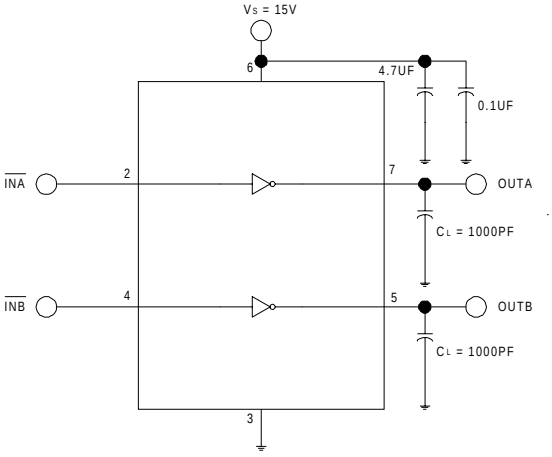

Figure 3. Switching Time Test Circuit