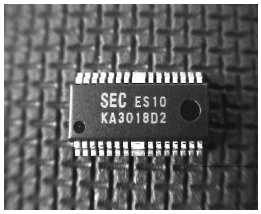
3-CH MOTOR DRIVER

The KA3018D2 is a monolithic integrated circuit, suitable for a 3-ch motor driver which drives focus actuator, tracking actuator, and sled motor of a CD system.

28-SSOPH-300



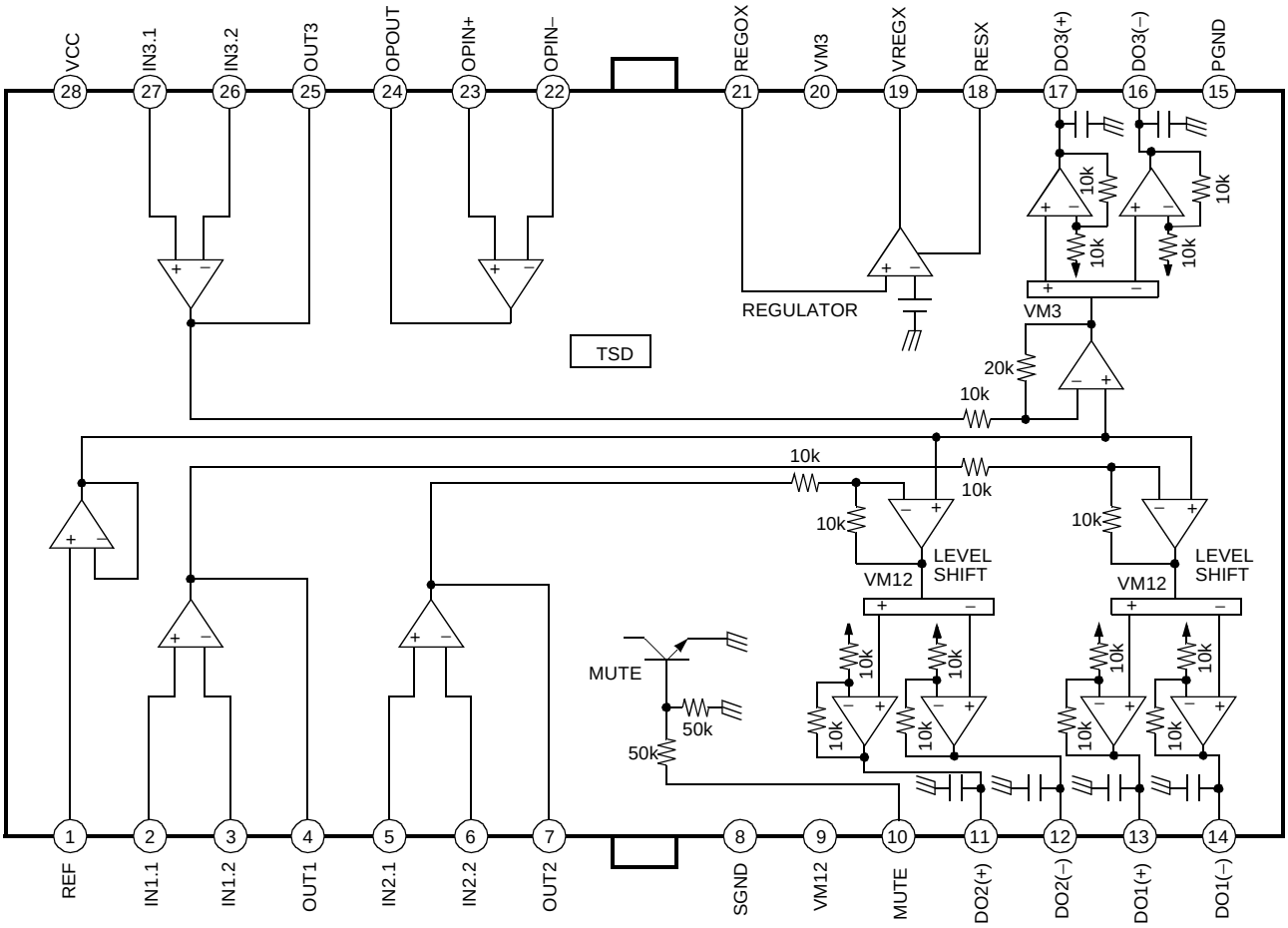
FEATURES

- 3-Channel BTL (Balanced transformer-less) driver
- Built-in variable regulator with reset (Series-REG)
- Built-in thermal shutdown circuit
- Built-in mute circuit
- Built-in normal op-amp
- Operating supply voltage: 4.5 ~ 5.5V
- Corresponds to 3.3V or 5V DSP

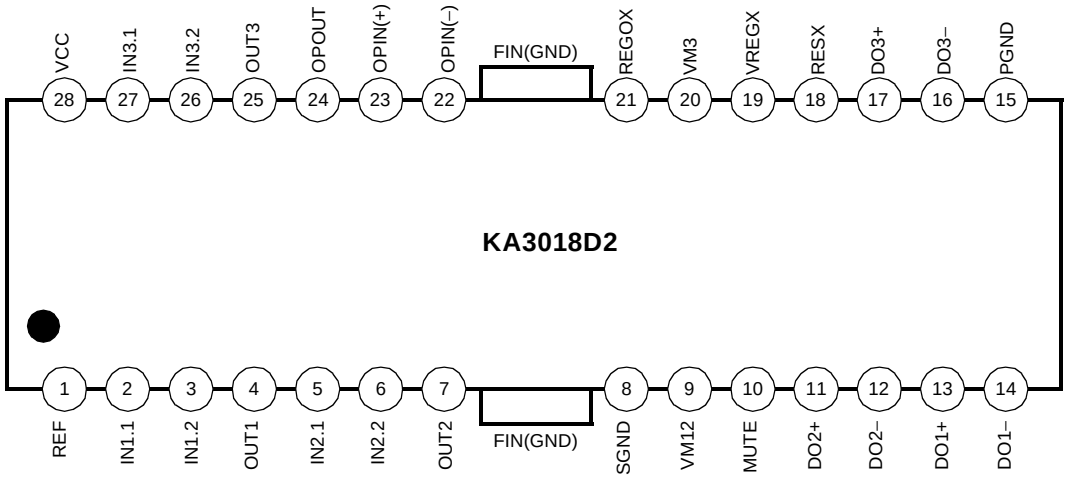
ORDERING INFORMATION

Device	Package	Operating Temperature
KA3018D2	28-SSOPH-300	–35°C ~ +85°C

BLOCK DIAGRAM



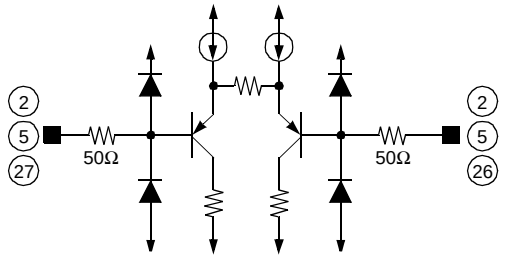
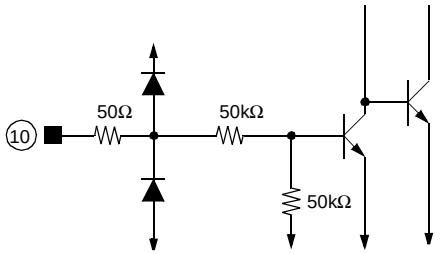
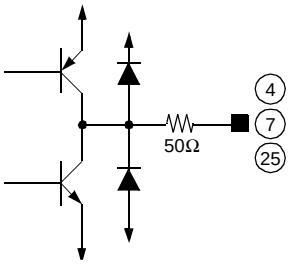
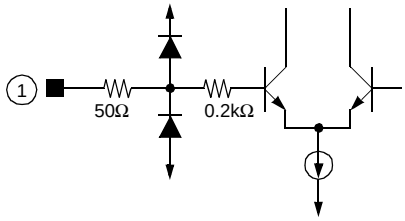
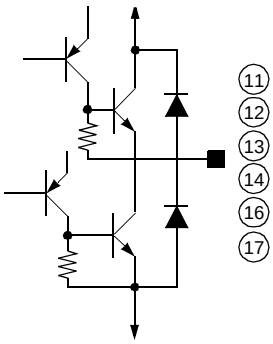
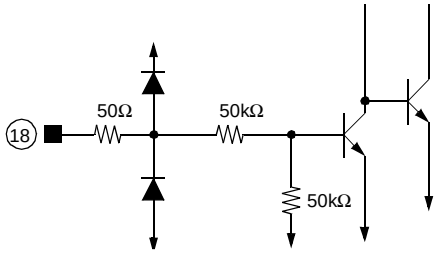
PIN CONFIGURATION



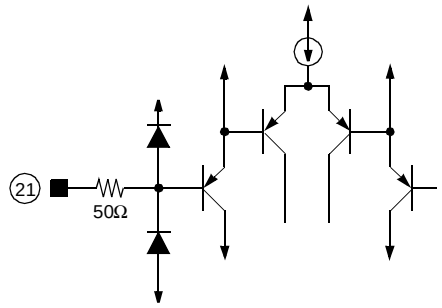
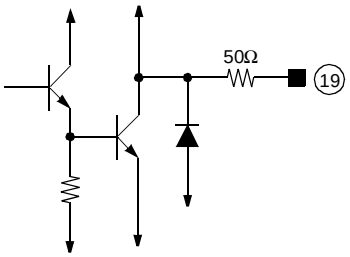
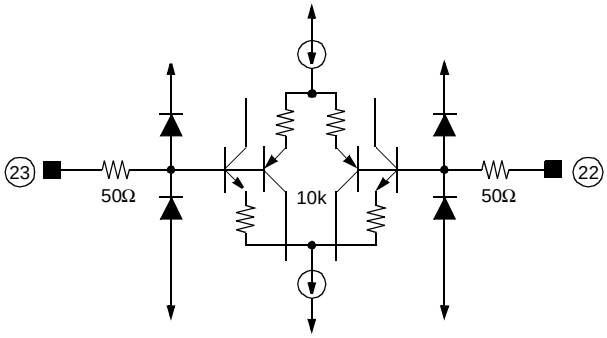
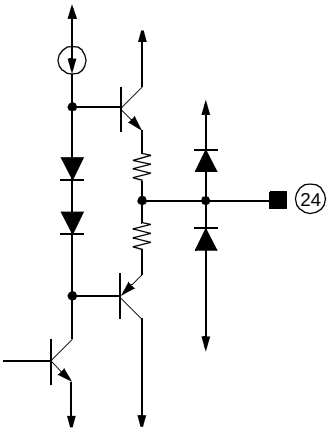
PIN DESCRIPTION

Pin No.	Symbol	I/O	Description	Pin No.	Symbol	I/O	Description
1	REF	I	Bias voltage input	15	PGND	–	Power ground
2	IN1.1	I	Op-amp CH1 input (+)	16	DO3–	O	Drive3 output (–)
3	IN1.2	I	Op-amp CH1 input (–)	17	DO3+	O	Drive3 output (+)
4	OUT1	O	Op-amp CH1 output	18	RESX	I	Regulator reset
5	IN2.1	I	Op-amp CH2 input (+)	19	VREGX	O	Regulator output
6	IN2.2	I	Op-amp CH2 input (–)	20	VM3	–	BTL CH3 supply VTG
7	OUT2	O	Op-amp CH2 output	21	REGOX	I	Regulator
8	SGND	–	Signal ground	22	OPIN(–)	I	Op-amp input (–)
9	VM12	–	BTL CH1, 2 supply VTG	23	OPIN(+)	I	Op-amp input (+)
10	MUTE	I	Mute	24	OPOUT	O	Op-amp output
11	DO2+	O	Drive2 output (+)	25	OUT3	O	Op-amp CH3 output
12	DO2–	O	Drive2 output (–)	26	IN3.2	I	Op-amp CH3 input (–)
13	DO1+	O	Drive1 output (+)	27	IN3.1	I	Op-amp CH3 input (+)
14	DO1–	O	Drive1 output (–)	28	VCC	–	Supply voltage

EQUIVALENT CIRCUITS

Error amp input	Mute input
	
Error amp output	**Signal reference input**
	
Power output	**Regulator reset**
	

EQUIVALENT CIRCUITS (Continued)

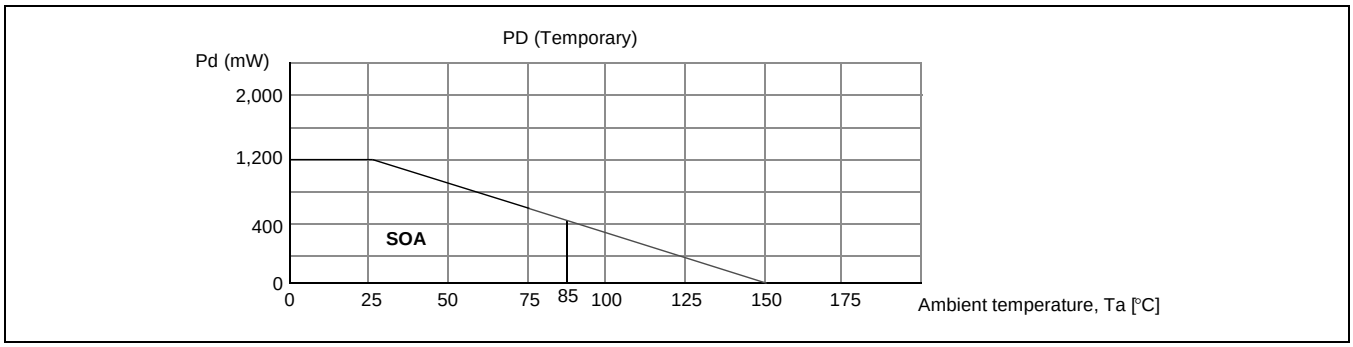
Regulator	Regulator output
	
General op amp input	**Normal op amp output**
	

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Characteristics	Symbol	Value	Unit
Maximum supply voltage	V_{CCMAX}	18	V
Power dissipation	P_D	1.5 note	W
Operating temperature range	T_{OPR}	–35 ~ +85	°C
Storage temperature range	T_{STG}	–55 ~ +150	°C

NOTE:

1. When mounted on a 76.2mm × 114mm × 1.57mm PCB (Phenolic resin material).
2. Power dissipation reduces 12mW/°C for using above Ta = 25°C
3. Do not exceed Pd and SOA (Safe operating area).
4. This is a temporary result.



RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	–	5.5	V

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=25°C, V_{CC}=VM12=VM3=5V)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Quiescent current	I_{CC}	V_{IN}=0V	–	8	12	mA
Mute on current	I_{MUTE}	Mute pin=GND	–	1	3	mA
Mute on voltage	V_{MON}	–	–	–	0.5	V
Mute off voltage	V_{MOFF}	–	2	–	–	V
BTL DRIVE PART						
Input offset voltage	V_{IO}	–	–20	–	+20	mV
Output offset voltage	V_{OO}	V_{IN}=2.5V	–20	–	+20	mV
Maximum output voltage 1	V_{OM1}	V_{CC}=5V, R_L=8Ω (CH1, 2)	2.7	3.4	–	V
Maximum output voltage 2	V_{OM2}	V_{CC}=5V, R_L=24Ω (CH3)	3	3.8	–	V
Close loop voltage gain 1	G_{VC1}	f=1kHz, V_{IN}=0.1V_{RMS} (CH1, 2)	10.5	12	13.5	dB
Close loop voltage gain 2	G_{VC2}	f=1kHz, V_{IN}=0.1V_{RMS} (CH3)	16	18	20	dB
Ripple rejection ratio	RR	V_{IN}=0.1V_{RMS}, f=120Hz	–	60	–	dB
Slew rate	SR	V_O=2Vp-p, f=120kHz	–	0.8	–	V/µs
GENERAL OP AMP PART						
Input offset voltage	V_{OFOP}	–	–10	–	+10	mV
Input bias current	I_{BOP}	–	–	–	300	nA
High level output voltage	V_{OHOP}	V_{CC}=5V, R_L=1kΩ	3	4	–	V
Low level output voltage	V_{OLOP}	V_{CC}=5V, R_L =1kΩ	0.7	1	1.3	V
Output sink current	I_{SINK}	V_{CC}=5V, R_L= 50Ω	5	10	–	mA
Output source current	I_{SOURCE}	V_{CC}=5V, R_L=50Ω	5	10	–	mA
Open loop voltage gain	G_{VO}	V_{IN}=–75dB, f=1kHz	–	75	–	dB
Ripple rejection ratio	RR_{OP}	V_{IN}=–20dB, f =120Hz	–	65	–	dB
Slew rate	SR_{OP}	f=120kHz, 2Vp-p	–	1	–	V/µs
Common mode rejection ratio	CMRR	V_{IN}=–20dB, f=1kHz	–	80	–	dB
Common mode input range	V_{ICM}	V_{CC}=5V	–0.3	–	4.5	V

ELECTRICAL CHARACTERISTICS (Continued)

(Unless otherwise specified, Ta=25°C, V_{CC}=VM12=VM3=5V)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
ERROR AMP PART						
Input offset voltage	V_{OFOP}	–	–10	–	+10	mV
Input bias current	I_{BOP}	–	–	–	300	nA
High level output voltage	V_{OFOP}	V_{CC}=5V, R_L=10kΩ	4.5	4.8	–	V
Low level output voltage	I_{BOP}	V_{CC}=5V, R_L =10kΩ	–	0.2	0.5	V
Output sink current	V_{SINK}	V_{CC}=5V, R_L= 1kΩ	1	2	–	mA
Output source current	V_{SOURCE}	V_{CC}=5V, R_L=1kΩ	1	2	–	mA
Slew rate	SR_{OP}	f=120kHz, 2Vp-p	–	1	–	V/µs
VARIABLE REGULATOR PART						
Regulator output voltage	Vreg	IL=100mA	3.0	–	4.5	V
Load regulation	ΔV_{R1}	IL=0→200mA	–40	–	10	mV
Line regulation	ΔV_{CC}	IL=200mA, V_{CC}=5→8V	–20	–	30	mV

APPLICATION INFORMATION

1. REFERENCE INPUT & ALL MUTE FUNCTION

Pin 1 (REF) is a reference input pin.

- Reference input
  The applied voltage at the reference input pin must be between 1.5V and 3.5V, when V_{CC}=5V.
- Mute input
  The following input conditions must be satisfied for the normal mute function.

All mute on voltage	Below 0.5V	Mute function operation
All mute off voltage	Above 2V	Normal operation

2. PROTECTION FUNCTION

Thermal shutdown (TSD)

- If the chip temperature rises above 175°C, the thermal shutdown (TSD) circuit is activated and the output circuit is in the mute state, that is off state.

3. REGULATOR & RESET FUNCTION

The regulator configuration with the external components is illustrated in figure 1.

- The external circuit is composed of the KSB772 PNP transistor and a capacitor about 33μF, and two feedback resistors R1, R2.
  The capacitor operates both as a ripple eliminator and as compensation of the feedback loop.
- The output voltage (REG OUT) is

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \times 25 = 5[V] \quad \text{(Where R1 = R2)}$$

- When the voltage of pin 18 (Vreset) is 0V, the regulator reset function is activated, and the output voltage (REG OUT) becomes 0V. Otherwise, if the voltage of pin 18 is 5V, the regulator operates properly.

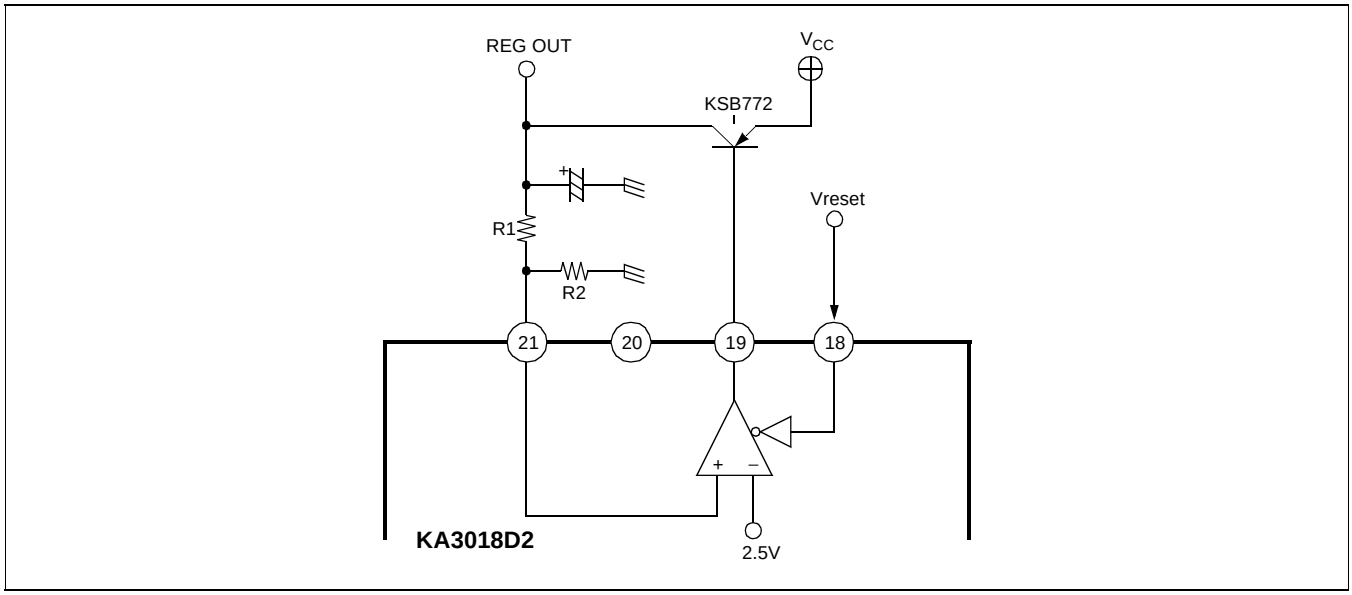


Figure 1. Regulator circuit

4. FOCUS / TRACKING ACTUATOR SLED MOTOR DRIVE PART

- The reference voltage, REF is given externally through pin 1.
- The error amp output signal is amplified by R2/R1 times and then fed to the level shift circuit.
- The level shift circuit produces the differential output voltages and drives the two output power amplifiers. Since the differential gain of the output amplifiers is equal to 2 × (1+ R4/R3), the output signal of the error amp is amplified by (R2 / R1) × 2 × (1 + R4 / R3).
- If the total gain is insufficient, the input error amp can be used to increase the gain.
- The bias voltage is about half of the power supply voltage (VM).

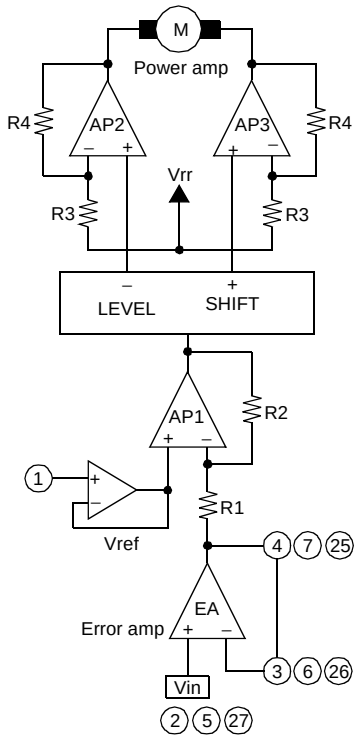
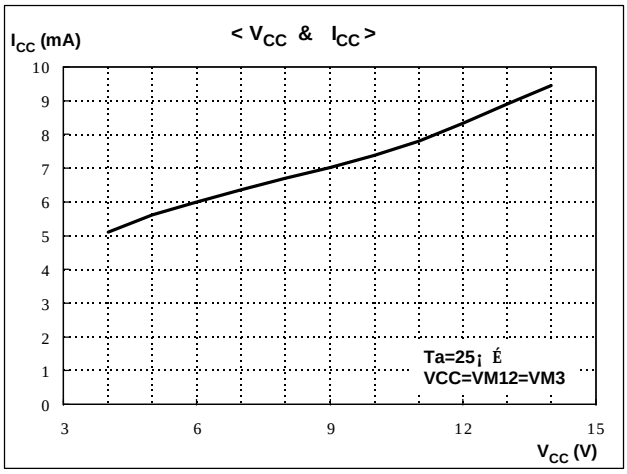
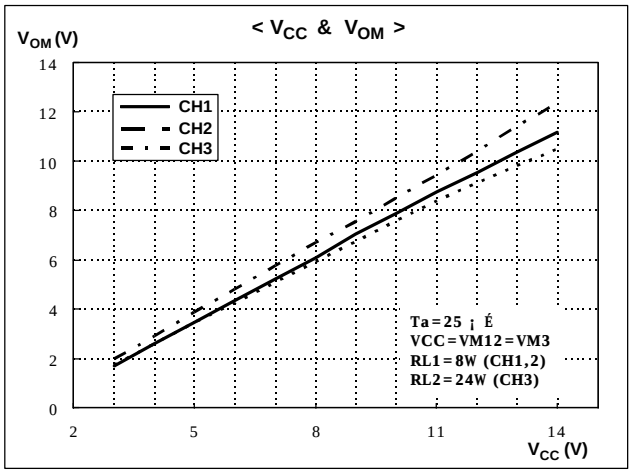
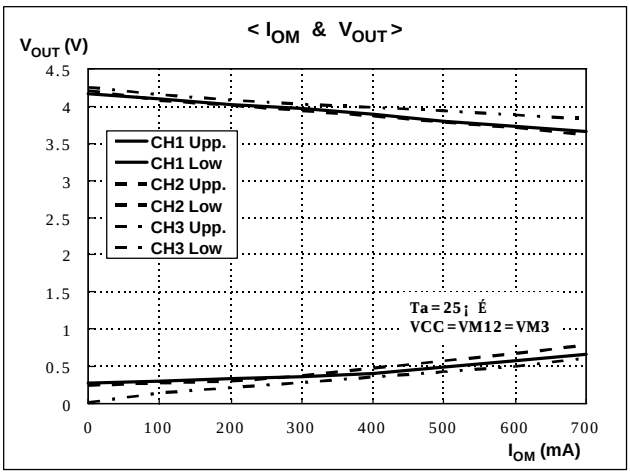


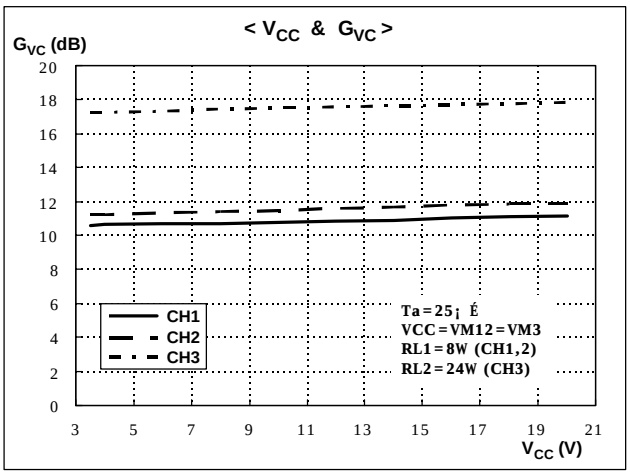
Figure 2. BTL drive circuit

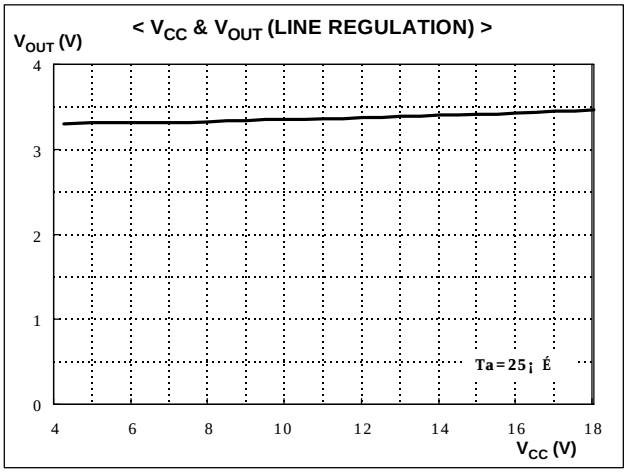
ELECTRICAL CHARACTERISTICS CURVES

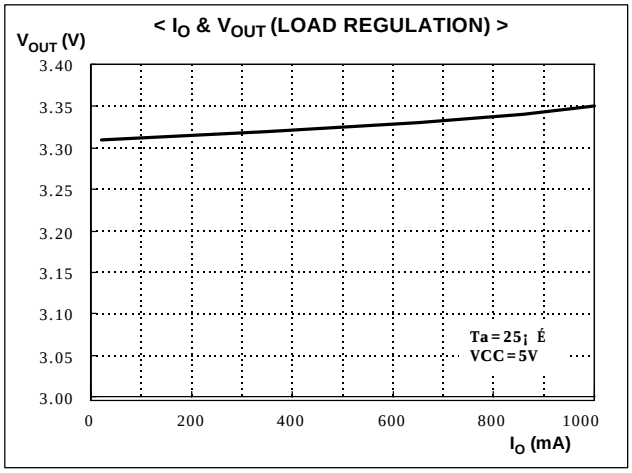




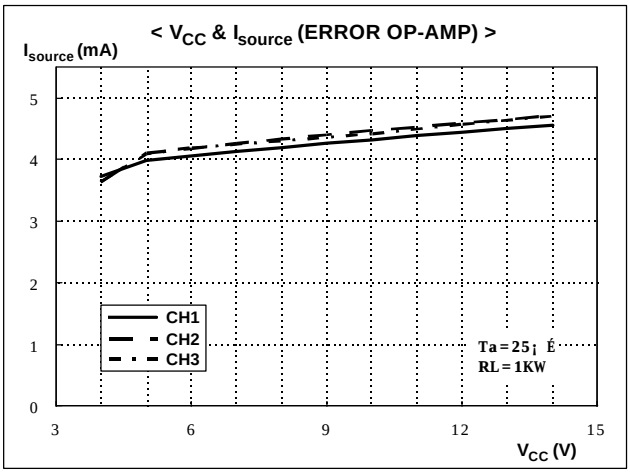


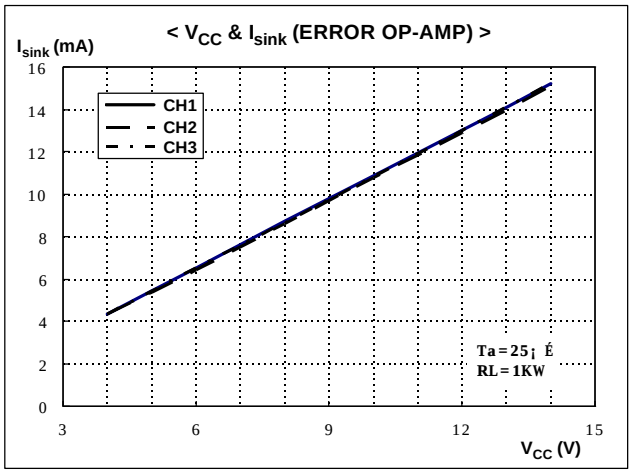


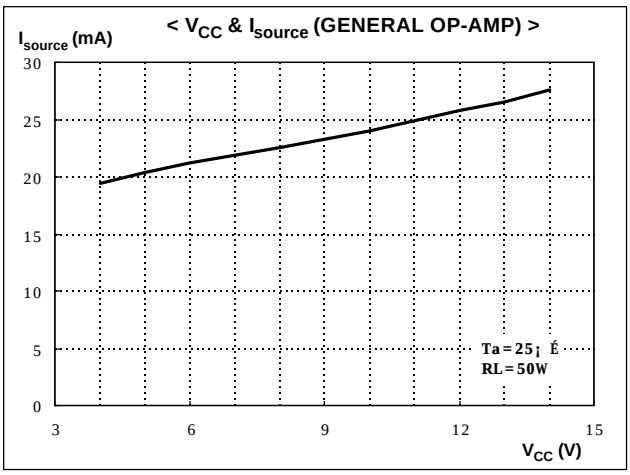


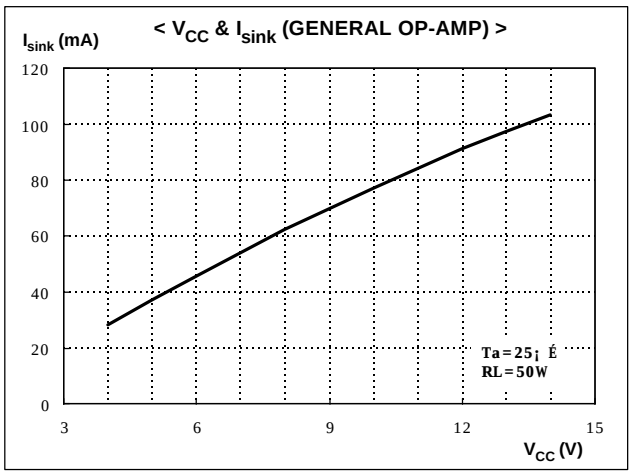


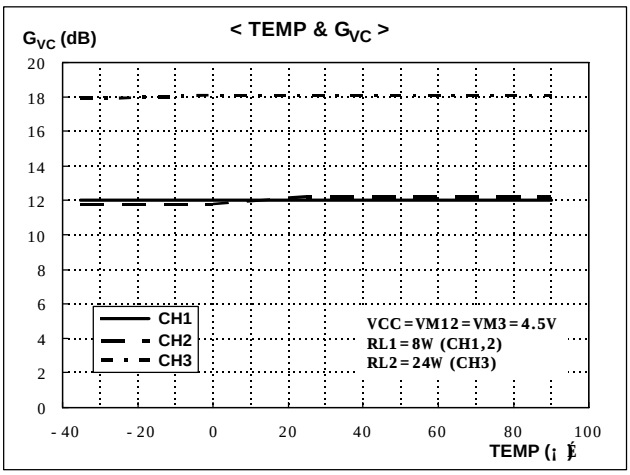
ELECTRICAL CHARACTERISTICS CURVES (Continued)

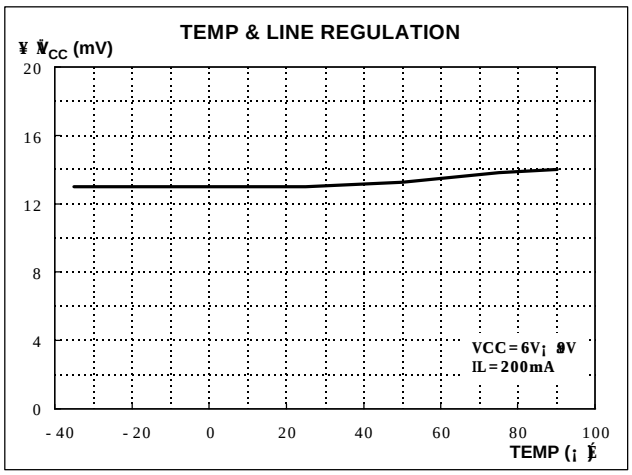






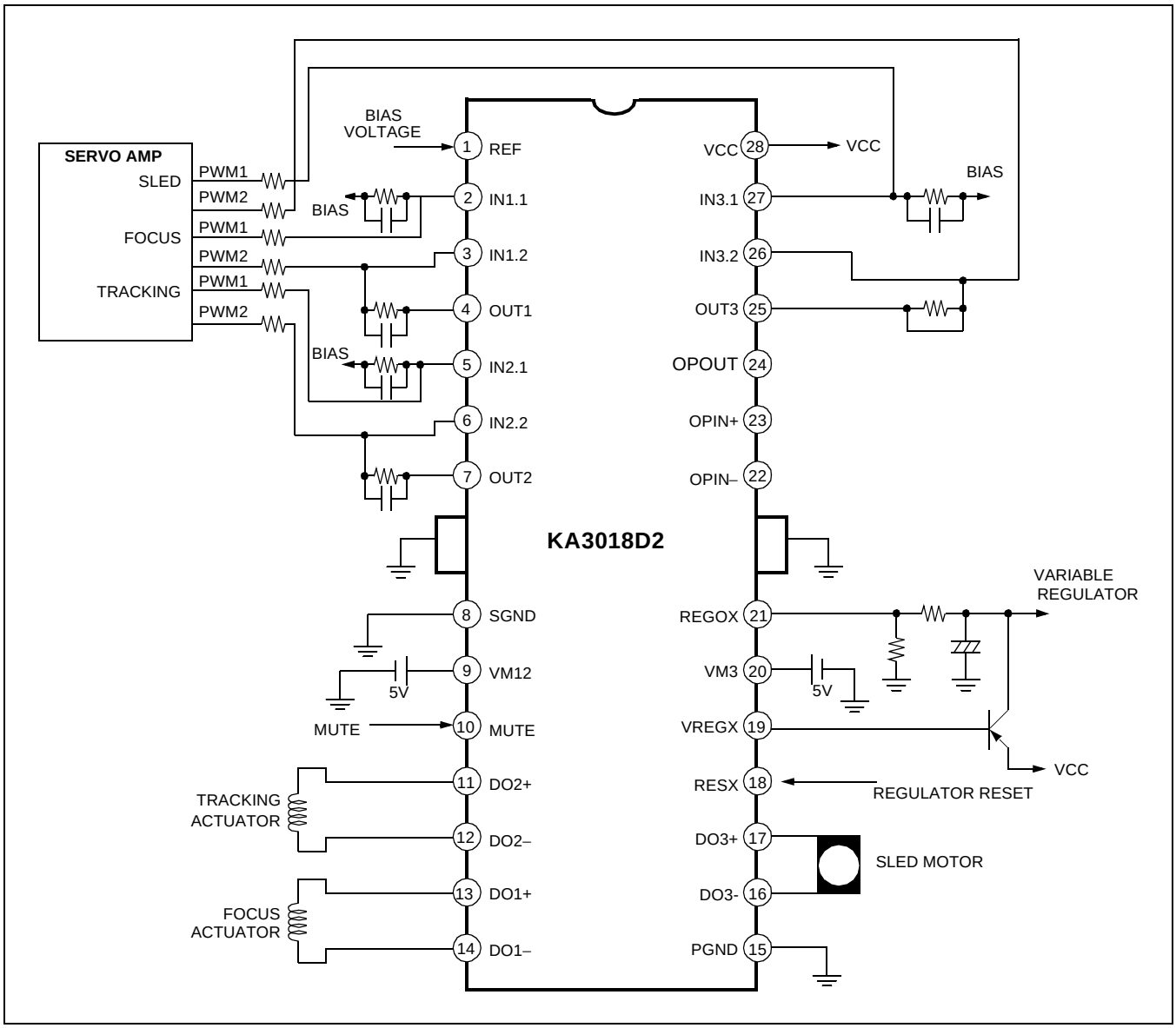






APPLICATION CIRCUIT 1

(Diffential PWM control mode)



THERMAL SHUT DOWN CIRCUIT

The IC is broken down by the heat when overload condition continues for a long time. So, KA3018D2 has a thermal shut down circuit to prevent this case. At that time temperature of the IC rises over 175°C, the circuit is operating and protects the IC against breakdown.

PACKAGE DIMENSIONS

28-SSOPH-300