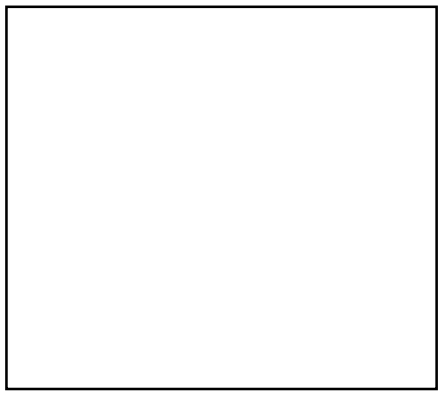
6-CH MOTOR DRIVER

The KA3031 is a monolithic integrated circuit suitable for a 6-ch motor driver which drives the tracking actuator, focus actuator, sled motor, tray motor, change motor and spindle motor of the CDP/CAR-CD systems.



FEATURES

- 4-CH balanced transformerless (BTL) driver
- 2-CH (forward - reverse) control DC motor driver
- Operating supply voltage (4.5 V ~ 16 V)
- Built-in thermal shut down circuit (TSD)
- Built-in under voltage lockout circuit (UVLO)
- Built-in over voltage protection circuit (OVP)
- Built-in MUTE circuit (CH1, CH2, CH3 and CH4)
- Built-in NORMAL OP-AMP
- Built-in 5 V regulator with RESET

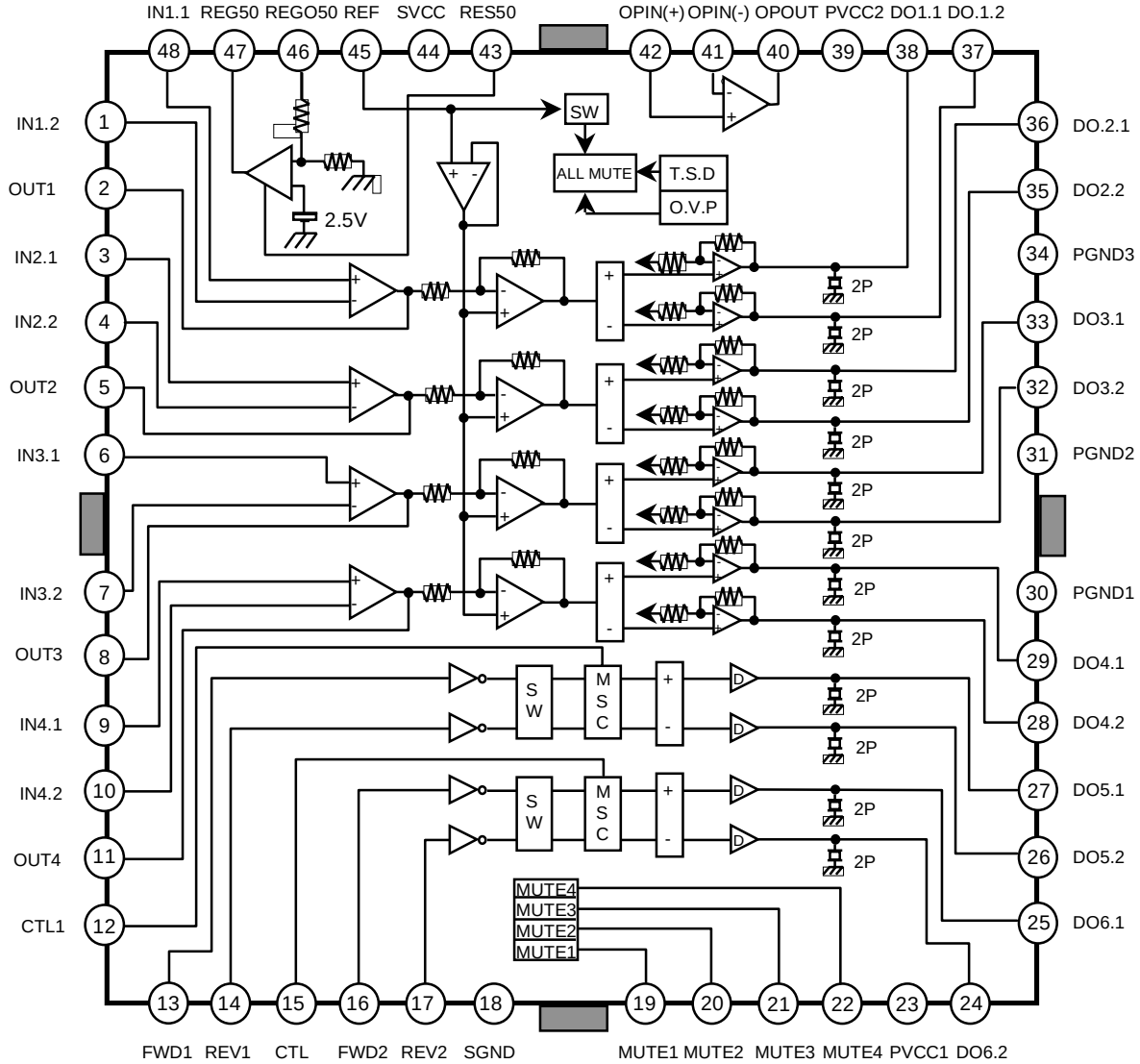
ORDERING INFORMATION

Device	Package	Operating Temperature
KA3031	48-QFPH-1414	-30°C ~ +85°C

TARGET APPLICATIONS

- CD - Player (Tray, Change)
- VIDEO-CD (Tray, Change)
- CAR CD-Player (Tray, Change)

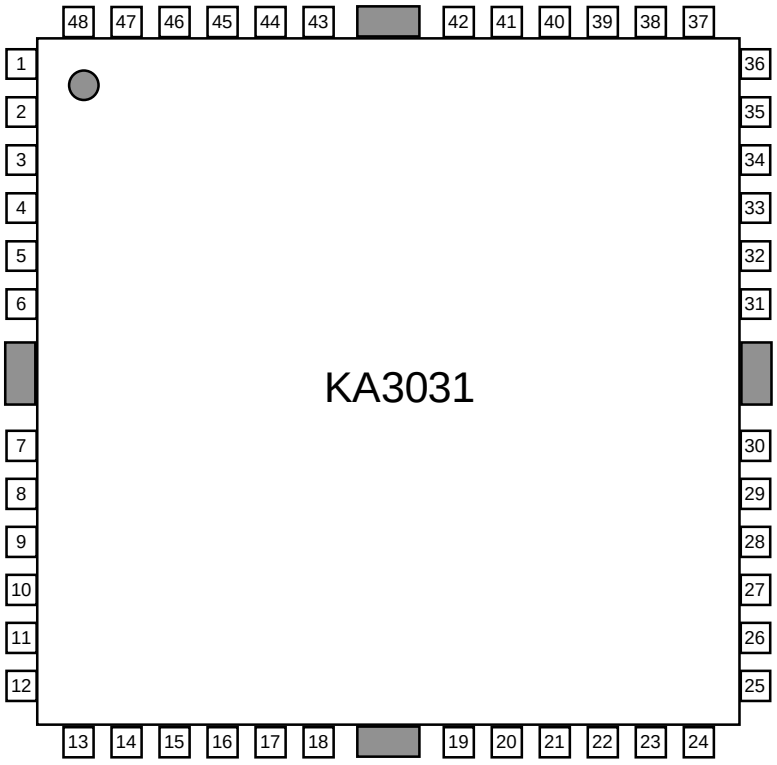
BLOCK DIAGRAM



Notes

1. SW = Logic Switch
2. MSC = Motor Speed Control
3. D = Output Driver

PIN CONFIGURATION



PIN DESCRIPTION

NO.	SYMBOL	I/O	DESCRIPTION
1	IN1.2	I	CH1 OP-AMP INPUT (-)
2	OUT1	O	CH1 OP-AMP INPUT
3	IN2.1	I	CH2 OP-AMP INPUT(+)
4	IN2.2	I	CH2 OP-AMP INPUT(-)
5	OUT2	O	CH2 OP-AMP INPUT
6	IN3.1	I	CH3 OP-AMP INPUT(+)
7	IN3.2	I	CH3 OP-AMP INPUT(-)
8	OUT3	O	CH3 OP-AMP INPUT
9	IN4.1	I	CH4 OP-AMP INPUT(+)
10	IN4.2	I	CH4 OP-AMP INPUT(-)
11	OUT4	O	CH4 OP-AMP INPUT
12	CTL1	I	CH5 MOTOR SPEED CONTROL
13	FWD1	I	CH5 FORWARD INPUT
14	REW1	I	CH5 REVERSE INPUT
15	CTL2	I	CH6 MOTOR SPEED CONTROL
16	FWD2	I	CH6 FORWARD INPUT
17	REW2	I	CH6 REVERSE INPUT
18	SGND	-	SIGNAL GROUND
19	MUTE1	I	CH1 MUTE
20	MUTE2	I	CH2 MUTE
21	MUTE3	I	CH3 MUTE
22	MUTE4	I	CH4 MUTE
23	PVCC1	-	POWER SUPPLY VOLTAGE (FOR CH5,CH6)
24	DO6.2	O	CH6 DRIVE OUTPUT

PIN DESCRIPTION (Continued)

NO.	SYMBOL	I/O	DESCRIPTION
25	DO6.1	O	CH6 DRIVE OUTPUT
26	DO5.2	O	CH5 DRIVE OUTPUT
27	DO5.1	O	CH5 DRIVE OUTPUT
28	DO4.2	O	CH4 DRIVE OUTPUT
29	DO4.1	O	CH4 DRIVE OUTPUT
30	PGND	-	POWER GROUND
31	PGND	-	POWER GROUND
32	DO3.2	O	CH3 DRIVE OUTPUT
33	DO3.1	O	CH3 DRIVE OUTPUT
34	PGND	-	POWER GROUND
35	DO2.2	O	CH2 DRIVE OUTPUT
36	DO2.1	O	CH2 DRIVE OUTPUT
37	DO1.2	O	CH1 DRIVE OUTPUT
38	DO1.1	O	CH1 DRIVE OUTPUT
39	PVCC2	-	POWER SUPPLY VOLTAGE (FOR CH1,CH2,CH3,CH4)
40	OPOUT	O	OPAMP OUTPUT
41	OPIN(-)	I	OPAMP INPUT(-)
42	OPIN(+)	I	OPAMP INPUT(+)
43	RES50	I	REGULATOR 5 V RESET
44	SVCC	-	SIGNAL SUPPLY VOLTAGE
45	REF	I	BIAS VOLTAGE INPUT
46	REG050	O	REGULATOR 5V OUTPUT
47	REG50	O	REGULATOR OUTPUT
48	IN1.1	I	CH1 OPAMP INPUT(+)

APPLICATION INFORMATION

1. REFERENCE INPUT & ALL MUTE FUNCTION

Pin 45 (REF) can use the reference Input pin or the All Mute signal input pin.

1.1. Reference Input

In the case of the reference input pin, you must keep the applied voltage range between 2[V] and 6.5[V] at Vcc = 8[V].

1.2 All Mute Input

When using the All MUTE function pin, applied voltage condition is as follows.

All MUTE ON Voltage	below 0.5[V]	Mute function operation
All MUTE OFF Voltage	above 2 [V]	Normal operation

2. SEPARATED CHANNEL MUTE FUNCTION

These pins are used for individual channel mute operation.

1) When the mute pins (pin19, 20, 21 and 22) are High level, the mute circuits are activated so that the output circuit is muted.
2) When the voltage of the mute pins (pin19, 20, 21 and 22) are Low level, the mute circuit is stopped and output circuits operate normally.
3) If the chip temperature rises above 175°C, then the thermal shutdown (TSD) circuit is activated and the output circuits are muted.

Mute1 (pin 19) - CH1 mute control input pin.
Mute2 (pin 20) - CH2 mute control input pin.
Mute3 (pin 21) - CH3 mute control input pin.
Mute4 (pin 22) - CH4 mute control input pin.

3. PROTECTION FUNCTION

3.1 Thermal Shutdown (TSD)

If the chip temperature rises above 175°C, then the thermal shutdown (TSD) circuit is activated and the output circuit is will be mute. The TSD circuit is temperature hysteresis 25°C.

3.2 Under Voltage Lockout (UVLO) and Over Voltage Protection (OVP)

It is designed to mute-operate the internal bias by the function of UVLO and OVP, when the power supply voltage falls below 3.5[V] or above 20[V].

4. Regulator & Reset Function

The regulator and reset circuits are as illustrated in Fig1. where R1=R2.

1) The external circuit is composed of the transistor, KSB772 and a capacitor,about 33[uF]. The capacitor is used as a ripple eliminator and should have good temperature cahracteristics.
2) The regulator output voltage (pin 46) is decided as follows.

Vout = 2 * 2.5 = 5[V] (where R1=R2)

3) When the voltage of pin 43 (Vreset) is at 5[V], the regulator output voltage (pin 46) becaues 5[V]. If the voltage of pin 43 is 0[V], the output voltage of pin 46 becaues 0[V].

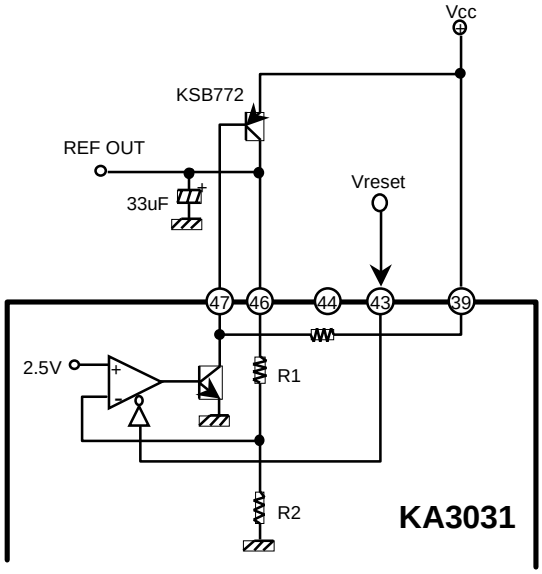
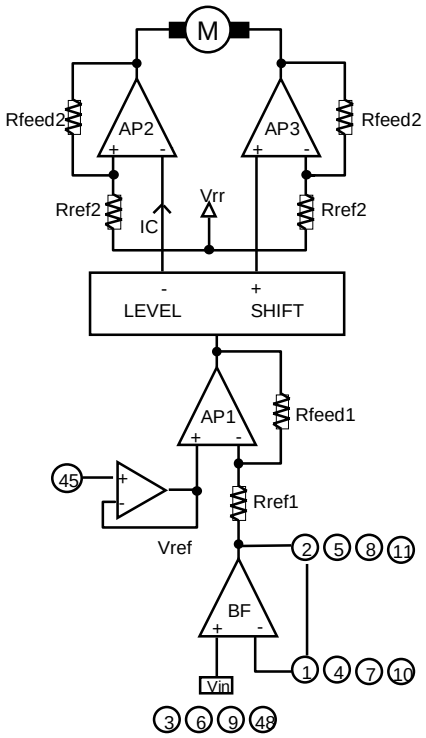


Fig. 1. Regulator Circuit

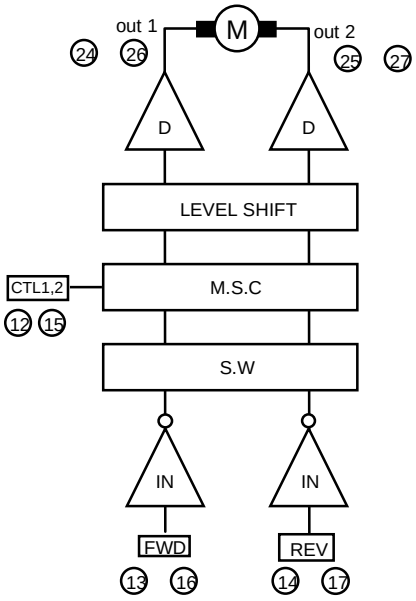
5. FOCUS, TRACKING ACTUATOR, SPINDLE, SLED MOTOR DRIVE PART



1) The voltage,Vref is the reference voltage given by the external bias voltage of the pin 45.
2) The input signal (Vin) through pins 3, 6, 9 and 48 is amplified one times (Rref1=Rfeed1) by the AP1 and then fed to the level shift.
3) The level shift produces the current due to the difference between the input signal and the arbitrary reference signal .
   The current produced as + ΔI and - ΔI are fed into the output amplifier, where output amplifier (AP2, 3) gain is two times (all Rref2=Rfeed2).
4) If you desire to change the gain,the input buffer amplifier (BF) can be used.
5) The Output stage is the balanced transformerless (BTL) driver.
6) The bias voltage Vrr is expressed as below;

$$Vrr = \frac{Vcc - Vbe}{2} \ [V]$$

6. TRAY, CHANGE MOTOR DRIVE PART



6.1 Rotational Direction Control

The forward and reverse rotational direction is controlled by FWD (pin 13, 16) and REV(pin 14, 17) input conditions are as follows.

INPUT		OUTPUT		
FWD	REV	OUT1	OUT2	State
H	H	H	H	Stop
H	L	H	L	Forward
L	H	L	H	Reverse
L	L	L	L	Stop

Out1 pins are pins 24 and 26, and out2 pins are pins 25 and 27.

6.2 Motor Speed Control

1)The almost maximum torque is obtained when it is used with the pins 12 and 15 (CTL1, 2) OPEN.
2) If the torque of the motor is too low, then the applied voltage at pins 12 and 15 (CTL1, 2) are 0[V].
3) When motor speed controlled, the applied voltage of the pins 12 and 15 (CTL1, 2) is between 0 and 4 V.
   Also, if the speed control is constant , the applied voltage of the pins 12 and 15 (CTL1, 2) is between 4 and 5 V.
4) This IC's applied maximum voltage is 6 V when Vcc is 8 V.
5) You must not use the applied CTL1, 2 voltage above 5.8 V when Vcc is 8 V, and 3 V when Vcc is 5 V.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Chacteristics	Symbol	Value	Unit
Maximum Supply Voltage	Vcc	18	V
Power Dissipation	Pd	2.8	W
Operating Temperature	Topr	-30 ~ +85	°C
Storage Temperature	Tstg	-55 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 25°C)

Chacteristics	Symbol	Value			Unit
		MIN	TYP	MAX	
Operating Supply Voltage	Vcc	4.5	-	16	V

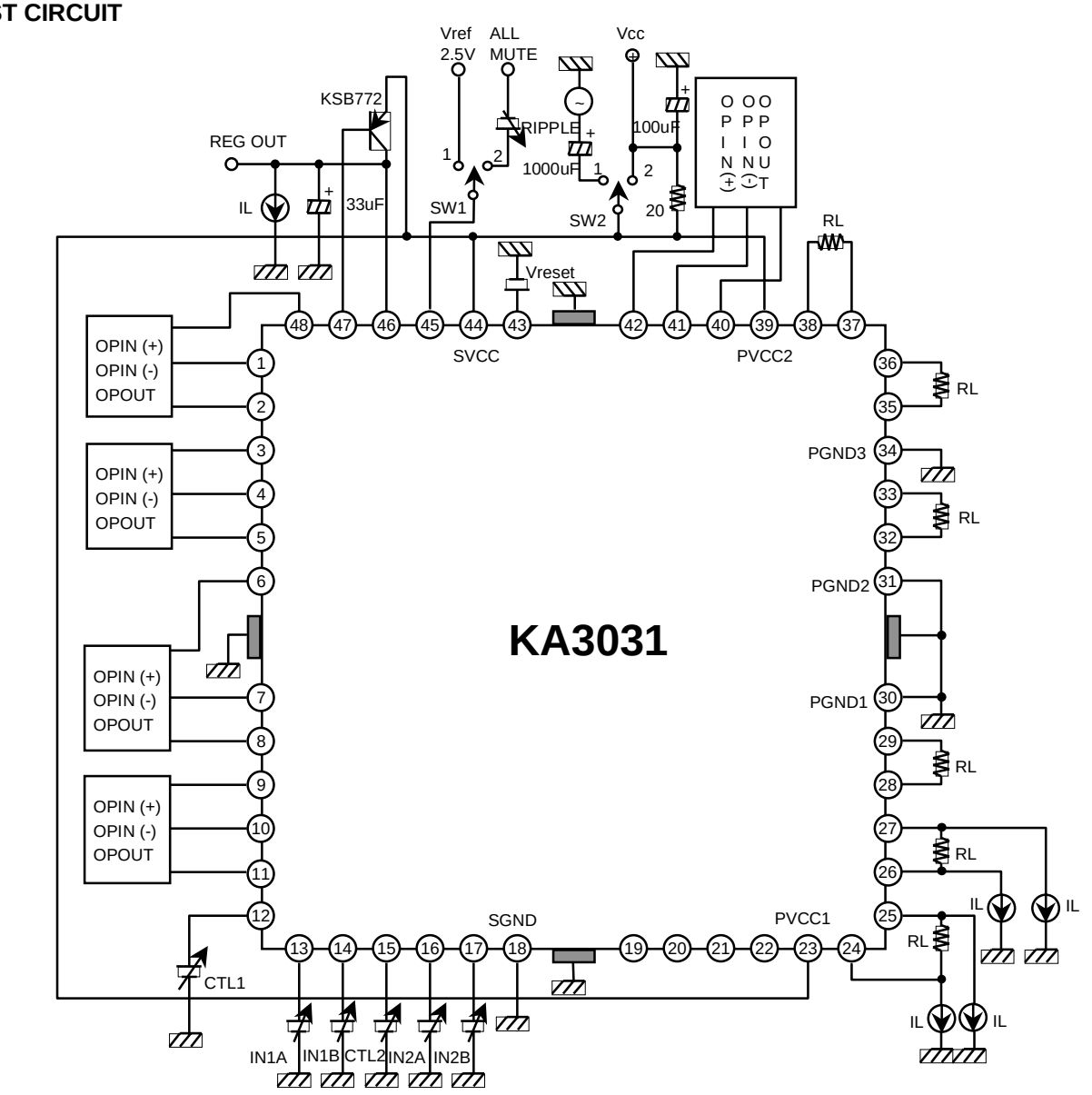
ELECTRICAL CHARATERISTICS
(Svcc= PVcc1= PVcc2=8 V, Ta=25°C, unless otherwise specified)

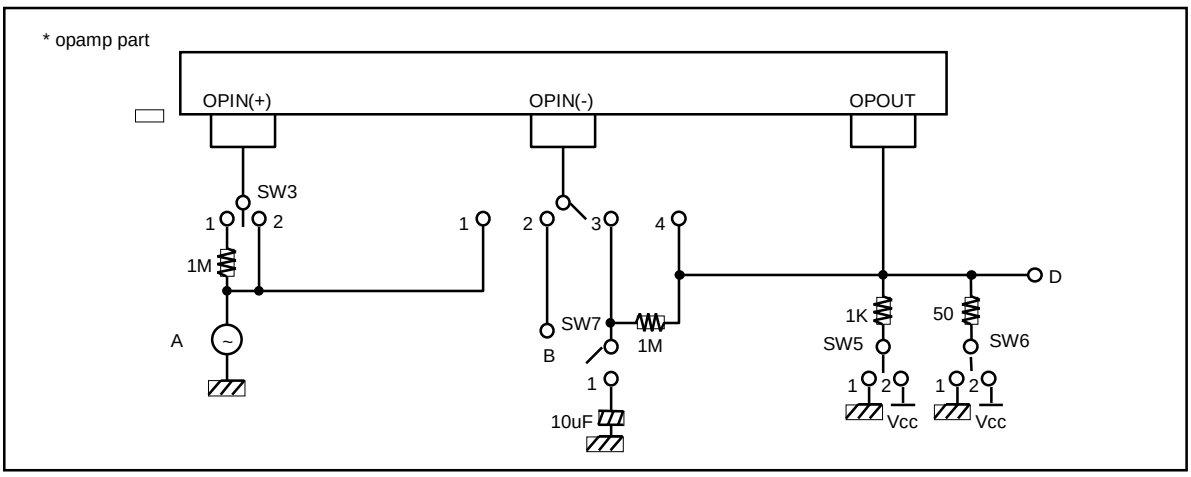
Characteristics	Symbol	MIN	TYP	MAX	Test Conditions	Unit
Quiescent Circuit Current	Icc	9	12	16	under no-load	mA
MUTE ON Current	Imute	-	6	10	pin45=GND	mA
MUTE ON Voltage	Vmon	-	-	0.5		V
MUTE OFF Voltage	Vmoff	2	-	-		V
* DRIVER PART(RL=8ohm)						
Input Offset Voltage	Vio	-20	-	+20		mV
Output Offset Voltage	Voo	-50	-	+50	Vin=2.5 V	mV
Maximum Output Voltage 1	Vom1	4	5.5	-	Vcc=8V, RL=8ohm	V
Maximum Output Voltage 2	Vom2	7	9	-	Vcc=13 V, RL=24 ohm	V
Closed-loop Voltage Gain	Avf	9	10.5	12	Vin=0.1 Vrms	dB
Ripple Rejection Ratio	RR	-	50	-	Vin=0.1 Vrms, f=120 kHz	dB
Slew Rate	SR	-	0.8	-	Square, Vout=2Vp-p, f=120 kHz	V/us
* NORMAL OPAMP PART						
Input Offset Voltage	Vof1	-10	-	+10		mV
Input bias Current	Ib1	-	-	300		nA
High Level Output Voltage	Voh1	6	6.8	-		V
Low Level Output Voltage	Vol1	-	1.0	1.8		V
Output Sink Current	Isink1	10	40	-	RL=50 ohm	mA
Output Soure Current	Isou1	10	40	-	RL=50 ohm	mA
Open loop Voltage Gain	GVo1	-	75	-	Vin=-75 dB, f=1 kHz	dB
Ripple Rejection Ratio	RR1	-	65	-	Vin=-20 dB, f=120 kHz	dB
Slew Rate	SR1	-	1	-	Square, Vout=2Vp-p, f=120 kHz	V/us
Common Mode Rejection Ratio	CMRR1	-	80	-	Vin=-20 dB, f=1 kHz	dB

ELECTRICAL CHARATERISTICS (Svcc= PVcc1= PVcc2=8 V, Ta=25°C)

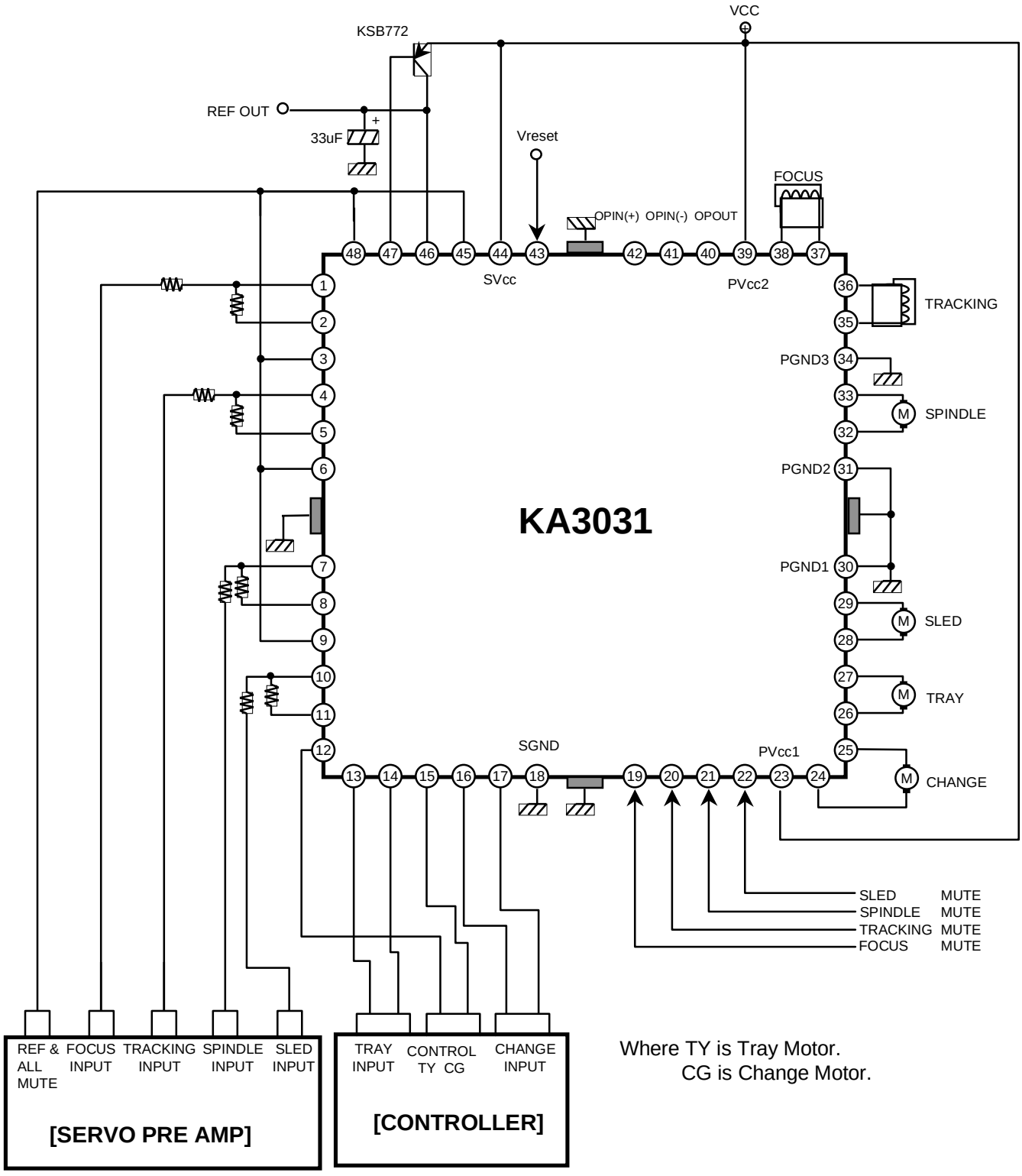
Charateristics	Symbol	MIN	Typ	MAX	Test Conditions	Unit
* INPUT OPAMP PART						
Input Offset Voltage	Vof2	-10	-	+10		mV
Input Bias Current	Ib2	-	-	300		nA
High Level Output Voltage	Voh2	7	7.7	-		V
Low Level Output Voltage	Voh2	-	0.2	0.5		V
Output Sink Current	Isink2	500	800	-		uA
Output Source Current	Isou2	500	800	-		uA
Open loop Voltage Gain	GVo2	-	80	-	Vin=-75 dB, f=1 kHz	dB
Slew Rate	SR2	-	1	-	Square, Vout=2Vp-p, f=120 kHz	V/us
Common Mode Rejection Ration	CMRR2	-	80	-	Vin=-20 dB, f=1 kHz	dB
* 5V REGULATOR PART						
Regulator Output Voltage	Vreg	4.75	5	5.25	IL=100 mA	V
Load Regulation	Δ Vr l	-40	0	+10	IL=0 → 200 mA	mV
Line Regulation	Δ Vcc	-20	0	+30	IL=200 mA, Vcc=6 V → 9 V	mV
Reset ON Volatge	Reson	-	-	0.5		V
Reset OFF Voltage	Resoff	2	-	-		V
* TRAY, CHANGER DRIVE PART (RL=45ohm)						
Input High Level Voltage	Vih	2	-	-		V
Input Low Level Voltage	Vih	-	-	0.5		V
Output Voltage 1	Vo1	5.2	6.0	6.8	Vcc=8 V, Vct l=3.5 V	V
Output Voltage 2	Vo2	7.5	8.5	9.5	Vcc=13 V, Vct l=4.5 V	V
Output Load Regulation	Δ Vr l	-	300	700		mV
Output Offset Voltage 1	Voo1	-10	-	+10	Vin=5 V, 5 V	mV
Output Offset Voltage 2	Voo2	-10	-	+10	Vin=0 V, 0 V	mV

TEST CIRCUIT





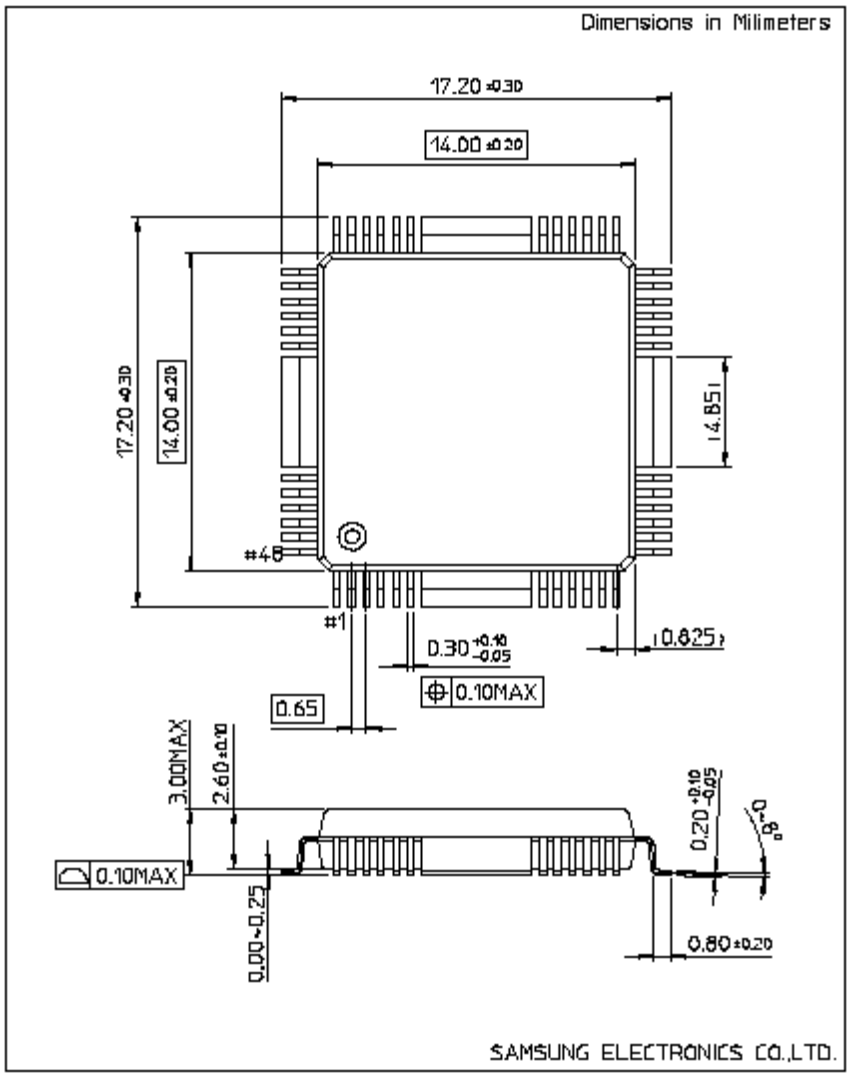
APPLICATION CIRCUIT

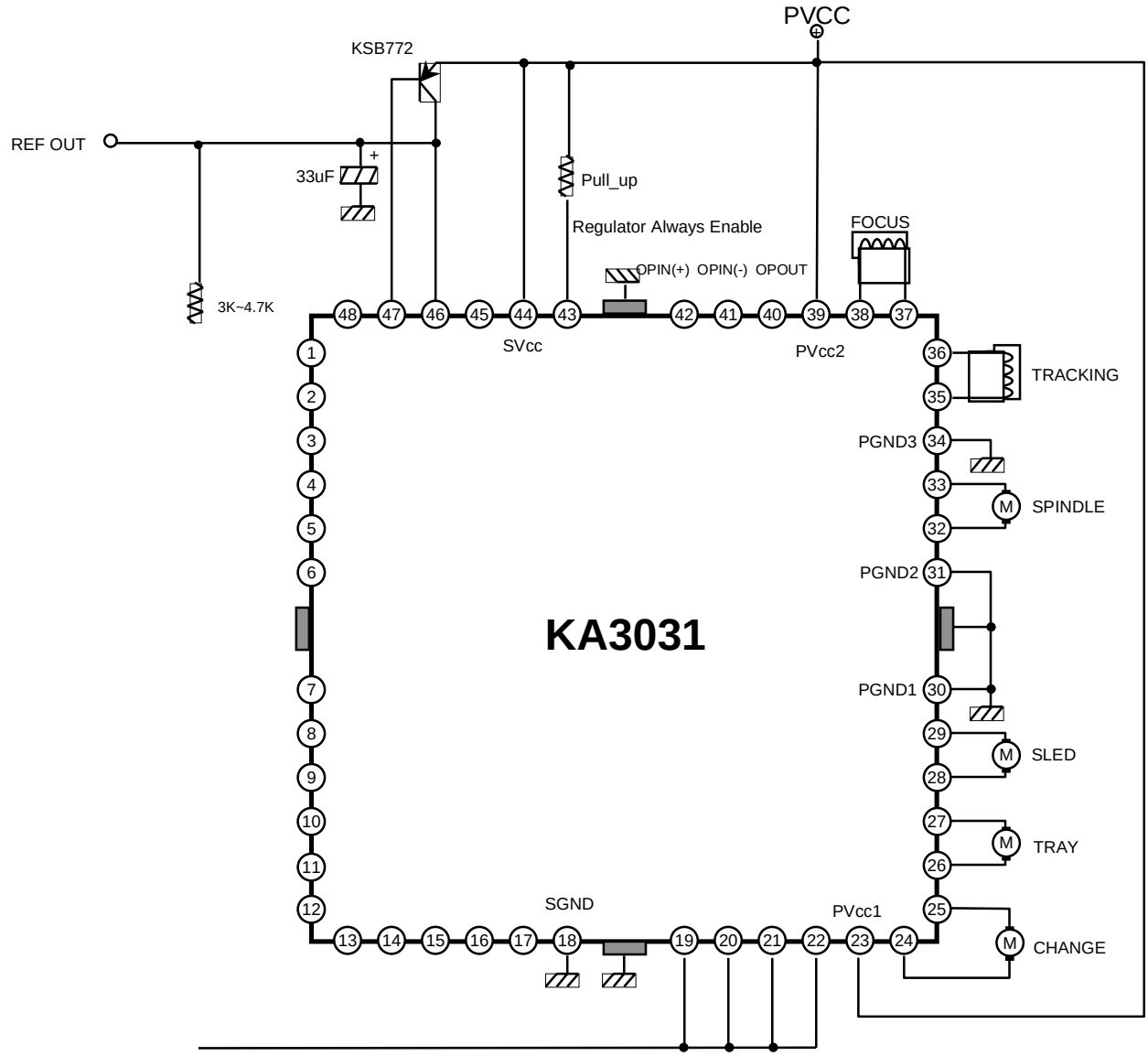


Note 1. Radiation pin is connected to the internal GND of the package.
Connect the pin to the external GND.

PACKAGE DIMENSIONS

48-QFPH-1414




PVCC
KSB772
REF OUT
33uF
Pull_up
Regulator Always Enable
FOCUS
OPIN(+) OPIN(-) OPOUT
3K~4.7K
SVcc
PVcc2
TRACKING
PGND3
SPINDLE
PGND2
KA3031
PGND1
SLED
TRAY
SGND
PVcc1
CHANGE