SPM + VCM ONE CHIP DRIVER

The KA3120 is an ASIC combination chip, which was designed for the HDD, includes the following functions: spindle motor drive, voice coil motor drive, retract and power management.

To drive and control the spindle, the digital ASIC provides the appropriate control signals (start up, commutation, speed control) to the KA3120.
The spindle motor condition is monitored by the FG output and the motor speed control is accomplished via the PWMSP input. The ASIC controls the voice coil motor current via PWMH and PWML inputs and the power management circuit always monitors the power supply voltages.

48-QFPH-1414

FEATURES

SPINDLE MOTOR DRIVE PART

- Soft switching
- Spindle brake after retract
- Adjustable brake delay time
- 2.0A max. current power driver
- Low output saturation voltage: 1V typical @1.6A
- PWM decoder & filter for soft switching
- The digital circuit (ASIC) based start-up, commutation and motor speed control
- Intelligent Retract (without bouncing)

VOICE COIL MOTOR DRIVE PART

- Trimmed low offset current
- 1.2A max. current power driver
- Gain selection and adjustable gain
- Automatic power down retract function
- Class AB linear amplifier with no dead zone
- Low output saturation voltage: 0.8V typical @1.0A
- Internal full bridge with Vertical PNP & NPN

APPLICATION

- Hard disk drive (HDD) products

ORDERING INFORMATION

Device	Package	Operating Temperature
KA3120	48–QFPH–1414	0 to 70°C

POWER RETRACT AND MANAGEMENT

- Power on reset with delay
- Hysteresis on both power comparators
- Over temperature & over current shut down
- 5V and 12V power monitor threshold accuracy ±2%
- Buffered reference voltage output pin accuracy 3.3V±2%

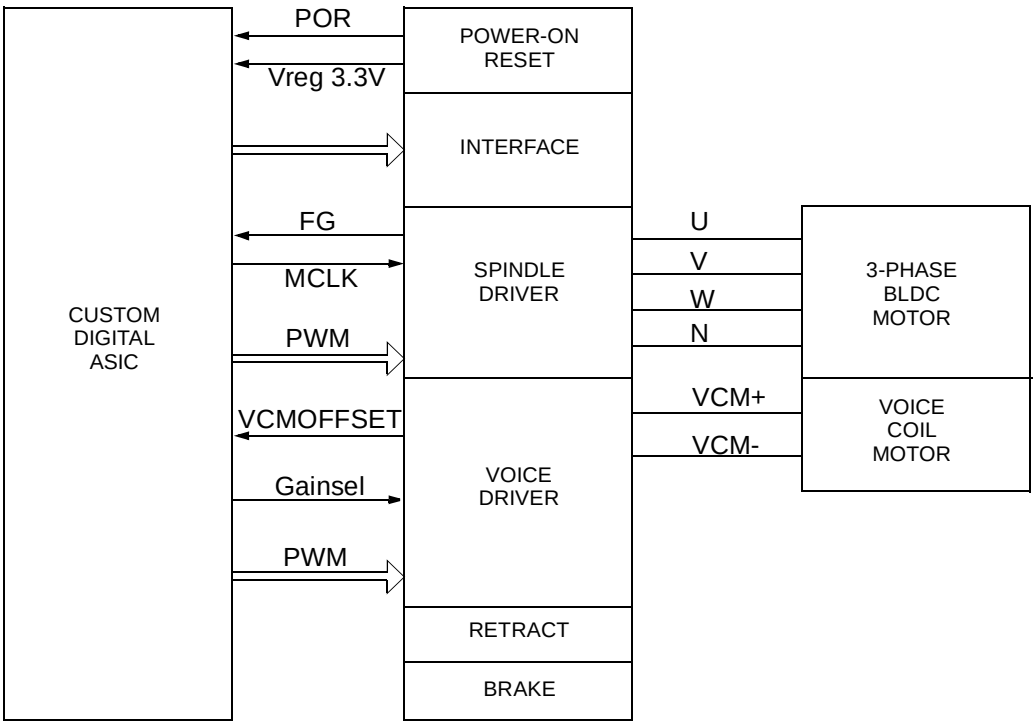
PACKAGE

- 48QFPH (48 pin Quad Flat Package Heat-sink)

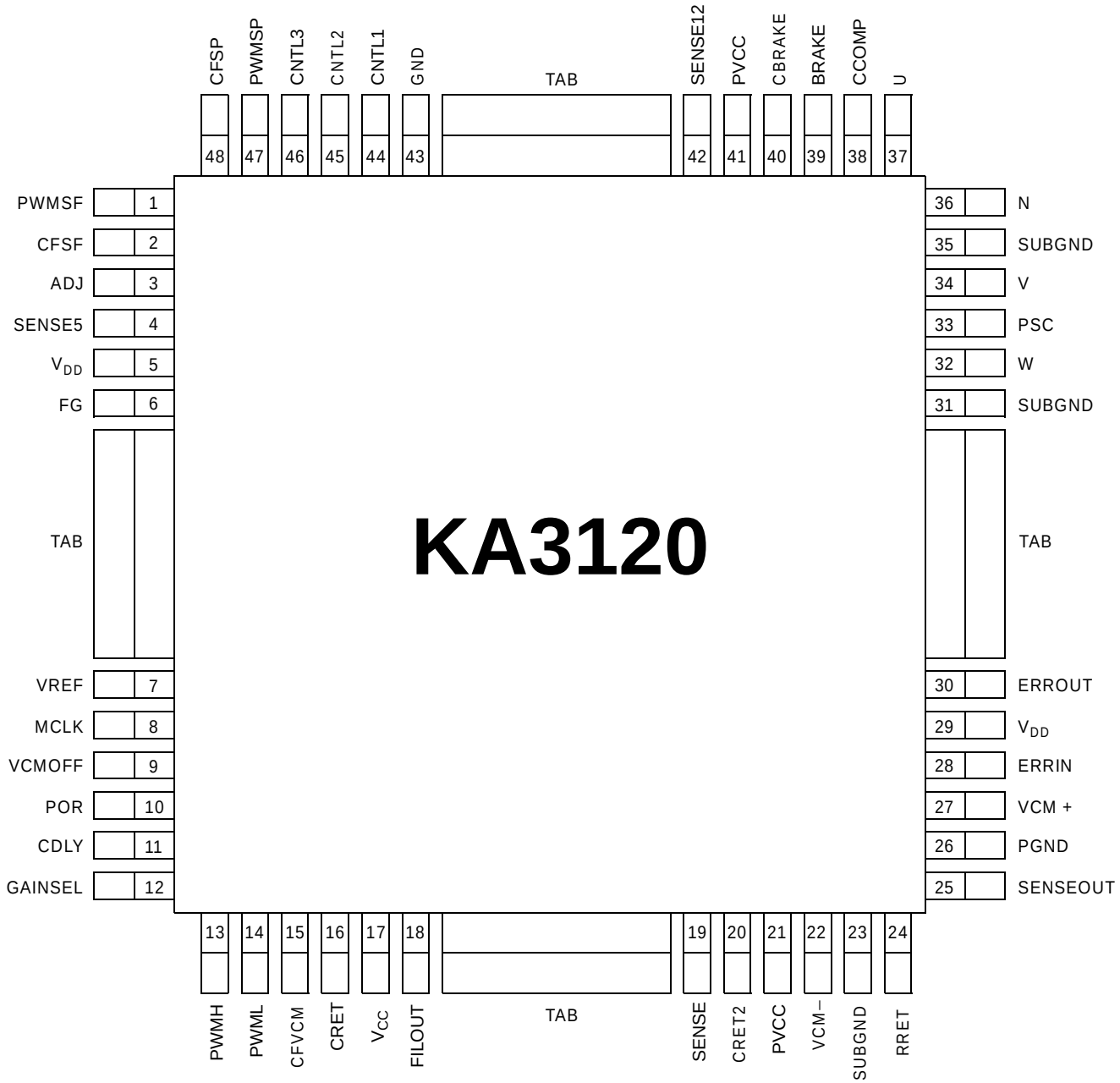
QUICK REFERENCE DATA (Ta = 25°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE					
Analog Supply Voltage	PVCC	10.8	12	13.2	V
Analog Supply Voltage	VDD	4.5	5	5.5	V
DRIVERS					
Maximum Spindle Current	$I_{SPINmax}$	–	–	2.0	A
Maximum VCM Current	I_{VCMmax}	–	–	1	A
Maximum Retract Current	$I_{RETRACTmax}$	–	–	190	mA

BLOCK DIAGRAM



PIN CONFIGURATION



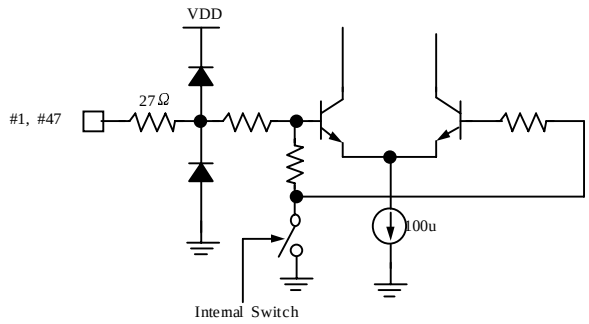
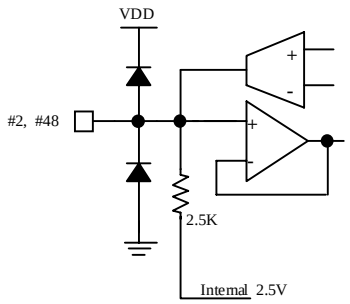
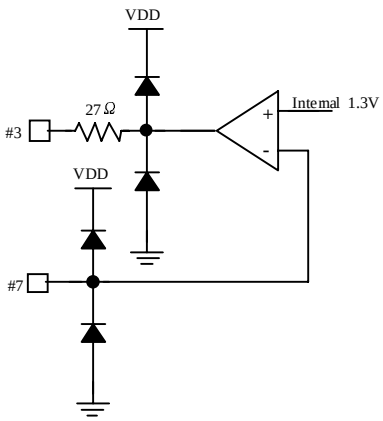
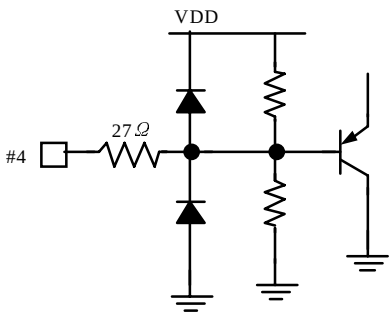
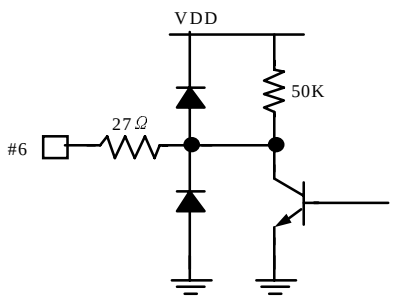
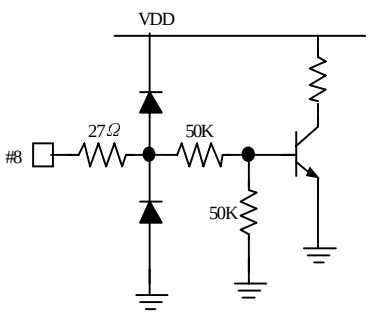
PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	PWMSF	I	PWM input for spindle soft switching
2	CFSF	–	Capacitor for spindle PWM soft switching filter
3	ADJ	–	Reference voltage adjustable
4	SENSE5	I	Adjustable for threshold voltage to 5V
5	V_{DD}	–	5V power supply
6	FG	O	Frequency generation to spindle speed
7	VREF	O	Output to regulate 3.3V ASIC power
8	MCLK	I	Clock from ASIC for switching
9	VCMOFF	O	VCM output offset monitoring pin
10	POR	O	Power on reset
11	CDLY	–	Power on reset delay
12	GAINSEL	I	VCM AMPLIFIER gain selection
13	PWMH	I	PWM signal input (MSB)
14	PWML	I	PWM signal input (LSB)
15	CFVCM	–	Filter capacitor for VCM PWM control
16	CRET	–	Current delay capacitor for retract
17	V_{CC}	–	12V power line
18	FILOUT	O	VCM PWM output
19	SENSE	I	VCM current sensing
20	CRET2	–	Power for retract
21	PVCC	–	12V power line for VCM output
22	VCM (–)	–	VCM output
23	SUBGND	–	Ground
24	RRET	I	Adjustable max. retract current
25	SENSEOUT	O	VCM sense AMPLIFIER output
26	PGND	–	Ground
27	VCM (+)	–	VCM output
28	ERRIN	I	VCM error AMPLIFIER input
29	V_{DD}	–	5V power supply
30	ERROUT	O	VCM error AMPLIFIER output
31	SUBGND	–	Ground
32	W	O	W phase output

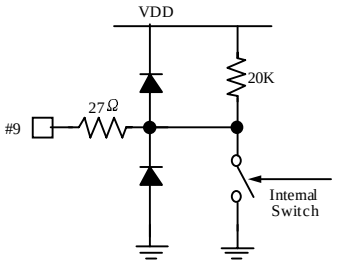
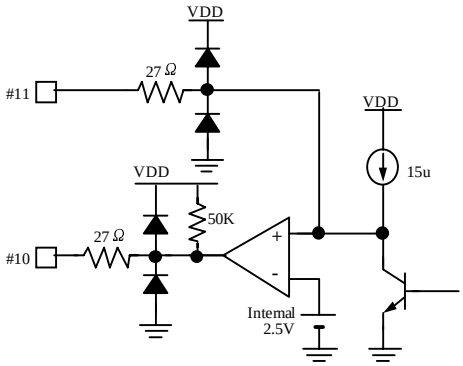
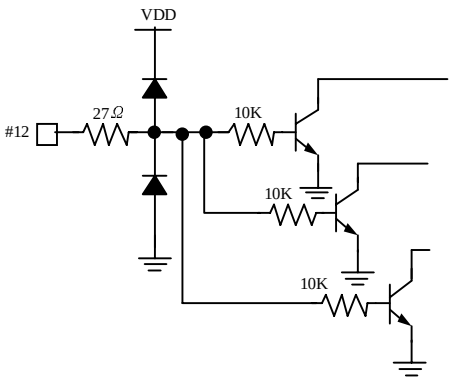
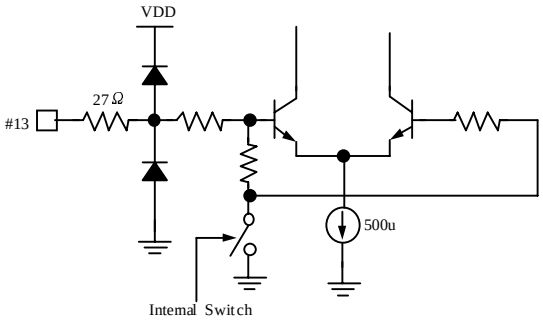
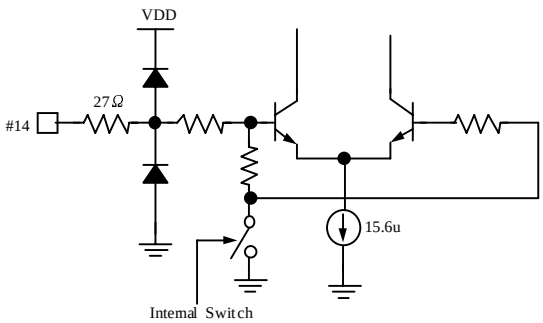
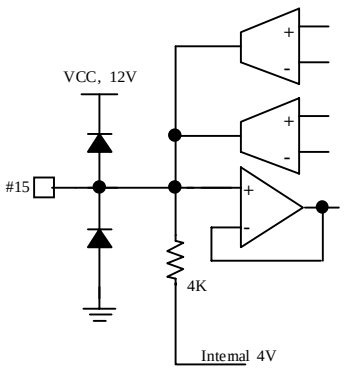
PIN DESCRIPTION (Continued)

Pin No.	Symbol	I/O	Description
33	PCS	O	Spindle output current sensing
34	V	O	V phase output
35	SUBGND	–	Ground
36	N	I	N phase (motor neutral line)
37	U	O	U phase output
38	CCOMP	–	Spindle output control compensation
39	BRAKE	O	Dynamic brake
40	CBRAKE	–	Back-EMF charging capacitor for brake power
41	PVCC	–	12V power line for spindle
42	SENSE12	I	Adjustable for threshold voltage to 12V
43	GND	–	Ground
44	CNTL1	I	Control input for spindle and brake
45	CNTL2	I	Control input for start-up clock and soft switching
46	CNTL3	I	Control input for VCM AMPLIFIER & retract
47	PWMSP	I	PWM input for spindle speed control
48	CFSP	–	Filter capacitor for spindle PWM control

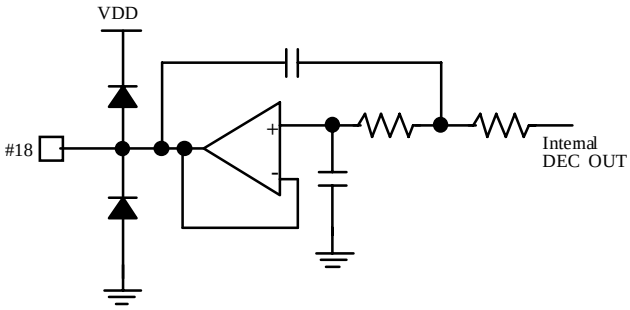
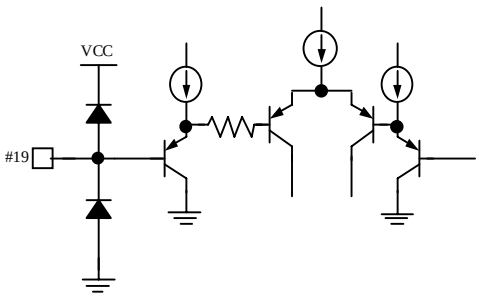
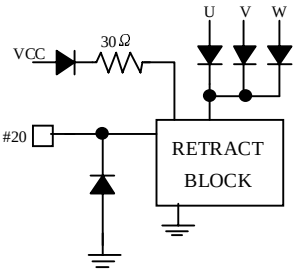
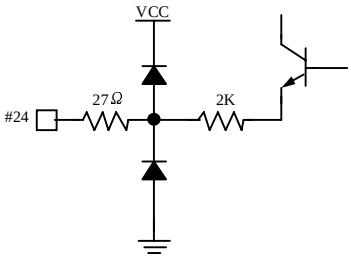
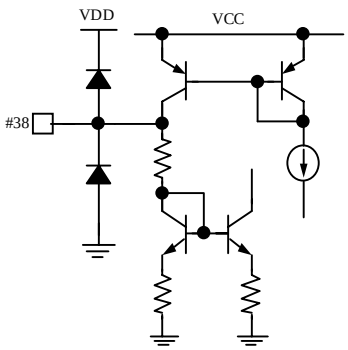
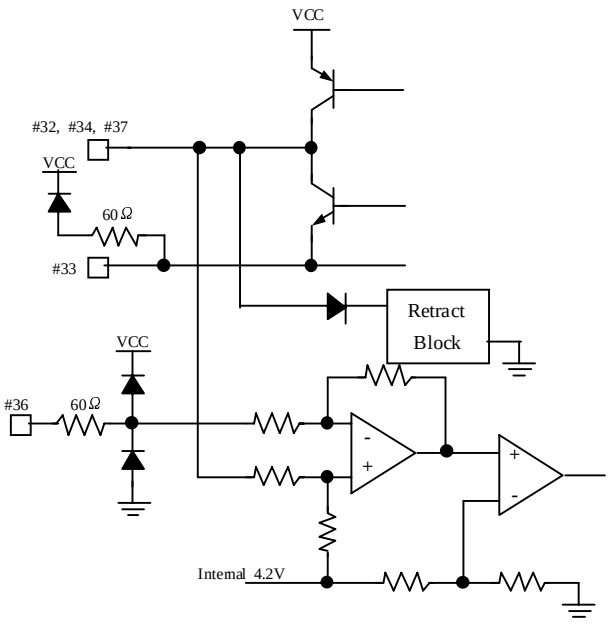
EQUIVALENT CIRCUITS

PWM decoder filter input	PWM decoder filter Cap.
	
Regulator part	**SENSE5 input**
	
FG output	**MCLK input**
	

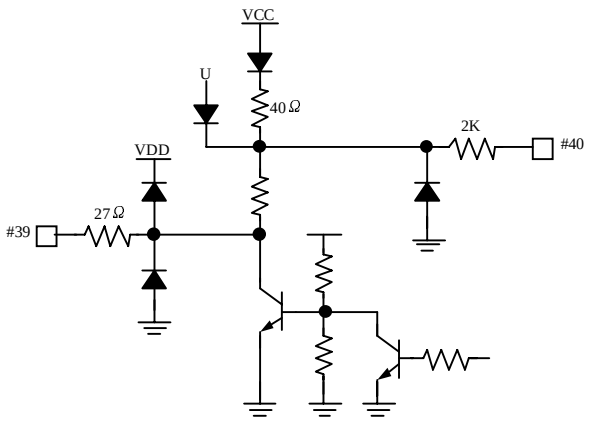
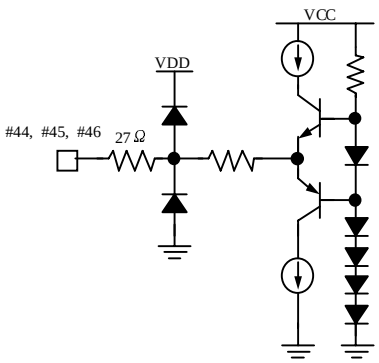
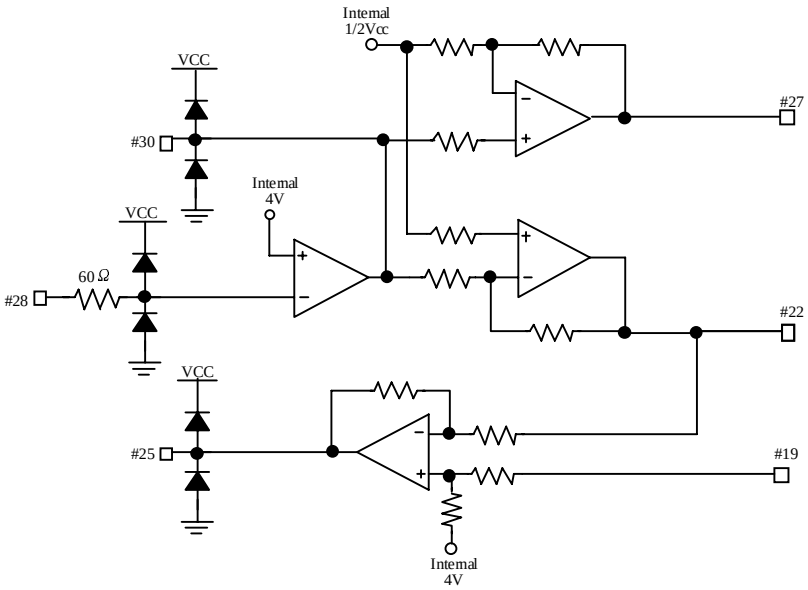
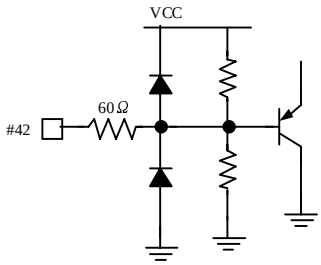
EQUIVALENT CIRCUITS (Continued)

VCM offset compensation output	Power On Reset part
	
VCM gain selection input	**VCM PWM high input**
	
VCM PWM low input	**VCM PWM filter Cap.**
	

EQUIVALENT CIRCUITS (Continued)

Filtered VCM PWM command output	Max. retract current set input
	
Cap. for retract power	**VCM current sense input**
	
SPM output compensation Cap.	**SPM output and BEMF sensing part**
	

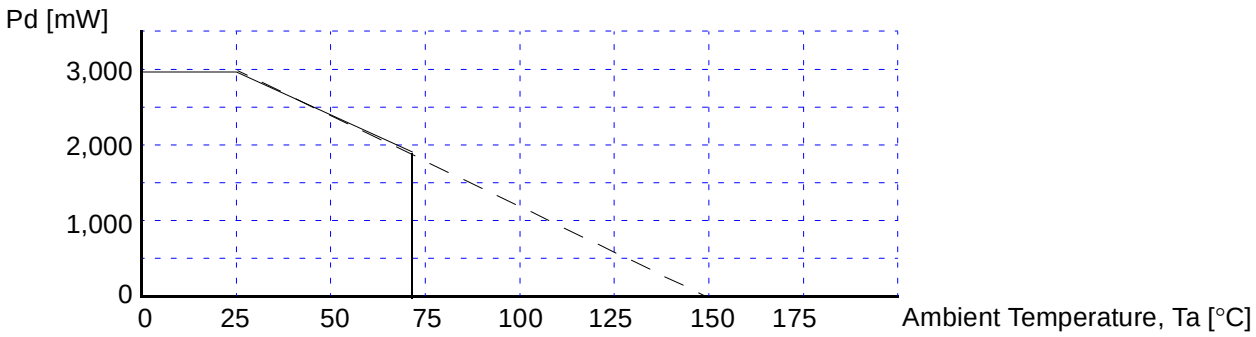
EQUIVALENT CIRCUITS (Continued)

Dynamic brake part	CNTL1,2,3 input
	
VCM output and control part	**SENSE12 input**
	

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Characteristic	Symbol	Value	Unit
Maximum signal block supply voltage for 5V line	V_{DDmax}	6	V
Maximum signal block supply voltage for 12V line	V_{CCmax}	15	V
Maximum power block supply voltage for 12V line	PV_{CCmax}	15	V
Maximum output current	I_{Omax}	2	A
Power dissipation	P_D	@3.0	W
Storage temperature	T_{STG}	–55 to 125	°C
Maximum junction temperature	T_{Jmax}	150	°C
Operating ambient temperature	T_A	0 to 70	°C

@: 1. When mounted on 50mm × 50 mm × 1mm PCB (Phenolic resin material)
2. Power dissipation is reduced 16 mV/°C for using above Ta=25°C
3. Do not exceed Pd and SOA.



RECOMMANDED OPERATING CONDITION

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}, PV_{CC}	10.8	12.0	13.2	V
Supply voltage in logic part	V_{DD}	4.5	5.0	5.5	V

ELECTRICAL CHARACTERISTICS

(TA=25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Spec			Unit
			Min.	Typ	Max.	
SUPPLY CURRENT						
5V Line Supply Current 1	I_{DD1}	CNTL1=0V, CNTL2=2.5V, CNTL3=0V	30	40	50	mA
5V Line Supply Current 2	I_{DD2}	CNTL1=CNTL2=CNTL3 =2.5V	15	18	20	mA
5V Line Supply Current 3	I_{DD3}	CNTL1=5V, CNTL2=2.5V, CNTL3=5V	15	18	20	mA
12V Line Supply Current 1	I_{CC1}	CNTL1=0V, CNTL2=2.5V, CNTL3=0V	7	9	12	mA
12V Line Supply Current 2	I_{CC2}	CNTL1=CNTL2=CNTL3 =2.5V	8	11	15	mA
12V Line Supply Current 3	I_{CC3}	CNTL1=5V, CNTL2=2.5V, CNTL3=5V	28	35	43	mA
POWER MONITOR						
Threshold Voltage level for 12V	V_{TH12}	V_{CC}=sweep, V_{DD}=5V	9.1	9.5	9.9	V
Hysteresis on 12V Comparator	V_{HYS12}	–	120	240	360	mV
Adjustable Pin Voltage for 12V	V12	–	3.1	3.3	3.5	V
Threshold Voltage level for 5V	V_{TH5}	V_{CC}=12V, V_{DD}=sweep	4.1	4.3	4.5	V
Hysteresis on 5V Comparator	V_{HYS5}	–	50	100	150	mV
Adjustable Pin Voltage for 5V	V5	–	2.75	2.9	3.05	V
POWER ON RESET GENERATOR						
Charging Current for POR Cap.	I_{CPOR}	V_{CC}=12V, V_{DD}=5V	8.5	12.5	17.0	µA
POR Threshold Voltage	V_{THPOR}	CDLY=sweep	2.3	2.5	2.7	V
Output High Voltage	V_{POH}	V_{CC}=12V, V_{DD}=5V	4.0	–	–	V
Output Low Voltage	V_{POL}	V_{CC}=12V, V_{DD}=5V	–	–	0.5	V
CONTROL INPUT						
Logic Control Input 1 MED Voltage	V_{CTL1O}	V_{CC}=12V, V_{DD}=5V	2.3	2.5	2.7	V
Logic Control Input 1 MED Current	I_{CTL1O}	CNTL1=2.5V	–5	0	5	µA
Logic Control Input 1 HIGH Voltage	V_{CTL1H}	CNTL1=sweep	4.0	–	V_{DD}	V
Logic Control Input 1 HIGH Current	I_{CTL1H}	CNTL1=5V	20	140	200	µA
Logic Control Input 1 LOW Voltage	V_{CTL1L}	CNTL1=sweep	–	–	1.0	V
Logic Control Input 1 LOW Current	I_{CTL1L}	CNTL1=0V	–200	–140	–20	µA
LOGIC CONTROL INPUT 2 & 3 SPEC's are EQUAL to LOGIC CONTROL INPUT 1						

ELECTRICAL CHARACTERISTICS (Continued)

(TA=25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Spec			Unit
			Min.	Typ	Max.	
SPINDLE FG GENERATION						
FG Output High Voltage	V_{FGOH}	–	4.5	–	–	V
FG Output Low Voltage	V_{FGOL}	–	–	–	0.5	V
FG Frequency	FG	–	2.9	3	3.1	kHz
SPINDLE PWM CONTROL						
High Input Current at PWMSP	I_{PWMSP1}	PWMSP=5V	100	113	130	µA
Low Input Current at PWMSP	I_{PWMSP2}	PWMSP=0V	–130	–113	–100	µA
CFSP Charging Current	I_{SPCH}	PWMSP=0V, CFSP=2.5V	80	100	120	µA
CFSP Voltage1 (0% Duty of PWMSP)	V_{SP0}	PWMSP=0V	2.2	2.25	2.3	V
CFSP Discharge Current	I_{SPDCH}	PWMSP=0V, CFSP=2.5V	80	100	120	µA
CFSP Voltage2 (100% Duty of PWMSP)	V_{SP100}	PWMSP=5V	2.7	2.75	2.8	V
CFSP Voltage3 (Open of PWMSP)	V_{SP50}	PWMSP=5V	2.7	2.75	2.8	V
SPINDLE PWM SOFT SWITCHING						
High Input Current at PWMSF	I_{PWMSF1}	PWMSP=5V	100	113	130	µA
Low Input Current at PWMSP	I_{PWMSF2}	PWMSP=5V	–130	–113	–100	µA
CFSP Charging Current	I_{SFCH}	PWMSP=0V, CFSP=2.5V	80	100	120	µA
CFSP Voltage1 (0% Duty of PWMSP)	V_{SF0}	PWMSP=0V	2.2	2.25	2.3	V
CFSP Discharge Current	I_{SFDCH}	PWMSP=0V, CFSP=2.5V	80	100	120	µA
CFSP Voltage2 (100% Duty of PWMSP)	V_{SF100}	PWMSP=5V	2.7	2.75	2.8	V
CFSP Voltage3 (Open of PWMSP)	V_{SF50}	PWMSP=5V	2.7	2.75	2.8	V
BRAKE						
CBrake Output Voltage	V_{BC}	–	–	–	V_{CC}-0.7	V
Brake Output HIGH Voltage	V_{BH}	–	–	–	V_{CC}-0.9	V
Brake Output LOW Voltage	V_{BL}	–	–	–	0.5	V
SPINDLE OUTPUT						
U Saturation Voltage	V_{SATU}	–	–	–	0.5	V
V Saturation Voltage	V_{SATV}	–	–	–	0.5	V
W Saturation Voltage	V_{SATW}	–	–	–	0.5	V

ELECTRICAL CHARACTERISTICS (Continued)

(TA=25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Spec			Unit
			Min.	Typ	Max.	
Leakage Current	I_{LQ}	V_{CC}=15V, U=0V	–	–	10	µA
Spindle Transconductance Gain	GM_S	–	0.7	0.8	0.9	A/V
REGULATOR						
Adjustable PIN Voltage	V_{ADJ}	V_{DD}=sweep	1.2	1.3	1.4	V
SPINDLE MCLOCK						
HIGH Threshold Voltage	V_{MH}	–	2.0	1.4	–	V
LOW Threshold Voltage	V_{ML}	–	–	1.4	0.8	V
HIGH Input Current	I_{MH}	–	15	25	35	µA
LOW Input Current	I_{ML}	–	–10	0	10	µA
VCM PWM CONTROL						
High PWMH Input Current	I_{PWMH1}	PWMH=5V	–	113	130	µA
Low PWMH Input Current	I_{PWMH2}	PWMH=0V	–130	–113	–	µA
High PWML Input Current	I_{PWML1}	PWML=5V	–	113	130	µA
Low PWML Input Current	I_{PWML2}	PWML=0V	–130	–113	–	µA
CFVCM Charge/Discharge Current1	I_{CFVCM1}	PWMH=5V, PWML=5V	–	516	530	µA
CFVCM Charge/Discharge Current2	I_{CFVCM5}	PWMH=Open, PWML=Open	–10	0	10	µA
CFVCM Charge/Discharge Current3	I_{CFVCM9}	PWMH=0V, PWML=0V	–530	–516	–	µA
VCM ERROR AMPLIFIER.						
Input Bias Current	I_{BIAS1}	–	–	5	10	µA
Input Offset Voltage	V_{OS1}	–	–	5	10	mV
Open Loop Voltage Gain	GV1	–	60	80	–	dB
Gain Bandwidth	GBW1	–	1	1.5	–	MHz
AMP Output Voltage Swing	V_{O1}		1.0	–	11.0	V
VCM SENSE AMPLIFIER						
Input Bias Current	I_{BIAS1}	–	–	5	10	µA
Input Offset Voltage	V_{OS1}	–	–	5	10	mV
Open Loop Voltage Gain	GV1	–	60	80	–	dB
Gain Bandwidth	GBW1	–	1	1.5	–	MHz
AMP Output Voltage Swing	V_{O1}	–	1.0	–	11.0	V

ELECTRICAL CHARACTERISTICS (Continued)

(TA=25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Spec			Unit
			Min.	Typ	Max.	
VCM POWER AMPLIFIER						
Input Bias Current	I_{BIAS1}	–	–	5	10	µA
Input Offset Voltage	V_{OL1}	–	–	5	10	mV
Open Loop Voltage Gain	GV1	–	60	80	–	dB
Gain Bandwidth	GBW1	–	1	1.5	–	MHz
Amp Output Voltage Swing	V_{O1}	Rload=100Ω	0.5	–	11.5	V
Output Saturation Voltage	V_{CMSAT}	I_O=1A	–	–	1	V
VCM AMPLIFIER TOTAL						
VCM Transconductance Gain High	GM_{VH}	–	0.40	0.43	0.45	A/V
VCM Transconductance Gain High	GM_{VL}	–	0.09	0.11	0.13	A/V
RETRACT						
Min. Operating Voltage of CRET2	V_{CRET2}	–	3	–	–	V
Source Voltage	V_{SRC}	–	–	1.5	–	V
Sinking Saturation Voltage	V_{RTSAT}	–	–	–	0.4	V
THERMAL SHUT DOWN						
Operating Temperature	T_{SD}	–	–	150	–	°C
Thermal Hysteresis	T_{HYS}	–	–	30	–	°C

APPLICATION INFORMATION

SPINDLE MOTOR DRIVE PART

The KA3120 is a combination chip consisting of Spindle Motor and Voice Coil Motor designed for HDD system. According to the spindle conditions, the digital ASIC circuit provides optimum control signals (start-up, commutation, speed control, and switching mode) to the KA3120.

Detection of the Back-EMF (BEMF) of the spindle motor has to be output to an external digital circuit via FG. The MCLK and PWM signals are used to determine the commutation timing and to control the spindle speed, respectively.

SPINDLE DRIVER

The spindle includes both low and high side drivers (H–bridge) for a three-phase sensorless brushless DC motor. To reduce the saturation voltage, the vertical PNP Tr is used as the high side driver.

FREQUENCY GENERATION (FG)

FG stands for Frequency Generation. It is the out signal toward the digital ASIC.
Representing the current spindle speed frequency, it contains important information about the motor speed and motor spin.
According to the FG frequency, the digital ASIC provides different motor clock signals to the motor drive IC via MCLK and checks the motor speed to send the VCM enable signal via CNTL3.

FG frequency (Hz), motor speed (rpm) and pole number are directly related as shown below in the three phase motor.

FG frequency = motor speed $\times$ pole number $\times$ 3 / 120

In a typical application,

FG frequency = 5400 $\times$ 8 $\times$ 3 / 120 = 1080Hz

FG frequency = Output frequency x 3

MCLK & MASK

The MCLK is a motor clock used as the standard clock signal for the proper commutation timing of the spindle motor. It is supplied by the ASIC.

As shown in table 1, it has different delay times depending on the mode of the spindle speed. Table 1. MCLK & MASK Delay Time to the Spindle Speed.

Table 1. MCLK & MASK Delay Time to the Spindle Speed

	MCLK (Td)	MASK	Switching
Start-up mode	2ms	1ms	Hard Switching
Acceleration mode	FG(n–1)/2	FG(n–1)/4	Hard Switching
Running mode	FG(n–1)/32	344.45us	Soft Switching

After the FG_Edge signal, the MCLK occurs after a half FG_Edge delay time in the acceleration mode and 1/ 32 FG_Edge delay time in the soft switching mode.

MASK

When the coil current is abruptly changed in a short time interval, a spark voltage occurs. This spark voltage mixes with the FG output to give the wrong spindle information to the ASIC. To eliminate the spark voltage from the FG output, the masking block is needed.

$$Vcoil = -L\frac{di}{dt}$$

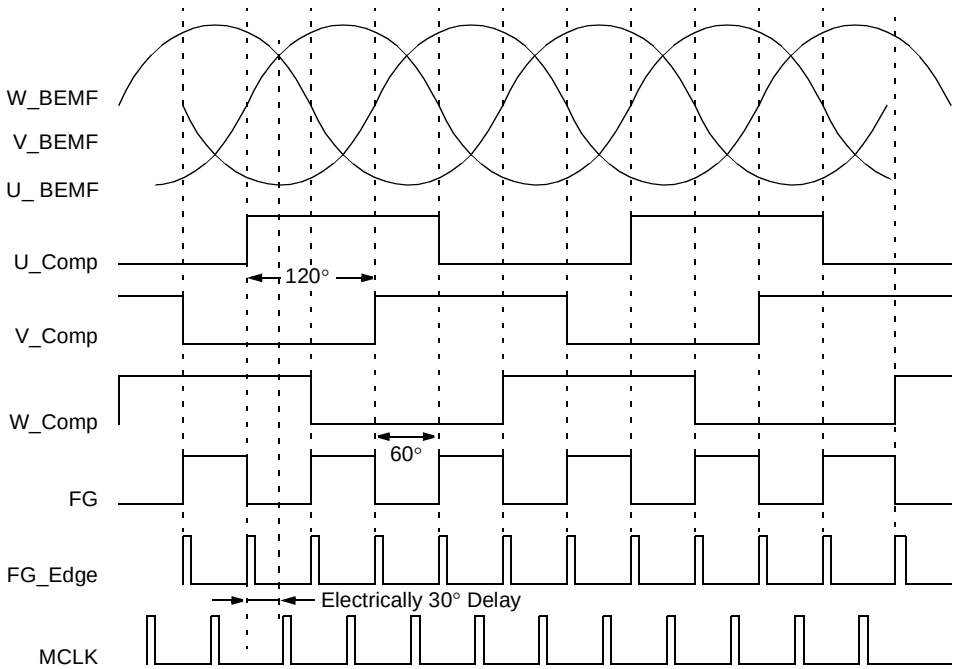


Figure 1. BEM, FG, and MCLK in the Acceleration Mode

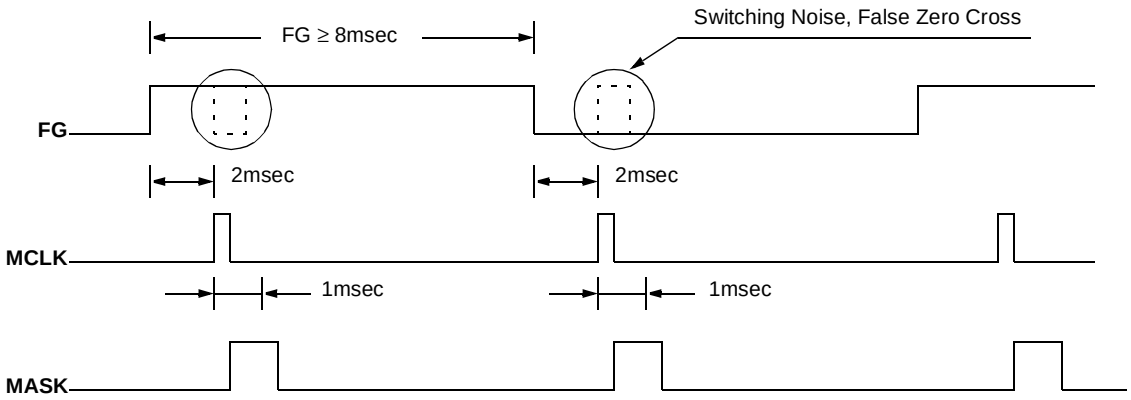


Figure 2. MCLK vs MASK in the Start-up Mode

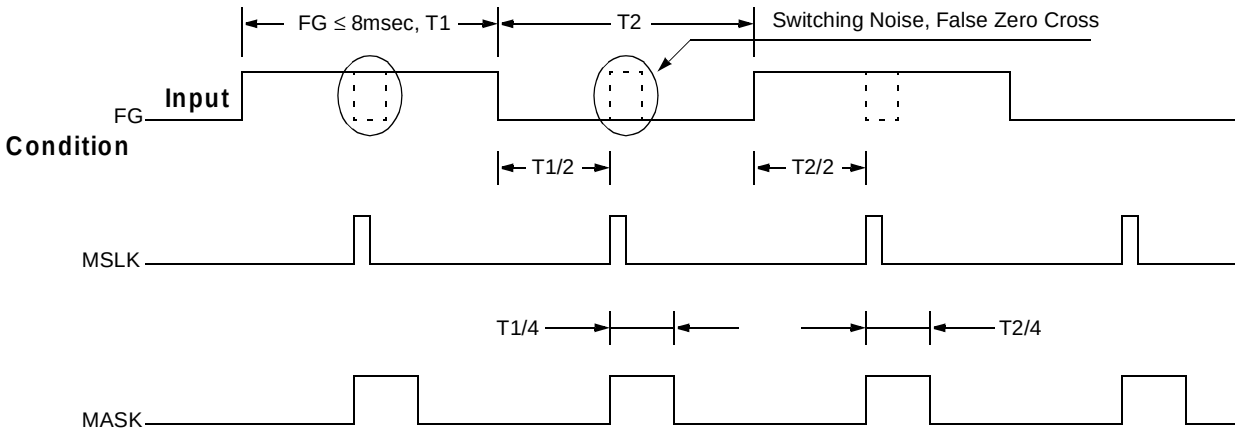


Figure 3. MCLK vs MASK in the Acceleration Mode

PWMDEC AND SPEED CONTROL

Motor speed is measured by the ASIC via the FG output. The digital ASIC compares FG frequency with the target motor speed and sends the speed compensation signal to the PWMSP input of the KA3120. This PWM signal is internally filtered and is converted into DC voltage through the built-in PWM Decoder Filter. The analog output of the filter depends on the duty of the PWM signal. The filter is a one-pole, low-pass filter. The pole location of the filter is determined by the external capacitor connected to pin(48) CFSP.

$$Ispindle = (D - 0.17) \cdot \frac{0.75}{R33(= 0.25)}$$

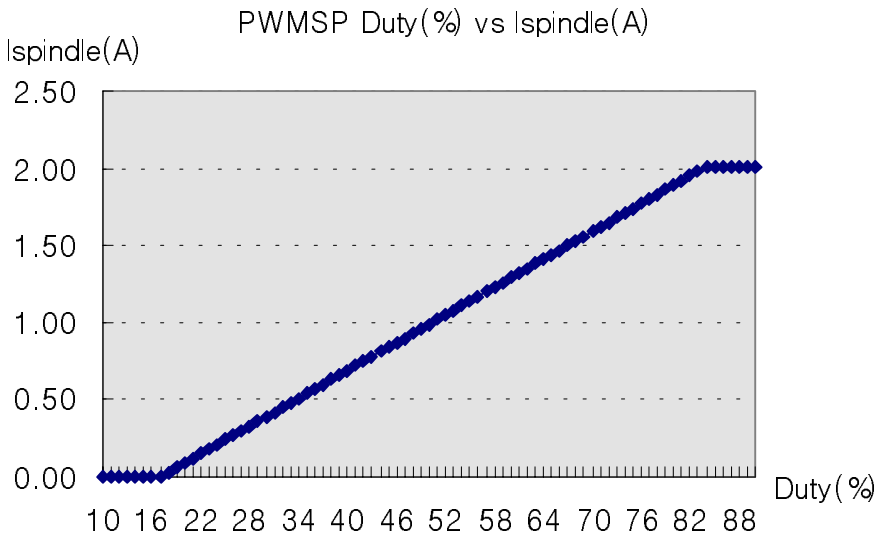


Figure 4. Spindle Current vs PWMSP Duty Variation

Start-Up Mode

The BEMF is used in the sensorless BLDC motor driver to determine the rotor position. The detected rotor position is a very important information to control the motor speed and the commutation timing.

At standstill condition, there is no BEMF voltage and no FG output. There is no information about the motor position. However the spindle motor must be started up at standstill.

To drive the spindle at the start-up mode, the digital ASIC sends the spindle enable signal via CNTL1 and supplies the HIGH or OPEN signal in turns via CNTL2 to be used as commutation signal of the spindle motor.

The digital ASIC continuously provides HIGH or OPEN signal until the BEMF generated is enough large to produce the FG signal i.e. the spindle motor can be driven by the self commutation. During a fixed time, if the BEMF generated is too small and the spindle motor is not driven by the self commutation, the ASIC resets all signals sent and retries the spindle.

Table 2. Pin Setup Truth Table

	CNTL1 (1)		CNTL2 (2)	CNTL3 (3)		GAINSEL	
	SPM Driver	Brake	S/W	VCM Driver	Retract	SPM DRIVER	VCM GAIN
High (5V)	1	0	Hard S/W	1	0	Normal	0.11
Open (Floating)	0	0	Hard S/W	0	0	x	x
Low (0V)	0	1	Soft S/W	0	1	Start up(4) Hold	0.43

NOTES:
1. CNTL1: spindle motor control
2. CNTL2: switching mode control
3. CNTL3: VCM motor control
4. Test only
5. “1”: enable; “0”: disable; “S/W”: switching

ACCELERATION MODE

When the BEMF detected is enough to be used as the information of motor position, the mode is changed from start-up to acceleration. The ASIC sends the optimum commutation timing signal via MCLK according to the FG input.

By using the BEMF, the spindle is self-commuted at acceleration and running modes. During the motor drive, the spindle motor is commuted at that point which is electrically 30° delayed after the FG_Edge generates.

RUNNING MODE

It is called to the running mode when the spindle motor speed arrives within ± 1% of the target speed. The switching mode, commutation delay time, MCLK delay time (Td) and masking time are changed at the running mode.

The spindle motor speed is controlled by PWM signal within ± 0.01%.

The soft switching using the current slope of the motor may reduce noise, EMI (Electromagnetic Interference) and spark voltage which is generated on the motor coil at the switching.

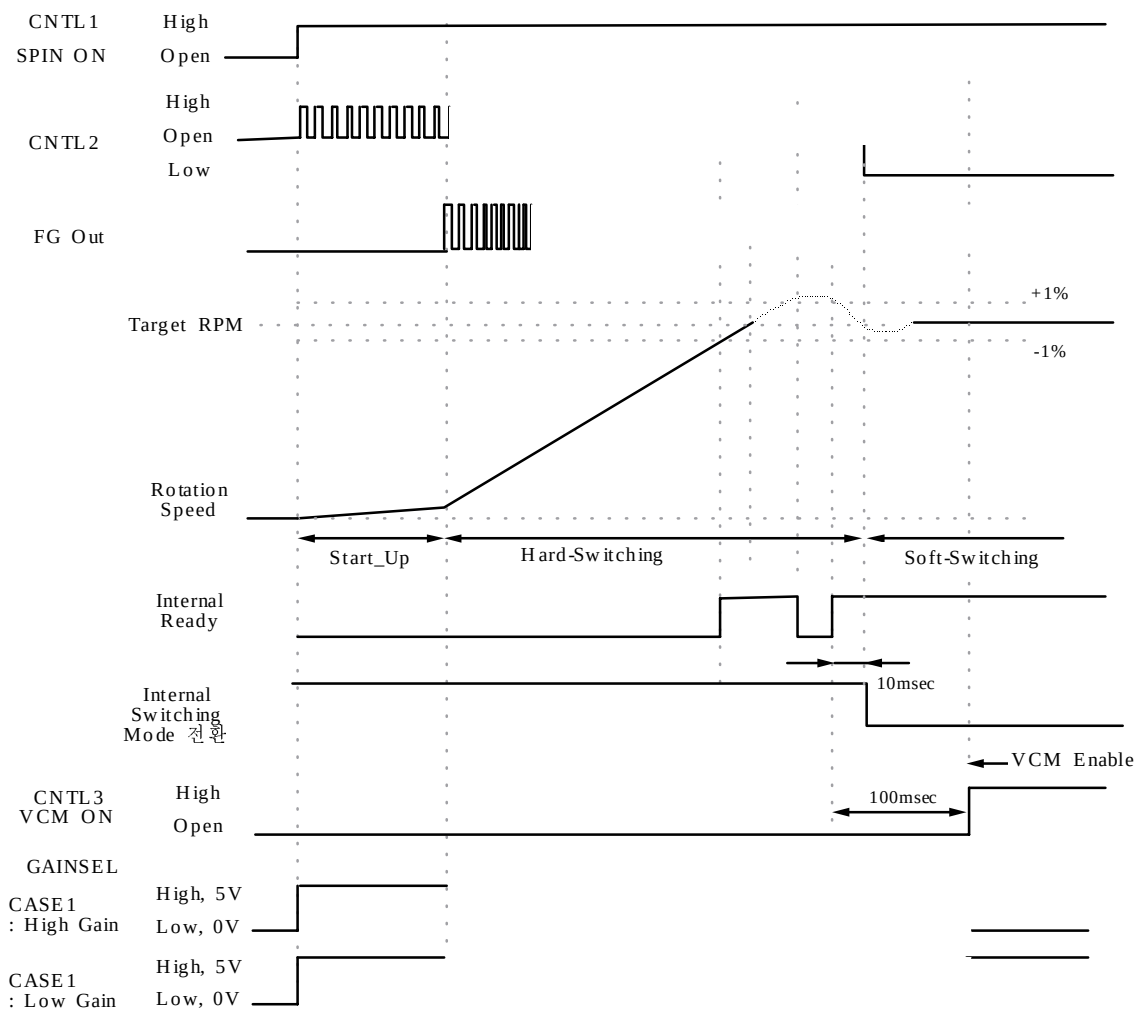


Figure 5. Motor Start-up Sequence

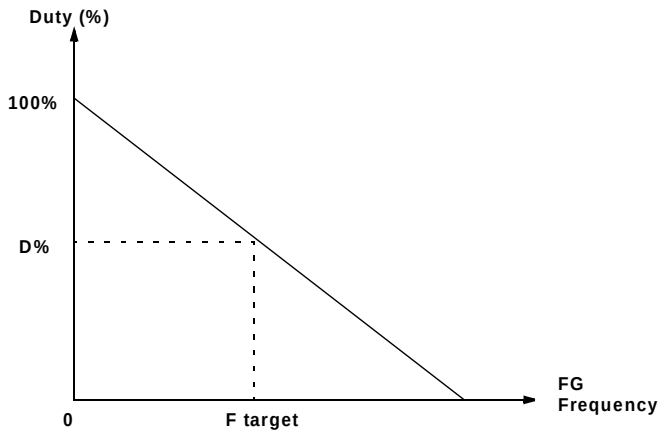
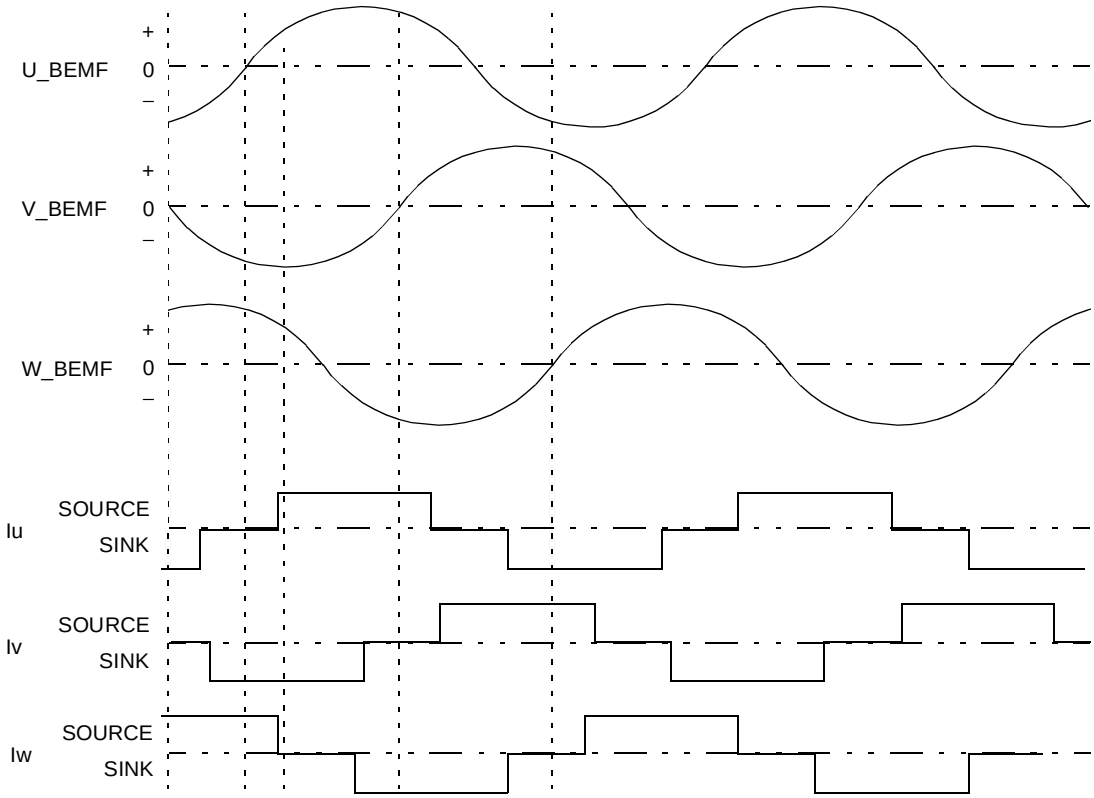


Figure 6. FG vs PWMSP Duty Variation

(1) Acceleration Mode: Hard-Switching Mode



(2) Running Mode: Soft-Switching Mode

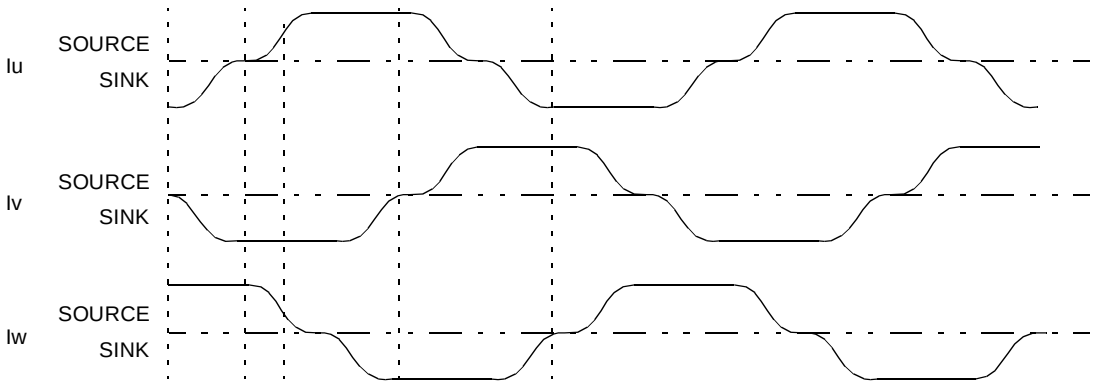


Figure 7. Acceleration and Running the Spindle Motor

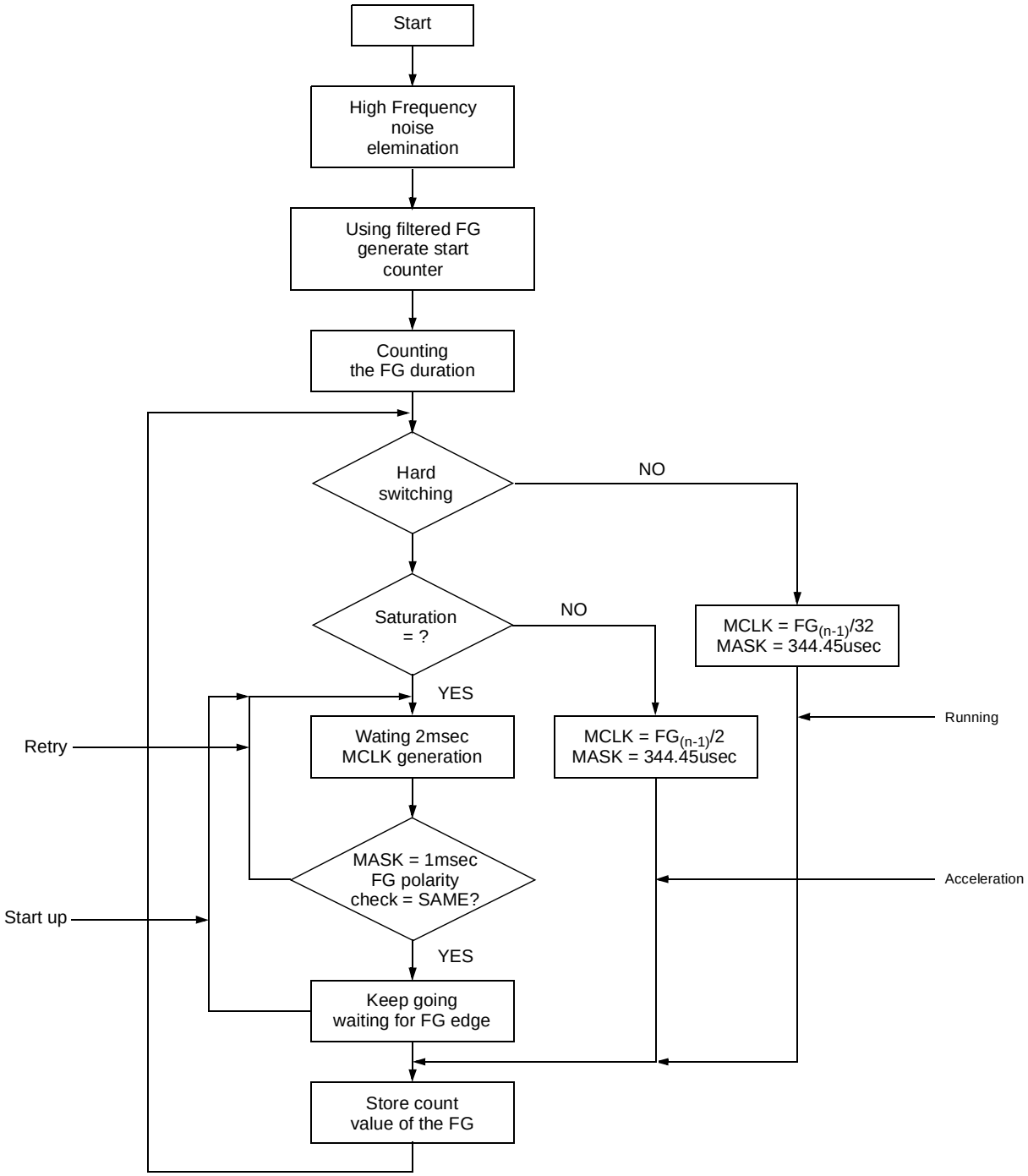


Figure 8. MCLK Generation Flow Chart

VOICE COIL MOTOR

VCM Driver

The voice coil motor drivers are the linear, class AB, H−bridge type drivers with all power devices internal to the chip. After the VCM is enabled via CNTL3, the VCM current level is controlled by two PWM signals. The input voltage level at pin PWMH weighs, at a maximum, 32 times more than the input voltage at pin PWML. These PWM signals are filtered by an internal 2nd−order low-pass filter and converted into PWMOUT (DC Voltage). The filter PWMOUT depends only on the duty factor and not on the logic level. The PWM Filter's pole is adjustable by pin CFVCM connected to the external capacitor.

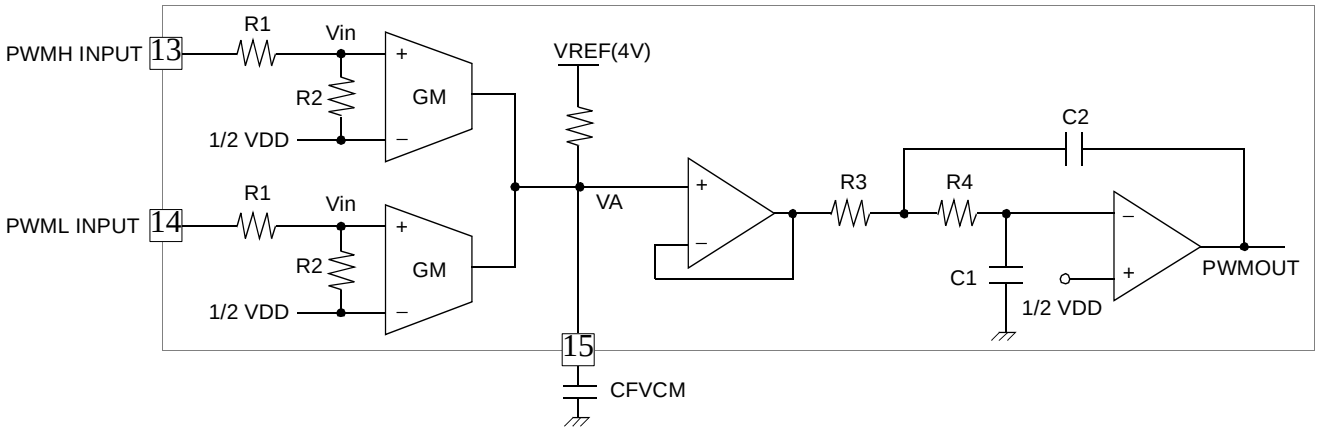


Figure 9. PWM Decoder & Filter Schematic 2

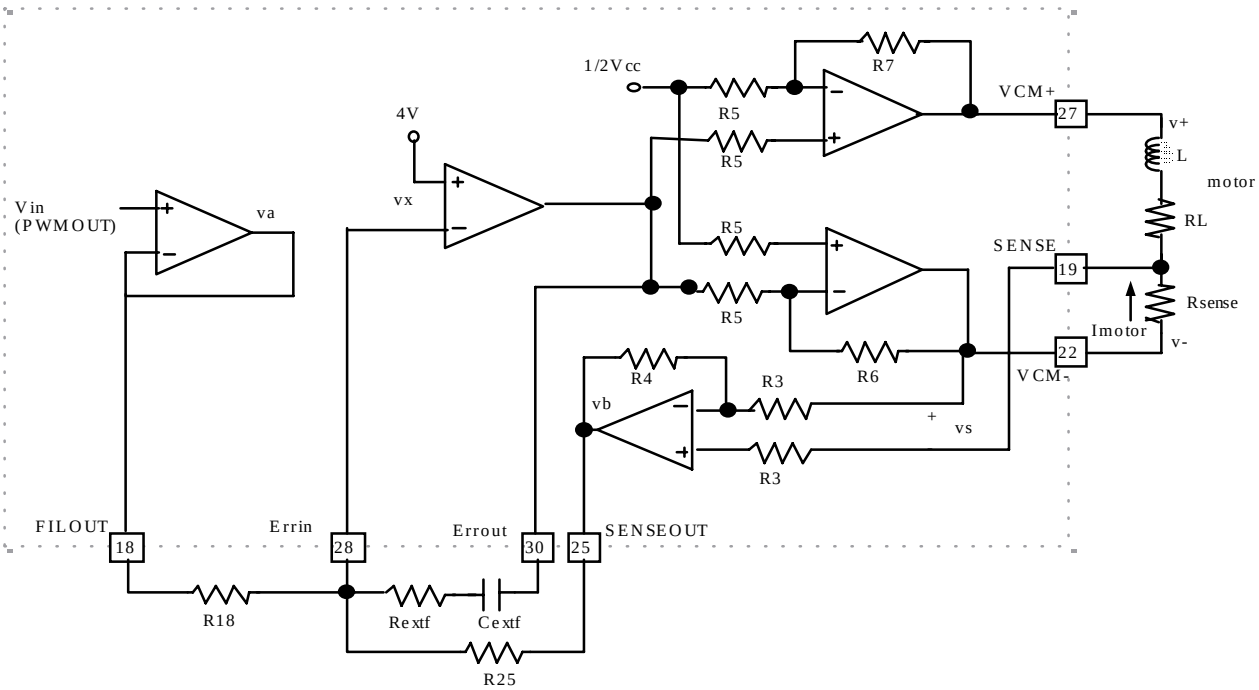


Figure 10. VCM Driver Schematic

The transconductance of VCM AMPLIFIER Gain, Gm, is:

$$Gm = \frac{Imotor}{Vin} = \frac{2 \cdot Aerror \cdot Apower \cdot R25}{2 \cdot R18 \cdot Rsense \cdot As \cdot Aerror \cdot Apower + (R18 + R25)(Zmotor + Rsense)}$$

$$Gm = \frac{Aloop}{1 + Aloop}\left(\frac{R25}{R18}\frac{1}{Rsense}\frac{1}{As}\right)$$

$$Aloop = \frac{2 \cdot R18 \cdot As \cdot Aerror \cdot Apower}{(R18 + R25)(Zmotor + Rsense)}$$

Therefore Aloop >> 1,

$$\therefore Gm \cong \frac{R25}{R18} \cdot \frac{1}{Rsense} \cdot \frac{1}{As}$$

The Transconductance (Gm) can be adjusted by selecting the external components R18, R25 and sense resister Rsense.

if R18 = 15K, R25 = 15K, Rsense = 1
GAINSEL = 0 (0V) , 1/AS = 0.43
Gm = 0.43
GAINSEL = 1 (5V) , 1/AS = 0.11
Gm = 0.11

VCM current (Imotor) is:

GAINSEL = 0 (0V)

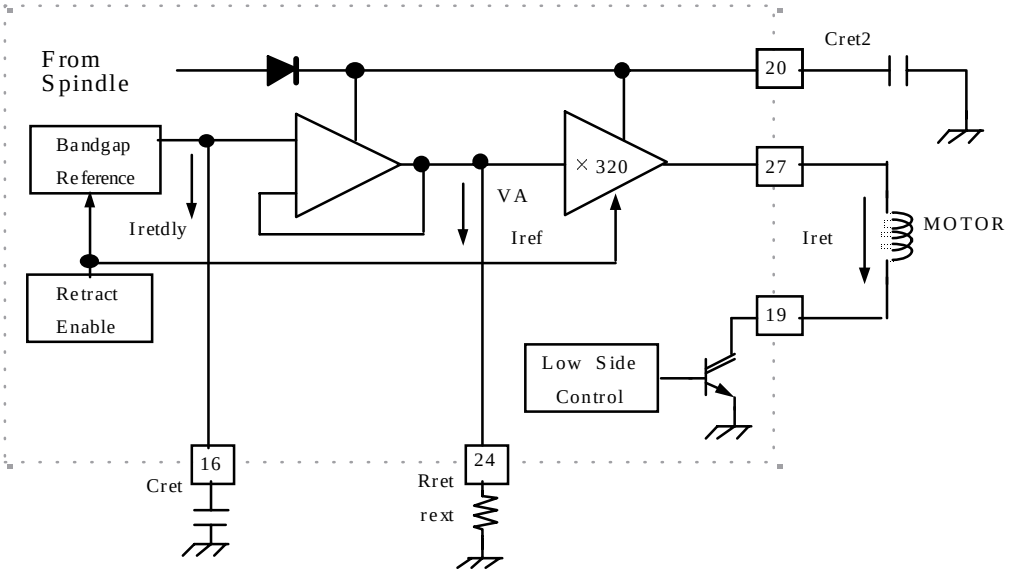
$$Imotor = 4 \times \left[(PWMH - 0.5) + \frac{1}{32}(PWML - 0.5)\right] \times \frac{R25}{R18} \times \frac{1}{Rsense} \times 0.43$$

GAINSEL = 1 (5V)

* Recommended Value*
R18 = R25 = 15K
Rsense = 1

PWMH(100%) = 1
PWMH(50%) = 0.5
PWMH(0%) = 0

$$Imotor = 4 \times \left[(PWMH - 0.5) + \frac{1}{32}(PWML - 0.5)\right] \times \frac{R25}{R18} \times \frac{1}{Rsense} \times 0.11$$



RETRACT CIRCUIT

The retract function is the operation where the VCM moves from the data zone to the parking zone when off normal state power and abnormal power interrupt cause the spindle to stop.

Figure 11. Retract Block Schematic

$$VA = Vband = 1.3V$$

$$Iref = \frac{VA}{Rext + 2K}$$

$$Iret = Iref \times 320$$

$$Tretdly = \frac{Cret \times Vband(= 1.3V)}{Iretdly(= 100u)}$$

POWER MANAGEMENT FEATURES

LOW POWER INTERRUPT:

The low power interrupt operation occurs when the power supply voltage (5V,12V) level drops below each threshold voltage. The threshold voltage (Vth) and time delay (Tdly) may be adjustable by the external component value.

$$`dly = C\frac{Vth}{I},(Vth = 2.5V, I = 12.5uA)$$

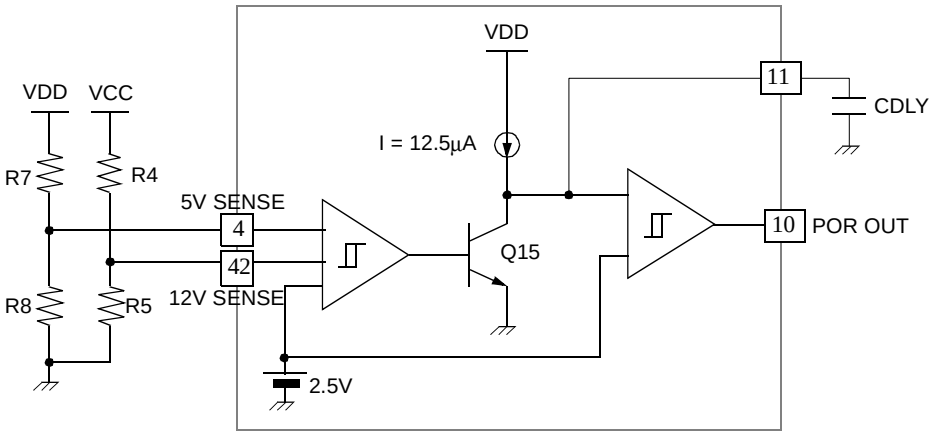


Figure 12. Power on Reset Block Schematic

POWER ON RESET

The power-on reset circuit monitors the voltage level of both +5V and +12V power supplies. The power–on reset circuit disables the spindle out block, the whole VCM block, and the digital ASIC when the power supply voltage level drops below the reference voltage.

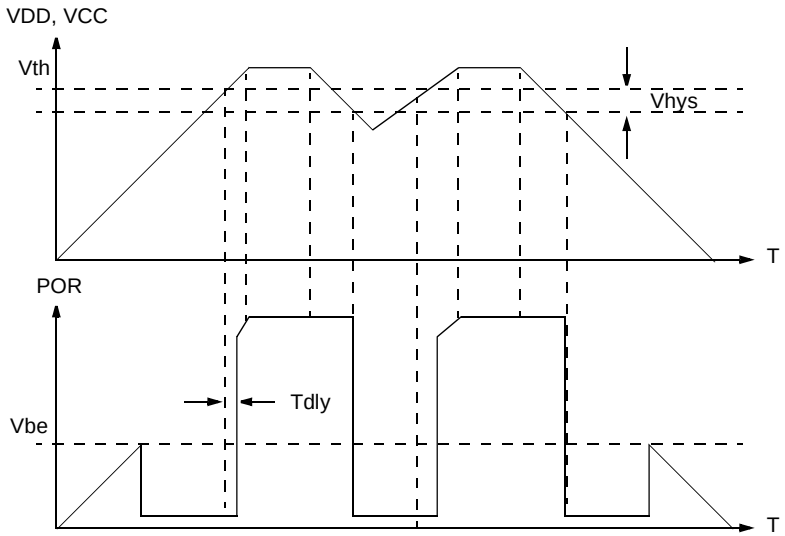


Figure 13. Power on Reset Function

$$Vhys = R10 \times I_{Q15} \cong 4.2mV$$

$$VDD; \frac{R4 + R5}{R5} \times Vhys$$

$$VCC; \frac{R7 + R8}{R8} \times Vhys$$

$$VDD,th = 2.6 \times \frac{R4 + R5}{R5} \cong 4.5V$$

$$VCC,th = 2.6 \times \frac{R7 + R8}{R8} \cong 9.5V$$

3.3V Regulator

The KA3120 includes the 3.3V regulator block which supplies power of the digital ASIC. It consists of the bias block, the band gap reference, the error amp and the external NPN power Tr. The regulator voltage level can be varied by appropriately selecting the external resistor values, R3a, R3b.

$$Vreg = Vref\left(1 + \frac{R3a}{R3b}\right)$$

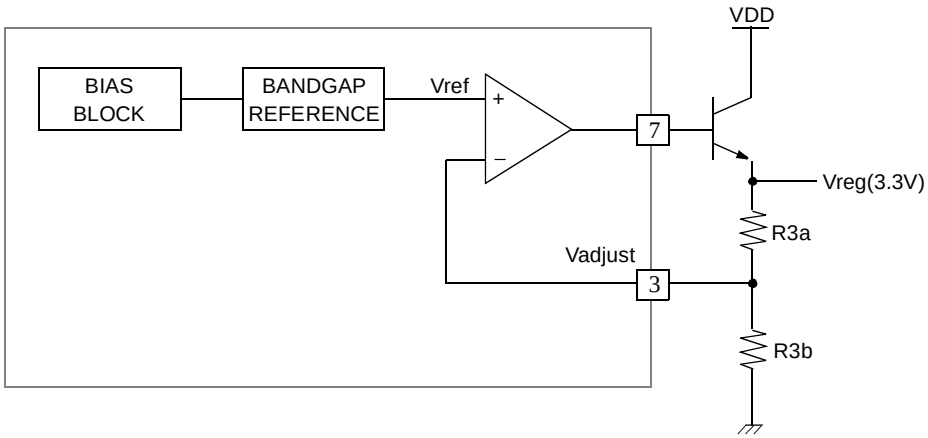


Figure 14. 3.3V Low Drop Regulator Schematic

NOTES :

1. Break Down Voltage of D20 < Maximum supply Voltage for 12V line (15V)

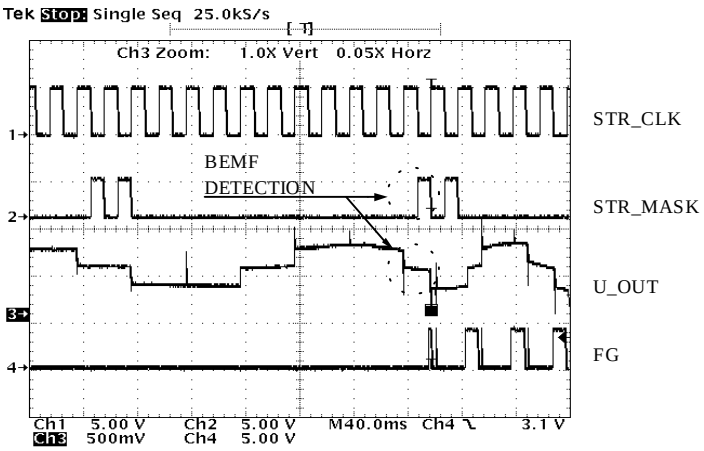


Figure 15. Start-up Mode

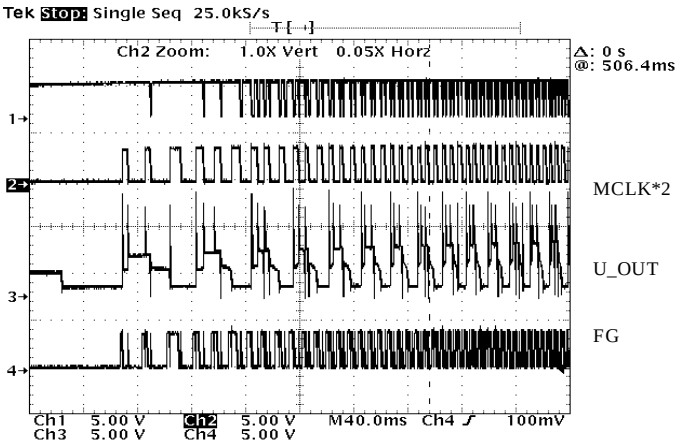


Figure 16. Acceleration Mode 1

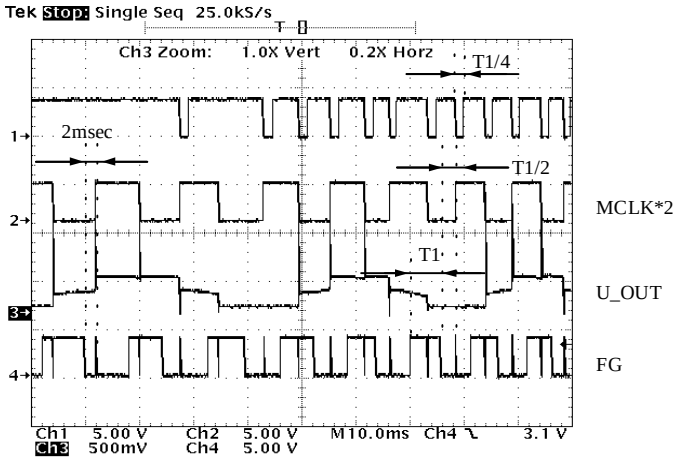


Figure 17. Acceleration Mode 2

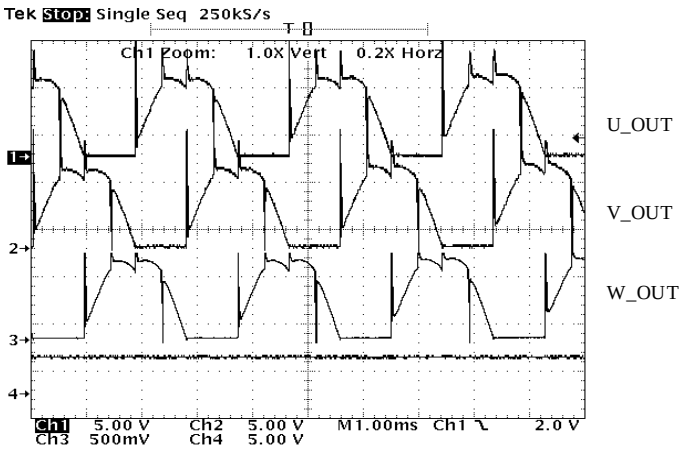


Figure 18. Output in Hard-switching Mode

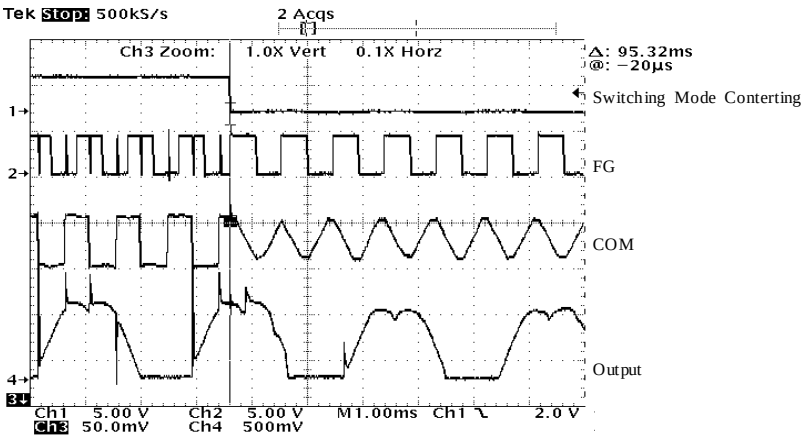


Figure 19. Switching Mode Converting

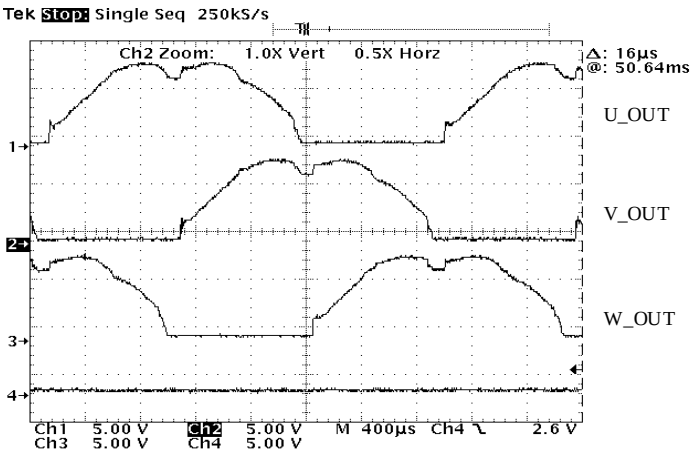


Figure 20. Soft-Switching Mode

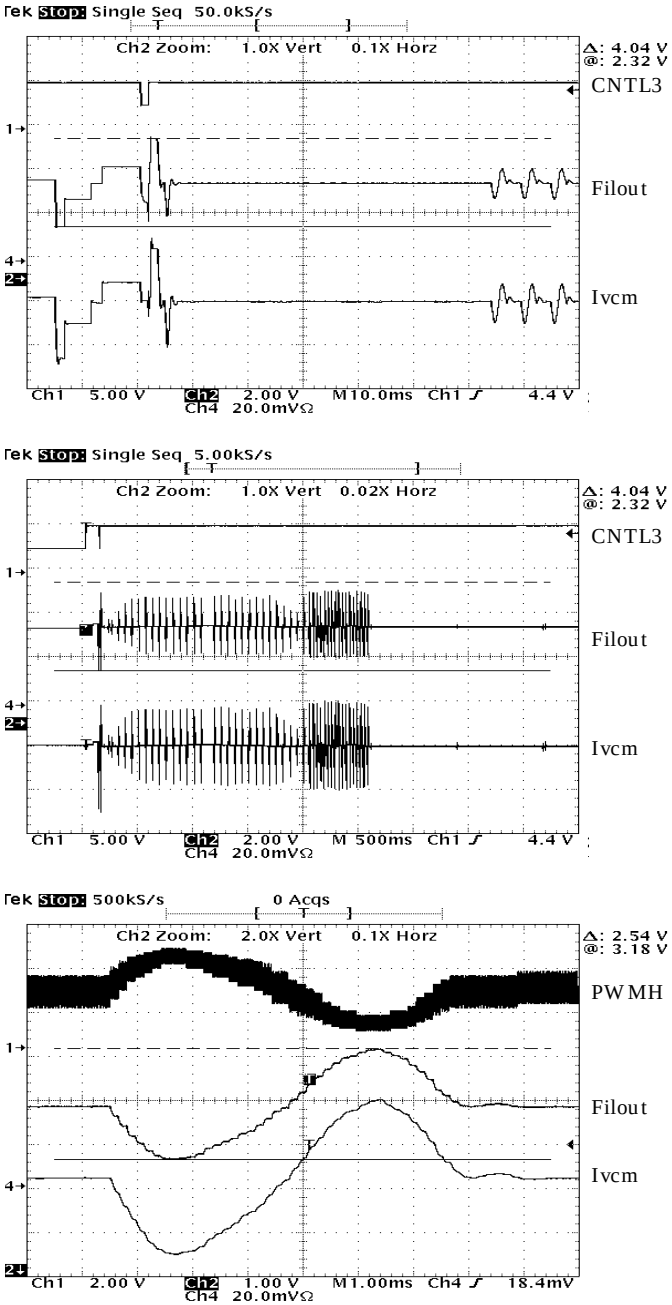


Figure 21. VCM Recalibration Flow

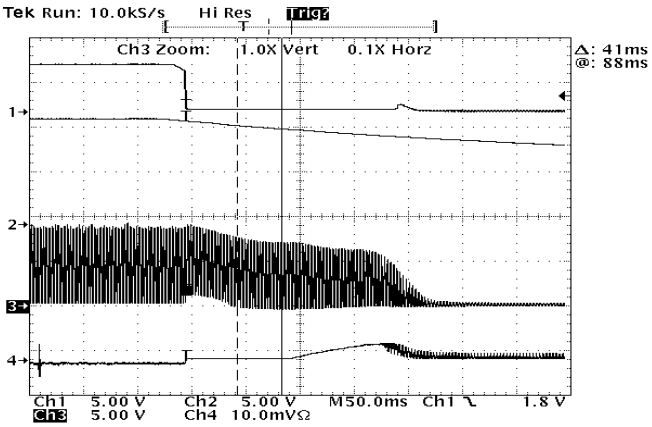
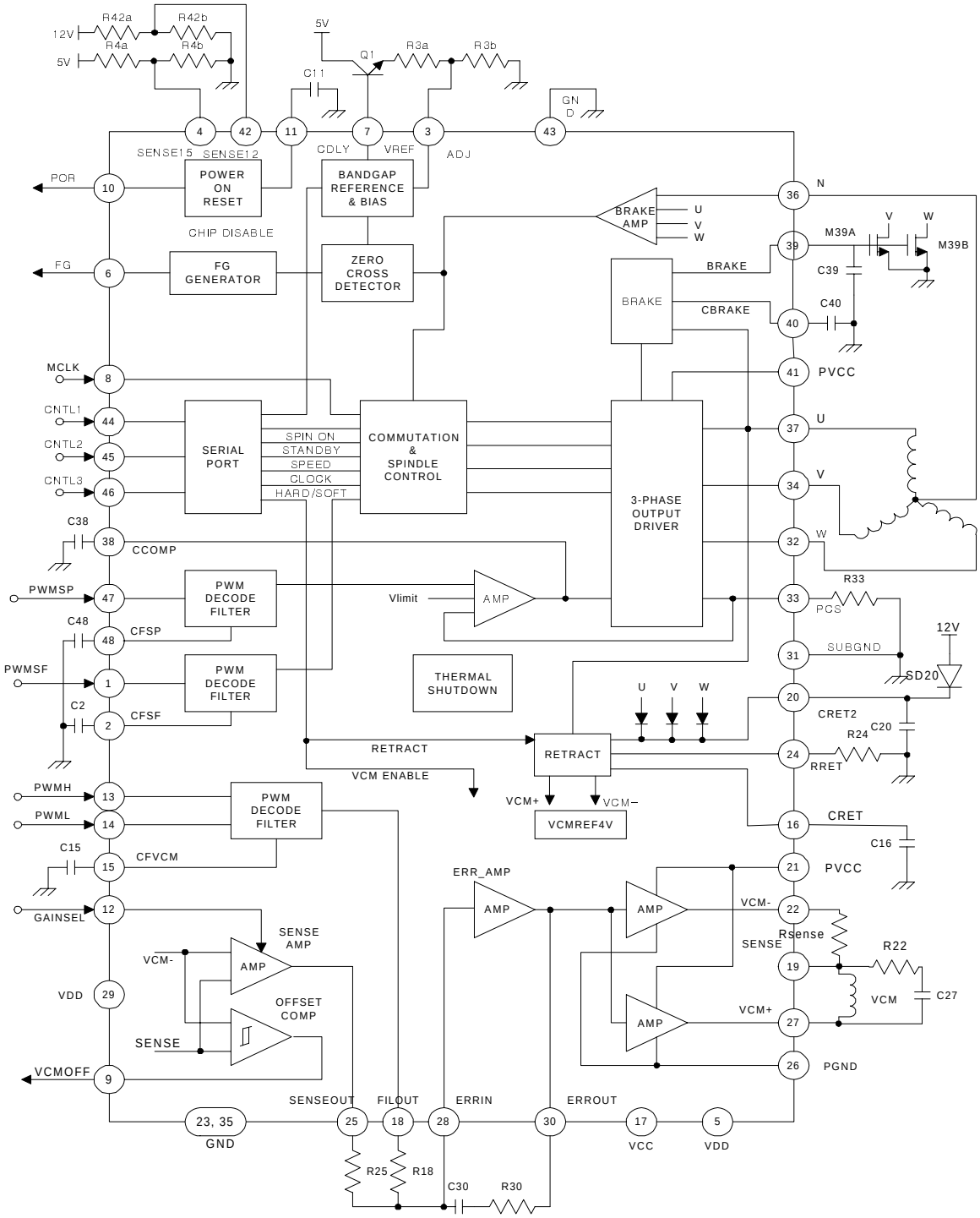


Figure 22. Retract & Break at Power off

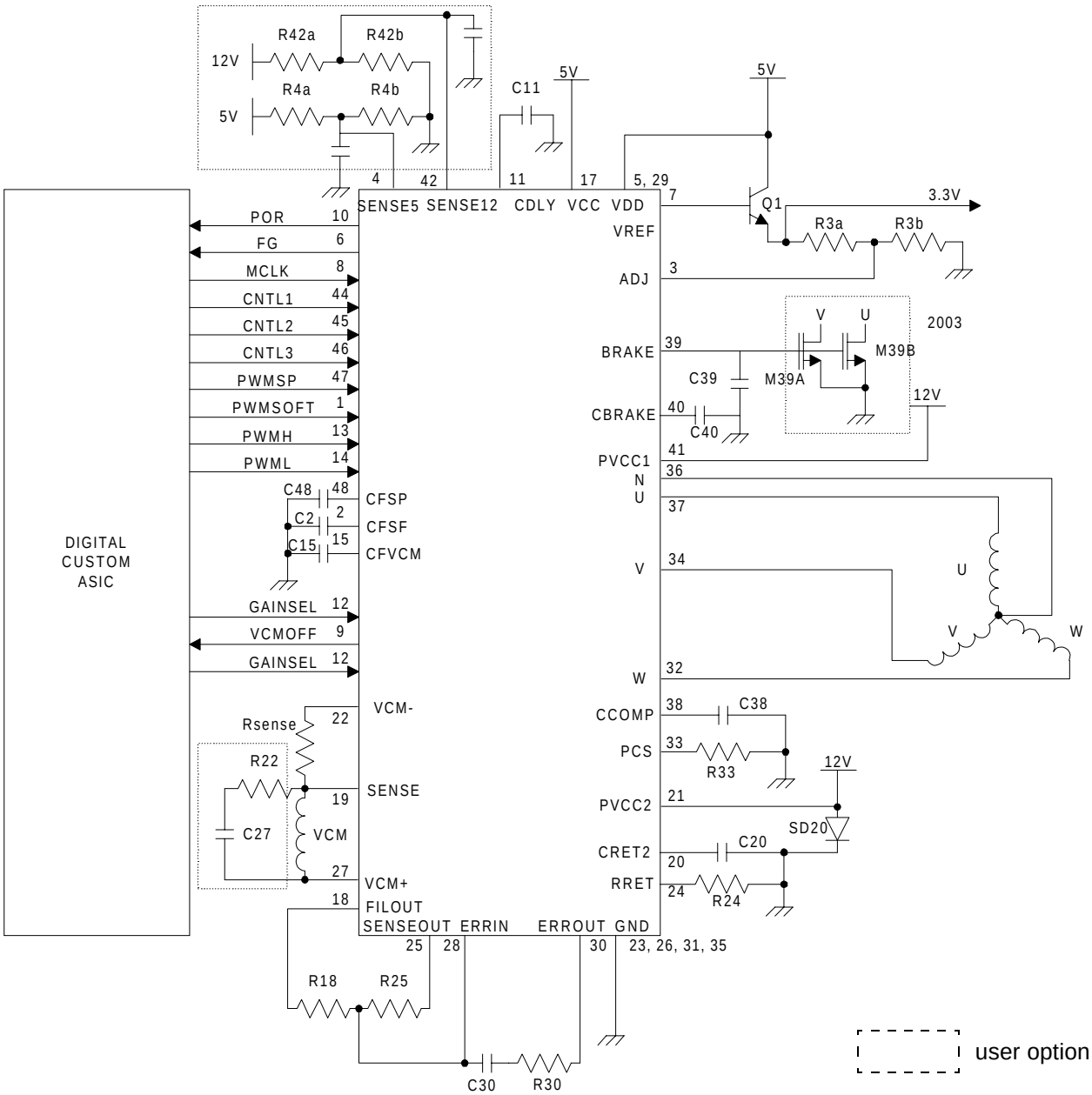
TYPICAL APPLICATION CIRCUIT



COMPONENT VALUE

Part NO	Value	Type	Part NO	Value	Type	Part NO	Value	Type	Part NO	Value	Type
R18	15K	1/4W	R4B	Option	1/4W	C27	1u	Ceramic	Q1	KSH29	D-PAK
R24	2.2K	1/4W	R42A	Option	1/4W	C30	1.2n	Ceramic	M39A	SSD2003	8SOP
R22	Option	1/4W	R42B	Option	1/4W	C38	150n	Ceramic	M39B		
R25	15K	1/4W	C2	10n	Ceramic	C40	220n	Ceramic	D20	RB4110	Schottky Diode
R30	1K	1W	C11	47n	Ceramic	C48	10n	Ceramic			
Rsense	1	1W	C15	10n	Ceramic	C39	Option	Ceramic			
R33	0.25	1/4W	C16	1u	Ceramic						
R4A	Otion	1/4W	C20	224n	Ceramic						

APPLICATION CIRCUIT



PACKAGE DIMENSION