KB22688   TV SOUND MPS FOR TWO CARRIER SYSTEM

ONE-CHIP TV SOUND MPX
(TWO - CARRIER SYSTEM)

The KB22688 is a monolithic integrated circuit designed for demodulating two carrier TV-MPX broadcast.

32-SDIP-400

FEATURES

- 1st & 2nd Sound IF
- Double-PLL FM Detection
- AGC for CCA part
- Matrix for Multi - Sound Broadcasts
- Pilot Detector
- External Control Interface
- ID Indicators (Stereo , Bilingual)

ORDERING INFORMATION

Device	Package	Operating Temperature
KB22688	32-SDIP-400	-10°C ~ + 70°C

FEATURES

- Available for Korea standard

- Non-clipping Output up to 400% modulation with AGC

- Available in DC control, Normal u-COM control or IIC

  bus control systems

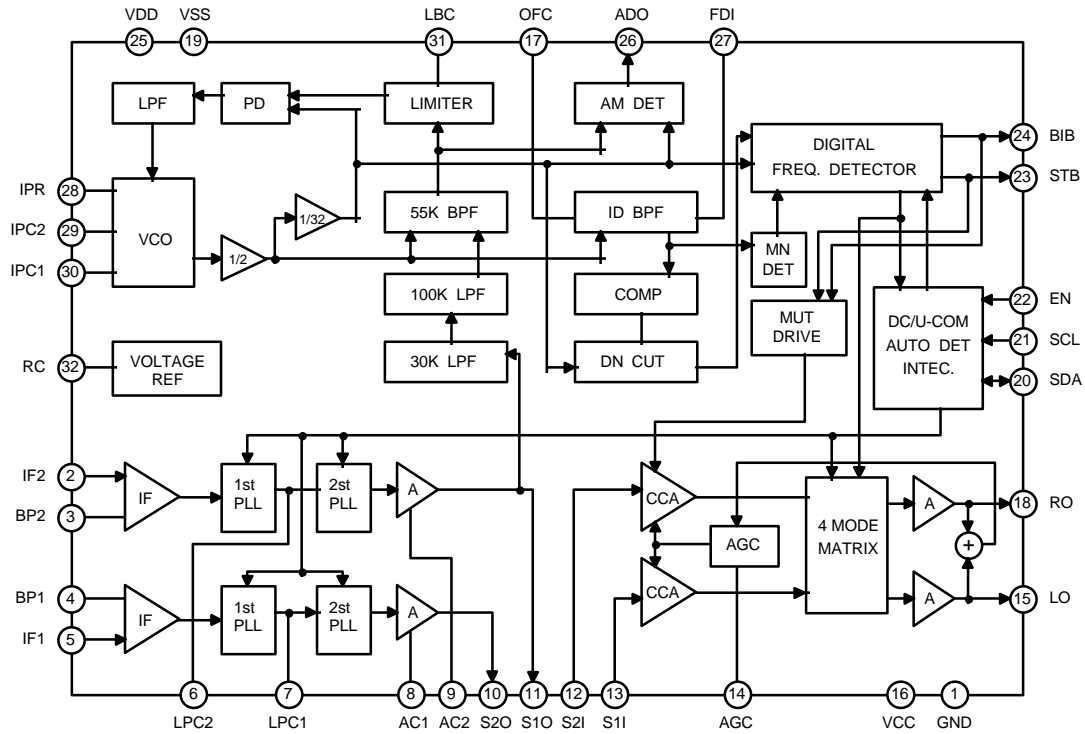- ID output : Direct LED drive or IIC serial data output

- Non-adjust

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BLOCK DIAGRAM

Pin labels (top): VDD (25), VSS (19), LBC (31), OFC (17), ADO (26), FDI (27)

Block labels: LPF, PD, LIMITER, AM DET, DIGITAL FREQ. DETECTOR, VCO, 1/32, 1/2, 55K BPF, ID BPF, MN DET, 100K LPF, COMP, MUT DRIVE, DC/U-COM AUTO DET INTEC., VOLTAGE REF, 30K LPF, DN CUT, IF, 1st PLL, 2st PLL, A, CCA, AGC, 4 MODE MATRIX, +

Left pin labels: IPR (28), IPC2 (29), IPC1 (30), RC (32), IF2 (2), BP2 (3), BP1 (4), IF1 (5)

Right pin labels: BIB (24), STB (23), EN (22), SCL (21), SDA (20), RO (18), LO (15)

Bottom pin labels: LPC2 (6), LPC1 (7), AC1 (8), AC2 (9), S2O (10), S1O (11), S2I (12), S1I (13), AGC (14), VCC (16), GND (1)

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ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Condition	Value	Unit
Maximum Supply Voltage	VCCmax		6	V
Power Dissipation	Pd		1000	mW
Operating Temperature	Topr	Vi = 0	- 10 ~ + 70	°C
Storage Temperature	Tstg		- 40 ~ + 125	°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Voltage	Vopr	4.5	5	5.5	V

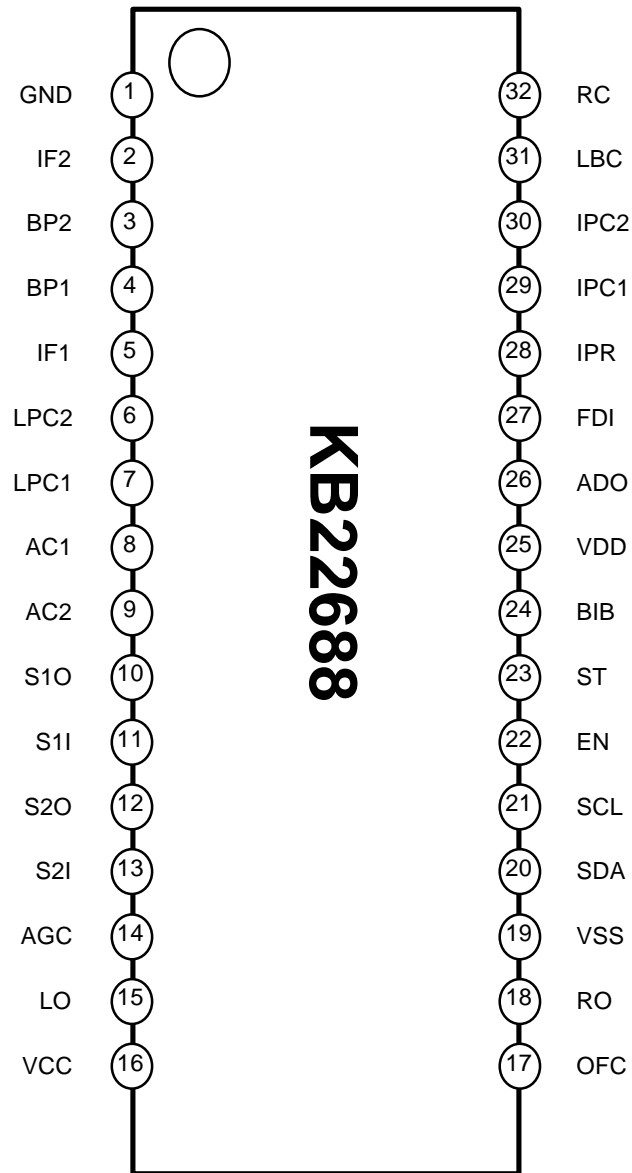## ELECTRICAL CHARACTERISTICS
(VCC = VDD = 5V, fm = 1KHz, Vi = 80dBu, Ta = 25°C, $\Delta f = \pm 25KHz$, unless otherwise specified)

Characteristics		Symbol	Condition	Min	Typ	Max	Unit
Total Circuit 1		ICC	Vi = 0	35	60	80	mA
Total Circuit 2		IDD	Vi = 0	-	-	5	mA
SIF	Input Limitng Voltage	Vlim	-	-	-	50	dBu
	AM Rejection Ratio	AMRR	AM 30 % Mod.	40	45	-	dB
	Input Impedence	Zin	-	-	1	-	Kohm
PILOT	Pilot Input Sensitivity	Vps	-	-	-	50	dBu
	ID ON time	Ton	MONO $\rightarrow$ ST,BI	-	1.0	1.5	SEC
	ID OFF time	Toff	ST, BI $\rightarrow$ MONO	-	-	0.3	SEC
MATRIX	Output Level	Vo	-	280	370	500	mVrms
	Matrix THD	THDm1	-	-	0.2	1.0	%
		THDm2	$\Delta f = \pm 100KHz$	-	0.5	10	%
	Noise Output (RF off)	Voff	Carrier OFF	-	50	370	mVrms
	Output Impedence	Zout	-	-	-	50	ohm
	Separation Ratio	SEP	$\Delta f = \pm 25$ KHz	40	45	-	dB
	Cross Talk	CT	$\Delta f = \pm 25$Khz	50	55	-	dB
	Matrix S/N Ratio	S/N	$\Delta f = \pm 25$Khz	55	60	-	dB
		S/N(st)	$\Delta f = \pm 25$ KHz (ST)	50	55	-	dB
	MUTE Attenuation ratio	Amute	$\Delta f = \pm 25$KHz	-	-66	-55	dB

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PIN CONFIGURATION

Pin	Name		Pin	Name
1	GND		32	RC
2	IF2		31	LBC
3	BP2		30	IPC2
4	BP1		29	IPC1
5	IF1		28	IPR
6	LPC2		27	FDI
7	LPC1		26	ADO
8	AC1		25	VDD
9	AC2		24	BIB
10	S1O		23	ST
11	S1I		22	EN
12	S2O		21	SCL
13	S2I		20	SDA
14	AGC		19	VSS
15	LO		18	RO
16	VCC		17	OFC

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PIN CONFIGURATION

Pin No.	Description	Pin No.	Description
1	Analog GND	17	ID Filter Offset Canceling Cap.
2	SIF 2 Input	18	R Output
3	SIF 2 Bypass	19	Digital VSS
4	SIF 1 Bypass	20	Data Input / Output (SDA)
5	SIF1 Input	21	Clock Input (SCL)
6	SIF 2 LPF Capacitor	22	Enable Input (EN)
7	SIF 1 LPF Capacitor	23	ID Indicator (Stereo)
8	SIF 1 Amplifier Capacitor	24	ID Indicator (Bilingual)
9	SIF 2 Amplifier Capacitor	25	Digital VDD
10	SIF 1 DET Output	26	AM DET Output
11	SIF 1 CCA Input	27	Freq. DET Input
12	SIF 2 DET Output	28	ID PLL VCO Resistor
13	SIF 2 CCA Input	29	ID PLL VCO Capacitor pin 1
14	AGC Detect Capacitor	30	ID PLL VCO Capacitor pin 2
15	L output	31	Limiter Bypass Capacitor
16	Analog VCC	32	Voltage Reference Capacitor

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INTERNAL PIN DESCRIPTION

Pin No	Symbol	Function	Description	Equivalent Circuit
1	GND	ANALOG GROUND	-	-
2, 5	SIF 2, SIF 1	SIF input pin	SIF signal input through a SIF filter	
3, 4	BP 2, BP 1	IF bypass pin	IF Bypass pin is Grounded with a capacitor	
6, 7	LPC 2, LPC 1	PLL LPF pin	The external capacitor extracts DC level from the 1st PLL output of FM DET	
8, 9	AC 1, AC 2	DET AMP NF Pin	Negative feedback pin of FM DET amplifier Grounded with a capacitor	

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INTERNAL PIN DESCRIPTION

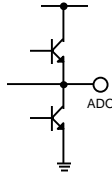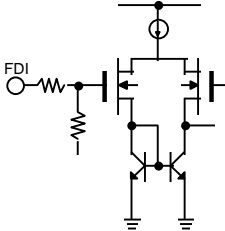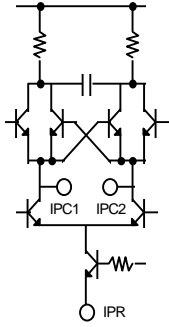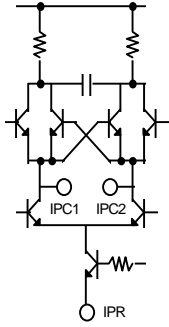| Pin No	Symbol	Function	Description	Equivalent Circuit
10, 12	S1O, S2O	FM DET Output	FM DET output pin Connedted with a De-emphasis circuit	
11, 13	S1I S2I	FM detected signal Input pin	Input pin of current control amplifier (CCA). FM detected output signal is added to this pin	
14	AGC	AGC DET PIN	AGC detect pin is grounded through a capacitor. If the signal level is over the predetermined value, this terminal's voltage will be raisen. AGC function can be deactivated by connect this terminal to GND.	
15, 18	LO, RO	MATRIX Output pin	Audio output signal is provided from this terminal	

INTERNAL PIN DESCRIPTION

Pin No	Symbol	Function	Description	Equivalent Circuit
16	VCC	ANALOG POWER	-	-
17	OFC	ID BPF OFFSET Cancel pin	The external capacitor is used to eliminate offset of ID filter .	
19	VSS	DIGITAL GROUND	-	-
20	SDA	SERIAL DATA IN & DATA OUT	It is the data communication line of IIC bus used to exchange the u-COM data and IC internal data .	
21	SCL	CLOCK SIGNAL	CLOCK line of IIC bus.	
22	EN	Enable Select PIN	It is always "H" in DC control system, always "L" in IIC bus system, and used as strobe port in nor-mal u-COM system.	
23	STB	STEREO Indicator pin	When ID is detected as "STEREO", this pin will remain "L" (OPEN DRAIN)	
24	BIB	BILINGUAL Indicator pin	When ID is detected as "Bilingual", this pin will remain "L" (OPEN DRAIN)	

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INTERNAL PIN DESCRIPTION

Pin No	Symbol	Function	Description	Equivalent Circuit
26	ADO	AM DET Output pin	AM detected signal will output from this terminal.	
27	FDI	Frequency DET IN	AM detected signal goes into this terminal coupled with a capacitor to remove DC offset.	
28	IPR	ID PLL VCO Resistor pin	Connected external resistor. This resistor is used to set VCO current .	
29, 30	IPR	ID PLL VCO Resistro pin	Connected external capacitor. This capacitor determines the oscillation freq. of VCO	

INTERNAL PIN DESCRIPTION

Pin No	Symbol	Function	Description	Equivalent Circuit
31	LBC	Limiter bypass capacitor pin	Ground through capacitor to extract DC level of output signal from the SC BPF output amplifier to the PD (Phase Detector) of ID PLL.	
32	RC	Voltage Reference Capacitor pin	Connect to capacitor to stablize the reference voltage	
25	VDD	Power Supply **(Digital)**	-	-

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OPERATION DESCRIPTION

① System

   KB22688 consists of IF AMP, FM DET, AGC, MATRIX, u-COM INTERFACE and ID DET blocks.
All blocks are non-abjust operable and available for Korea standard broadcast system.

② IF AMP BLOCK

  This block amplifies the provided IF signal to a detectable level of FM DET. Total gain is over
60dB and bandwidth is above 3 MHz .

③ FM DET

  KB22688 adopts non-adjust double-PLL type FM detection circuits.
1st PLL has a role of chasing FM carrier frequency with wide holding range (for example, hold range is
±2MHz) and 2nd PLL does actual FM detection with narrow holding range (about ± 300KHz), its free
running frequency is equal to FM carrier frequency that is detected by 1st PLL as mentioned before,
the free running frequency of 2nd PLL is determined by 1st PLL and the free running frequency of
2nd PLL can be varied according to FM carrier frequency (Korea is 4.5MHz).When 100% FM modulated
signal is provided, the amplitude of the output signal at FM output port is 100mVrms.

④ AGC

  The AGC block comprises AGC detector part and CCA part (Current control Amplifier).The MATRIX output
signal level is set to 370mVrms when applied 100% modulated FM signal and supply voltage is 5V. As the gain
of CCA is about 5dB and the gain of matrix is 6dB , so the output signal level of CCA is 185mVrms and the
matrix output is 370mVrms. If over- modulated (over 200%) FM signal is added to KB22688 input port, the output
will be clipped by supply voltage dynamic limitation range (The linear amplify range is limited lower than 800mVrms).
To prevent this problem, In KB22688 we use AGC circuit to reduce the gain of CCA part when the over- modulated
FM signal has been applied, AGC circuit is deactivated until the modulation is over 200 %. If AGC is activated,
the THD and separation characteristes of output signal would be deteriorated because the gain of CCA is varied
according to modulation ratio.

⑤ MATRIX

MATRIX part separates provided FM detected signal into MONO, STEREO, BILINGUAL, and SUB according to
braodcast status and end user's setting , it mainly consists of analog switches and operational amplifiers.
The input and output signal format of MATRIX is shown as follows.

Broadcast Mode	INPUT		
	S1	S2	Remark
STEREO	L + R	L - R	
BILINGUAL	MAIN	SUB	
MONO	MAIN	NONE *	* can be MAIN

User Select / Broadcast Mode	OUTPUT							
	STEREO		BILINGUAL		SUB		MONO	
	LOUT	ROUT	LOUT	ROUT	LOUT	ROUT	LOUT	ROUT
STEREO	2 L	2 R	L + R	L + R	L + R	L + R	L + R	L + R
BILINGUAL	MAIN	MAIN	MAIN	SUB	SUB	SUB	MAIN	MAIN
MONO	MAIN	MAIN	MAIN	MAIN	MAIN	MAIN	MAIN	MAIN

⑥ ID DET

ID signal is FM modulated to second carrier (SIF2) with a ± 2.5KHz FM modulation after AM modulated to 55KHz PILOT sub-carrier with a 50% AM modulation. ID DET part consists of 3 blocks : that is filter block for extracting pilot carrier, AM detector block for AM detection of ID signal and digital block for detecting the frequency of provided ID signal logically. In the filter block, audio signal is removed by HPF and pilot signal is extracted by the automatically adjusted switch - capacitor BPF(band pass filter) with a center frequency of 55KHz. ID signal is extracted from the pilot carrier in the AM detector block , then Digital block detects the frequency of ID signal, The ID signal can be detected in the range shown as follow:

ID	LOW OFF	LOW ON	HIGH ON	HIGH OFF
STEREO (150Hz)	125Hz	140Hz	160Hz	176Hz
BILINGUAL (276Hz)	237Hz	255Hz	300Hz	312Hz

For ID detector, the transition time from MONO to multi sound mode (STEREO or BILINGUAL) is about 1 SEC and from multi sound mode to MONO transition is about 0.3 SEC as to avoid detection error.

KB22688 has 2 types of ID output ; one is serial data out in IIC BUS u-COM control mode, the other is open drain type DC output, it can drive LED directely.

⑦ u-COM

KB22688 is available in DC control, normal u-COM control, and IIC BUS u-COM control system, and it can distinguish the control type automatically by monitoring PIN 22(EN) status. The relation of control source type and PIN 22 status is shown as follows.

	IIC BUS	NORMAL U-COM	DC CONTROL
EN (PIN 22)	always "L"	u -COM STROBE	always "H"

a) Protocol of IIC BUS u-COM control (PIN 22: L)

The KB22688 can be controlled via the 2-line IIC BUS by the u-COM. The two lines (SDA - serial data. SCL - serial clock) exchange information between the devices connected to the IIC bus. Both SDA and SCL are bidirectional lines which is connected to a positive supply voltage via a pull up resistor. When the bus is free both lined are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW data can only change when the clock signal line is LOW. A HIGH -to -LOW transition of the SDA line while SCL is HIGH is defined as a start condition. A LOW- to - HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition. The bus receiver will be reset by the reception of a start condition and is considered to be busy after the start condition. After a stop condition the bus is considered as free again.
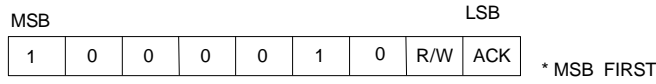
SDA ─┐ ┌─┐ 1 │ 2 │ 3 ┌ ········· ┐ 25 │ 26 │ 27 ┌─┐

SCL ─────┐ ┌┐ ┌┐ ┌┐ ····· ┌┐ ┌┐ ┌┐ ┌┐

1st Byte : 1 ~ 7th bit
8th bit - R/W   SLAVE Address : WRITE 84H, READ 85H

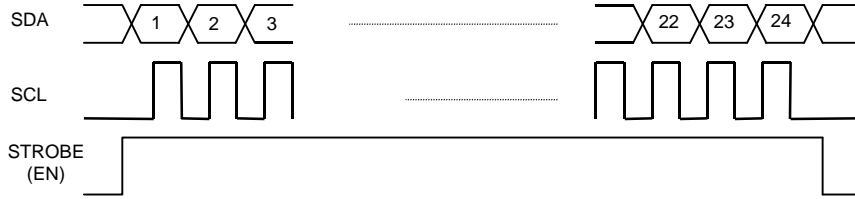9th , 18th, 27th bit ---- Acknowledge

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2nd bype : 10th ~ 17th bit   ---- SUB address (function)

3rd bype : 19th ~ 26th bit   ---- DATA (D1 ~ D8)

Data transmitted to the KB22688 starts with the module address as follows:
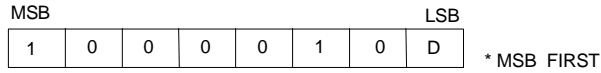
MSB							LSB	
1	0	0	0	0	1	0	R/W	ACK

* MSB FIRST

b)   Protocol of normal u-COM control (PIN 22: STROBE)

1st Byte :   1 ~ 7th bit   ----   chip select code (1000010B)

           8th bit   ----   NOT USE (don't care)

2nd Bype :   9th ~ 16th bit   ----   function assignment

3rd Bype :   17th ~ 24th bit   ----   DATA (D1 ~ D8)

The module address of KB22688 in normal u-COM control mode is as follows.

MSB							LSB
1	0	0	0	0	1	0	D

* MSB FIRST

The maximum STROBE pulse width in normal u-COM control mode should be under 6.0 mSEC. If the STROBE pulse width excess the limit, KB22688 will be changed to DC control mode.

c) Control item in each control mode

   In each control mode, control items is limited as follows.

CONTROL	MODE CHANGE	MUTE	PRE-SET	PRE-ADJUST SET	DATA TRANSMI-SSION	RECEIVE ACKNOW-LEDGE
IIC BUS	O	O	O	O	O	O
NORMAL u-COM	O	O	O	X	X	X
DC CONTROL	O	X	X	X	X	X

*** DEFINITIONS ***

      * PRE-SET : When power is ON, u-COM initials the status of KB22688 to pre-set status. (All IC has

               same pre-set status data)

* PRE-ADJUST SET : When power is ON, u-COM initials the status of KB22688 to pre-measured and

           stored status. (Different each IC)

* DATA TRANSMISSION : Transmit stored data to u-COM when u-COM requests.

* RECEIVE ACKNOWLEDGE : Return Acknowledge signal to u-COM after DATA receipt.

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d) u-COM control map

** In IIC BUS mode, SLAVE Address = WRITE : 84H, READ : 85H

** In normal u-COM mode, chip select code = 1000010B

SUB address (2nd Byte) (MSB <-> LSB)	MSB D1	D2	D3	D4	D5	D6	D7	LSB D8	Function	Remark
000XXXXX (MODE CONTROL)	0	0	X	X	X	X	X	X	MONO	END USER CONTROL
	1	0	X	X	X	X	X	X	STEREO	
	0	1	X	X	X	X	X	X	BILINGUAL	
	1	1	X	X	X	X	X	X	SUB	
001XXXXX (MUTE CONTROL)	0	X	X	X	X	X	X	X	MUTE OFF	
	1	X	X	X	X	X	X	X	MUTE ON	
010XXXXX (TEST MODE)	0	0	X	X	X	X	X	X	KOREA	IC MARKER TEST
	1	0	X	X	X	X	X	X	NOT USE	
	X	1	X	X	X	X	X	X	NOT USE	
011XXXXX	X	X	X	X	X	X	X	X	NOT USE	
100XXXXX	D1	D2	D3	D4	D5	X	X	X	SEP. ADJUST*	SET MAKER SETTING
101XXXXX	X	X	X	X	X	X	X	X	NOT USE	
110XXXXX (TEST MODE)	0	0	X	X	X	X	X	X	OPERATING	IC MAKER TEST
	1	0	X	X	X	X	X	X	NOT USE	
	X	1	X	X	X	X	X	X	NOT USE	
111XXXXX	X	X	X	X	X	X	X	X	NOT USE	

* MSB FIRST

* When power is ON, all latch datas are '0', so, KB22688 is set to MONO OFF, MUTE OFF, SEPARATION ADJUST DEFAULT (00001XXX).

* Separation Adjust Data

```
        D1D2D3D4D5              D1D2D3D4D5                D1D2D3D4D5

         0 0 0 0 0 (MIN)  <-- -  0 0 0 0 1 (TYP)    ---->  1 1 1 1 1 (MAX)
```

e) Control Function Descriptiom

* MODE CONTROL : Control the MATRIX structure according to broadcast status and end user's setting.
  KB22688 has 4 modes (MONO, STEREO, BILINGUAL and SUB)

* MUTE CONTROL : When MUTE CONTROL is on , the audio output of KB22688 is off .

* SEP. ADJUST : The separation characteristic of KB22688 in STEREO mode can be controlled by IIC BUS.
  This option controls S2 FM demodulated output signal level so as to make the separation characteristic
         in best status.

* TEST MODE : IC maker's test item.

f) DC Control Map (PIN22: H)

DC (LOGIC) INPUT		Function
SCL	SDA	
0	0	MONO
1	0	STEREO
0	1	BILINGUAL
1	1	SUB

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g) READ mode in IIC BUS u-COM control mode

  KB22688 can transmit the data which is registered inside IC to the u-COM in IIC BUS control system.

If the 8th bit of module address is "H", it means u-COM requests the data stored in the IC and KB22688 enter

data transmission mode. During the read mode, KB22688 ignores the data the data of 2nd bype (SUB address)

and transmits the internal data within the period of 3rd byte. The SDA line of u-COM should be maintain "H" to

accept transmitted data from IC. The format of read data is as follows.

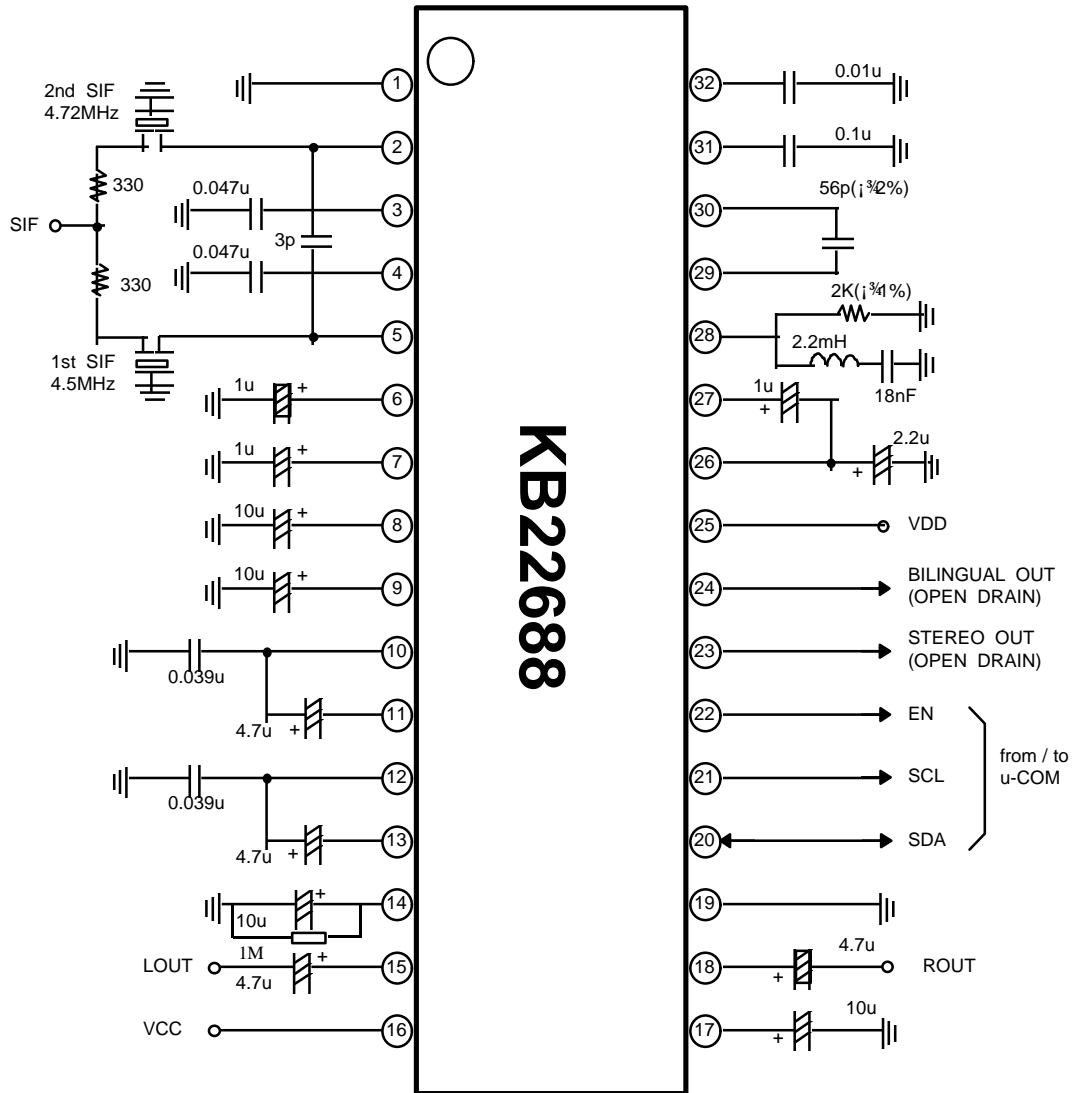| Bit of 3rd Byte	1	2	3	4	5	6	7	8
Transmit Data	BI	ST	$\overline{BI}$	$\overline{ST}$	ZC	$\overline{ZC}$	0	1
	0011 : MONO 1001 : BILINGUAL 0110 : STEREO 1100 : used in ST → BI mode transition other case : transmission error				Option for IC marker. (ZC : IC test option)			

h) Others

   In IIC BUS control system, if the SLAVE address is correct, the acknowledge signal will be generated by

KB22688 nomatter the sub address is right or wrong , When sub address is wrong IC will do nothing.

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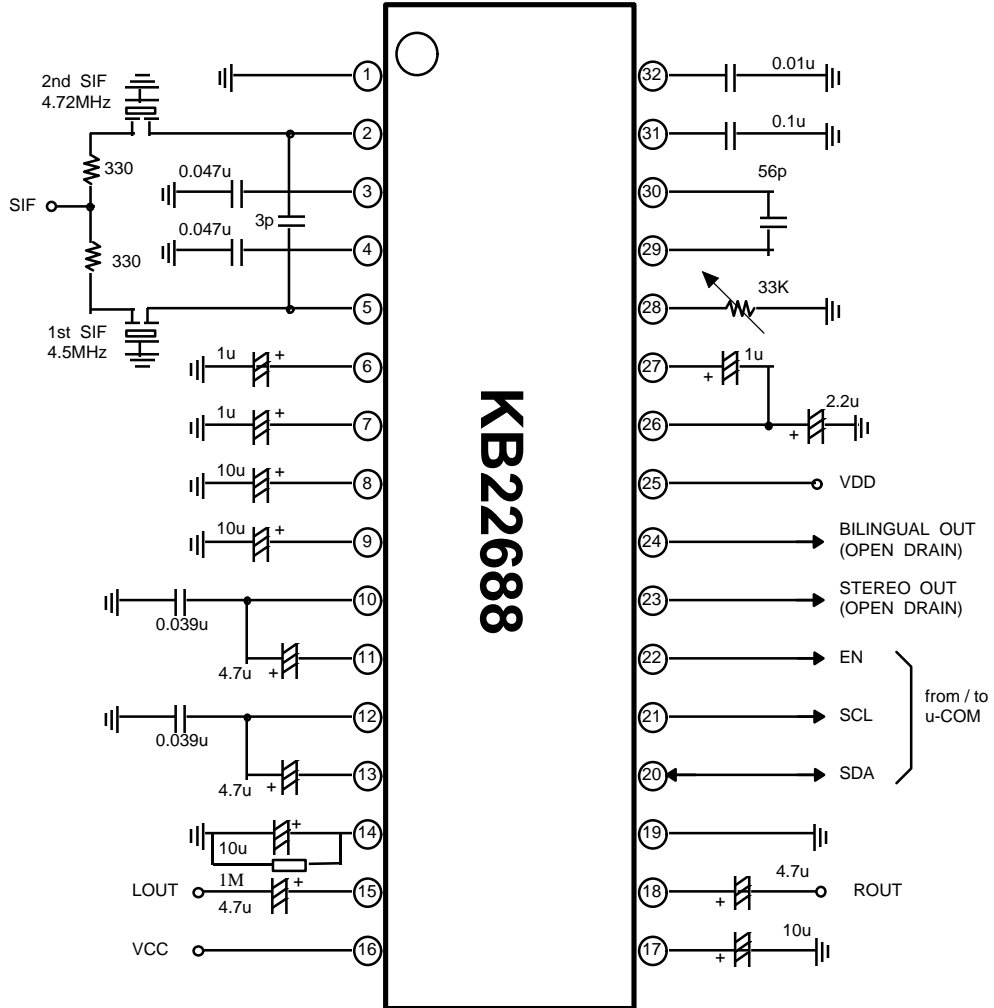
APPLICATION CIRCUIT 1 (RLC TYPE,NON-ADJUSTMENT)

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APPLICATION CIRCUIT 2 (VR TYPE,LOW COST)

2nd SIF
4.72MHz

330

SIF

0.047u

3p

0.047u

330

1st SIF
4.5MHz

1u +

1u +

10u +

10u +

0.039u

4.7u +

0.039u

4.7u +

10u +

1M

LOUT

4.7u +

VCC

KB22688

1   32   0.01u

2   31   0.1u

3   30   56p

4   29

5   28   33K

6   27   1u +

7   26   2.2u +

8   25   VDD

9   24   BILINGUAL OUT
              (OPEN DRAIN)

10   23   STEREO OUT
              (OPEN DRAIN)

11   22   EN

12   21   SCL   from / to
                         u-COM

13   20   SDA

14   19

15   18   4.7u   ROUT
              +

16   17   10u
              +
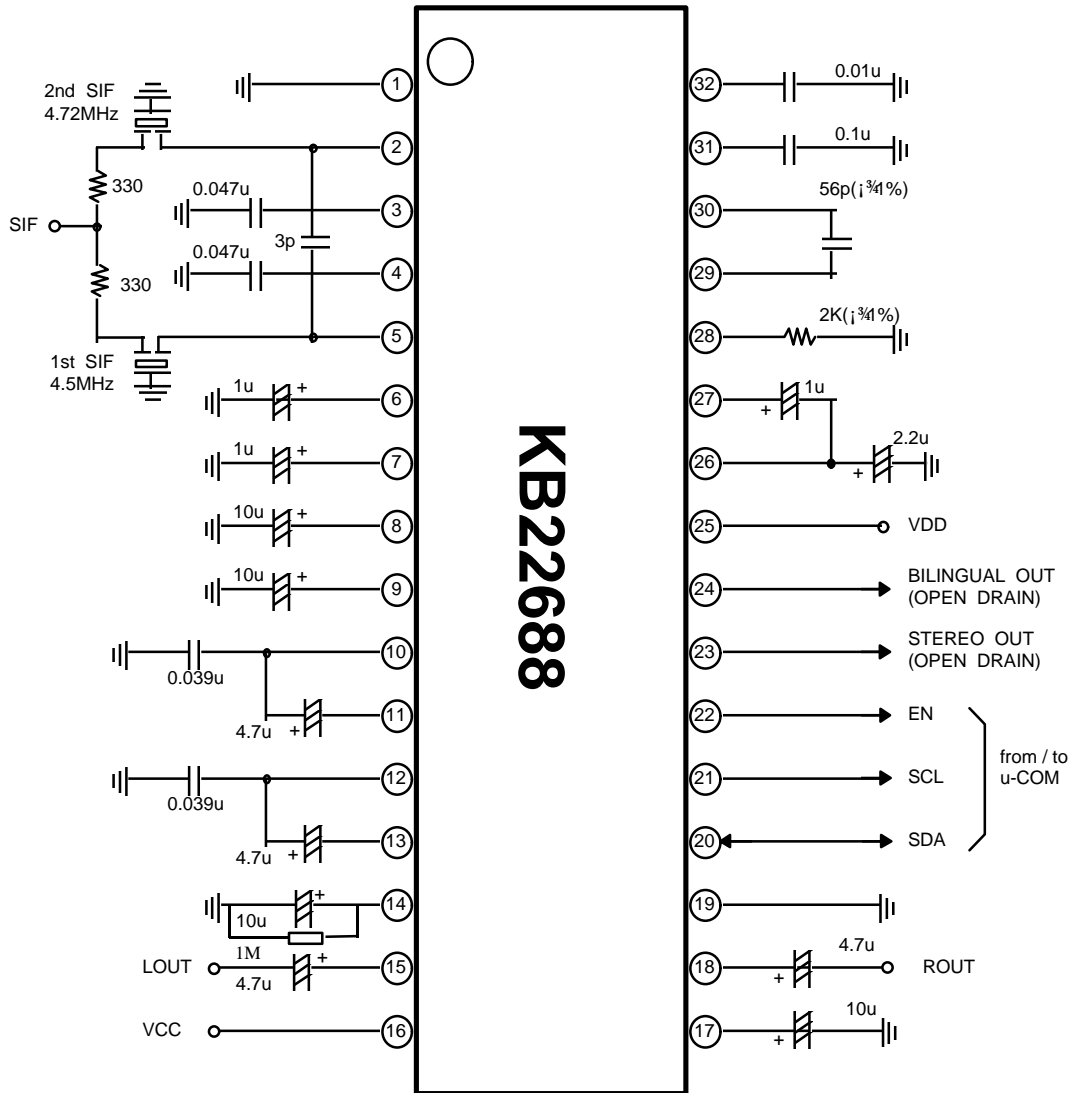
KB22688　　　　TV SOUND MPS FOR TWO CARRIER SYSTEM

APPLICATION CIRCUIT 3 (CRYSTAL TYPE,HIGH STABILITY)
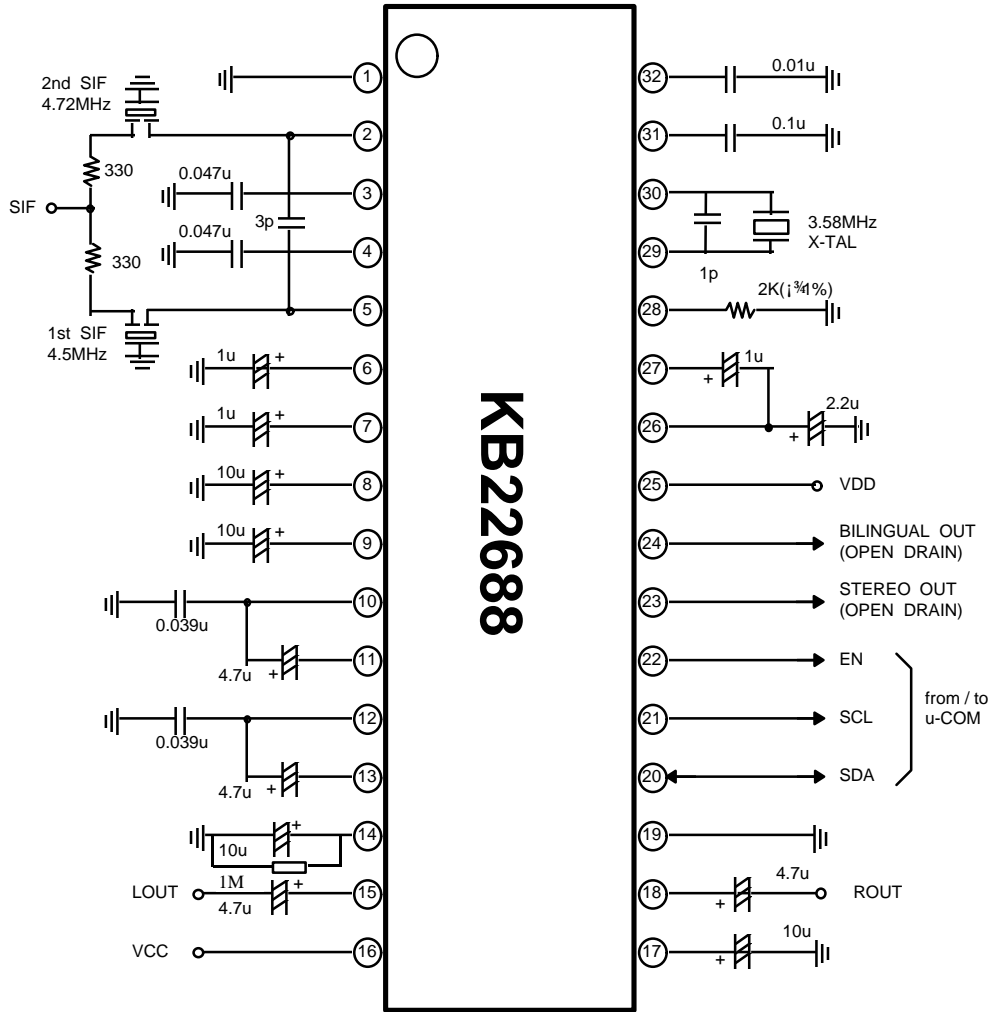
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## APPLICATION CIRCUIT 4 (RC TYPE,NON-ADJUSTMENT)

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NOTE:

1. The characteristic of SIF FILTER should be suitable to MPX sound system.

We suggest to use MURATA Co. products: SFSH4.5MCB and SFSH4.72MCB.

2. For VR type , we can adjust the variable resistor by testing the waveform of pin28,

It is not fine adjusted until the duty ratio of square wave is just 50%.
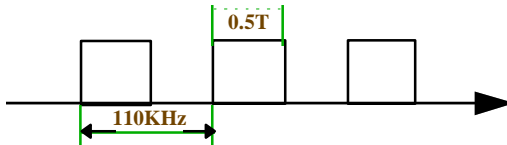
3. You can select the PLL OSC external components among 4 type:

ITEM \ TYPE	PLC	VR	CRYSTAL	RC
STABILITY	middle	low	high	middle
COST	middle	middle	high	low
AJUSTMENT	no	need	no	no
EXT. COMPONENTS	3	2	3	2

4. PROGRAM CONTROL MATHOD:

1) INSTALL: RUN   KB22688.EXE

2) KEYBOARD SETUP:

[NUMBER LOCK] --- OFF , [CAPS LOCK] --- ON

3) CONTROL MODE SELECT:

I: iiC BUS MODE ,   N: u-COM MODE ,   D: DC CONTROL MODE

4) CONTROL ITEM:

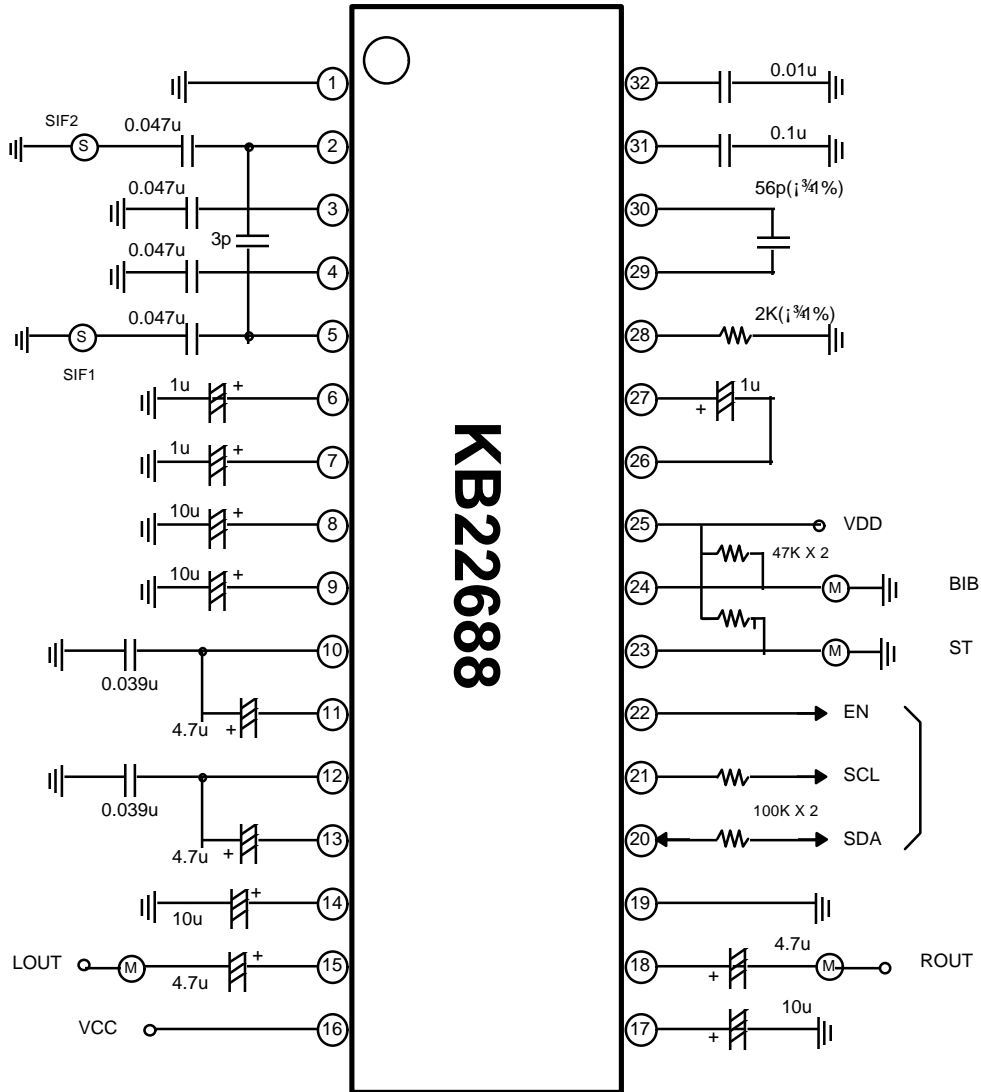MODE SELECT , MUTE SET UP , SEPERATION ADJUST.

5) EXIT:

CAP OLCK OFF , CTL+ C

5. PC Parallel prot PIN Description:

PIN	2	3	4	18
SIGNAL	SCK	SDA	EN	END

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TEST CIRCUIT

KB22688 TV SOUND MPS FOR TWO CARRIER SYSTEM

PACKAGE DIMENSION

32 - SDIP - 400

9.10 ¡¾0.2

#1

32

16

17

10.16

0.45 ¡¾0.1

(1.37)

1.00 ¡¾0.1

1.778

0.51MIN

3.80 ¡¾0.2

3.30 ¡¾0.3

5.08MAX

Dimensions in Milimeters

0 - 15¡ã

0.25 ¡¾0.1
0.15