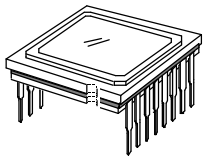
INTRODUCTION

The KC73125-M is an interline transfer CCD area image sensor developed for EIA 1/3inch video cameras.
it can be used for door phone, surveillance camera, object detection and pattern recognition.

16 Pin CERDIP



FEATURES

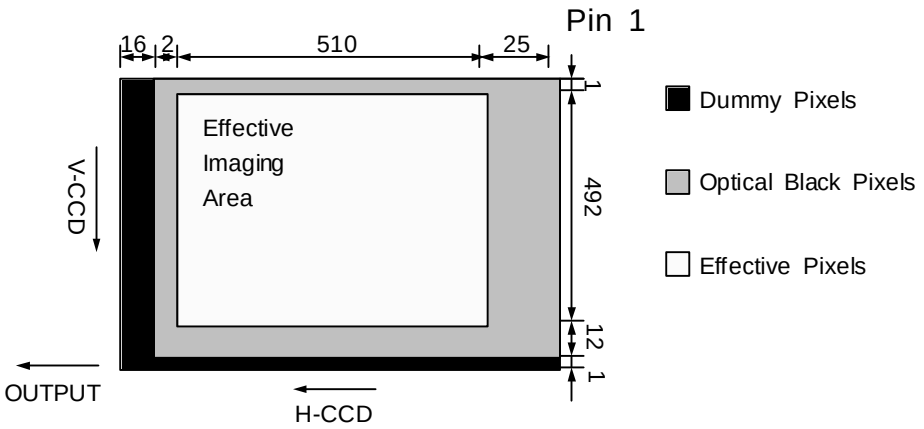
· High Sensitivity
· Optical Size 1/3inch Format
· Variable Speed Electronic Shutter
· Low Dark Current
· High antiblooming
· Low Smear
· Horizontal Register 5V Drive
· 16pin Ceramic DIP Package
· Field Integration Read Out System

ORDERING INFORMATION

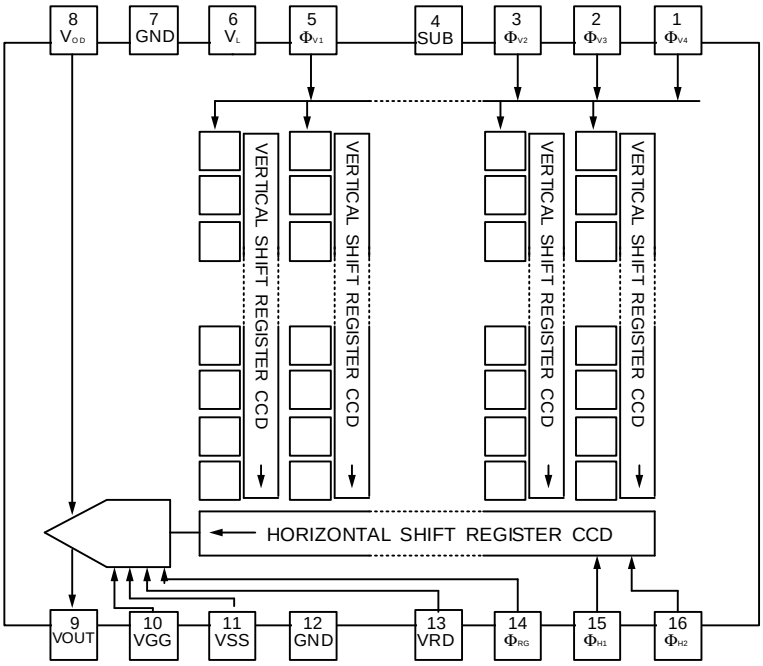
Device	Package	Operating Temperature
KC73125-M	16pin CERDIP	-10°C ~ + 50°C

STRUCTURE

· Number of total pixels : 537 (H) × 505 (V)
· Number of effective pixels : 510 (H) × 492 (V)
· Chip size : 5.90mm(H) × 5.10mm(V)
· Unit pixel size : 9.60μm(H) × 7.50μm(V)
· Optical blacks & dummies : Refer from below figure



BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Symbol	Description	Pin	Symbol	Description
1	Φ_{V4}	Vertical CCD Transfer Clock 4	9	VOUT	Signal Output
2	Φ_{V3}	Vertical CCD Transfer Clock 3	10	VGG	Output AMP Gate Voltage
3	Φ_{V2}	Vertical CCD Transfer Clock 2	11	VSS	Output AMP Source Voltage
4	SUB	Substrate Voltage	12	GND	Ground
5	Φ_{V1}	Vertical CCD Transfer Clock 1	13	VRD	Reset Drain Voltage
6	V_L	Protective Bias Voltage	14	Φ_{RG}	Charge Reset Clock
7	GND	Ground	15	Φ_{H1}	Horizontal CCD Transfer Clock 1
8	VOD	Output AMP drain Voltage	16	Φ_{H2}	Horizontal CCD Transfer Clock 2

ABSOLUTE MAXIMUM RATINGS *(1)

Characteristics	Symbols	Min.	Max.	Unit
Substrate Voltage	SUB-GND	-0.3	55	V
Supply Voltage	V_{DD},V_{OUT},V_{SS}-GND	-0.3	17	V
Vertical Clock Input Voltage	Φ_{V1},Φ_{V2},Φ_{V3},Φ_{V4}-GND	-10	20	V
	Φ_{V1},Φ_{V2},Φ_{V3},Φ_{V4}-V_L	-0.3	30	V
Horizontal Clock Input Voltage	Φ_{H1},Φ_{H2} - GND	-0.3	17	V
Voltage Difference between Vertical and Horizontal Clock Input Pins	Φ_{V1},Φ_{V2},Φ_{V3},Φ_{V4}	-20	20	V
	Φ_{H1},Φ_{H2}	-17	17	V
	Φ_{H1},Φ_{H2} - Φ_{V4}	-17	17	V
Output Clock	Φ_{RG},V_{GG} - GND	-0.3	17	V
Protection Circuit Bias Voltage	V_L - SUB	-65	0.3	V
Operating Temperature	T_{OPR}	-10	50	°C
Storage Temperature	T_{STG}	-30	80	°C

* (1) The device can be destroyed, If the applied voltage or temperature is higher than the absolute maximum rating voltage or temperature.

DC CONDITIONS

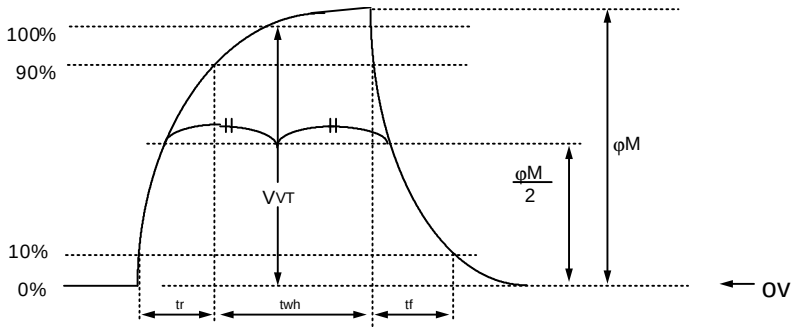
Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Output Stage Drain Bias	V_{DD}	14.55	15.0	15.45	V	
Output Stage Gate Voltage	V_{GG}	1.75	2.0	2.25	V	
Output Stage Source Voltage	V_{SS}	Ground through 680Ω			V	±5%
Substrate Voltage Adjustment Range	V_{SUB}	8.0		19.0	V	
Fluctuation Voltage Range after Substrate Voltage Adjusted	ΔV_{SUB}	-3		3	%	
Reset Gate Voltage Adjustment Range	V_{RGL}	1.0	2.0	4.0	V	
Fluctuation Voltage Range after Reset Gate Voltage Adjusted	ΔV_{RGL}	-3		3	%	
Protection Circuit Bias Voltage	V_L	V_{VL} voltage of the vertical clock waveform				
Output Stage Drain Current	I_{DD}		2.5		mA	

CLOCK VOLTAGE CONDITIONS

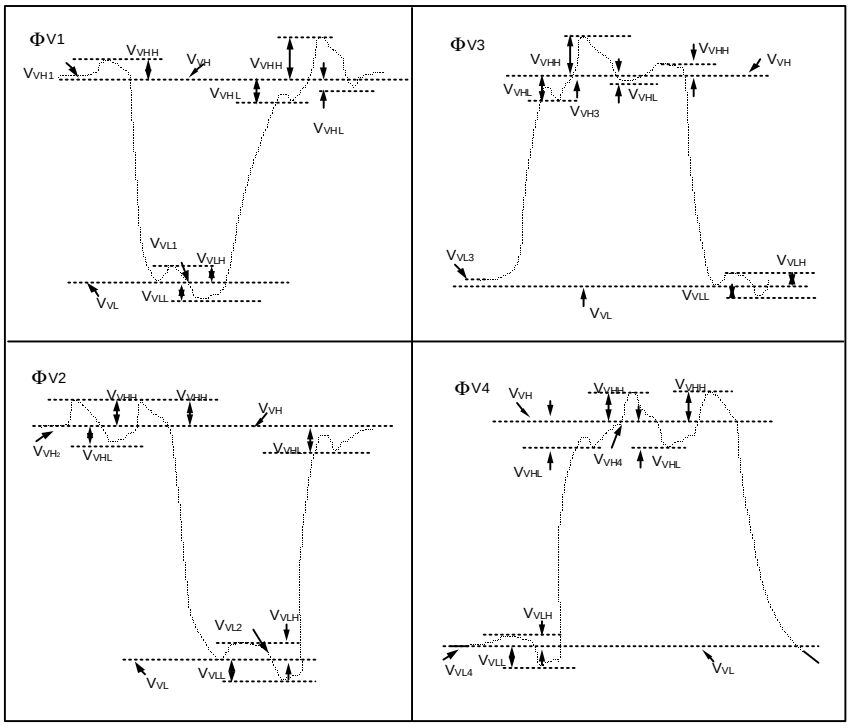
Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Read-out Clock Voltage	V_{VT}	14.55	15.0	15.45	V	High level
Vertical Transfer Clock Voltage	V_{VH1}~V_{VH4}	-0.05	0.0	0.05	V	$V_{VH}=(V_{VH1+}V_{VH2})/2$
	V_{VL1}~V_{VL4}	-9.0	-8.5	-8.0	V	$V_{VL}=(V_{VL3+}V_{VL4})/2$
Horizontal Transfer Clock Voltage	$V_{\phi H}$	4.75	5.0	5.25	V	High
	V_{HL}	-0.05	0.0	0.05	V	Low
Charge Reset Clock Voltage	$V_{\phi RG}$	4.75	5.0	5.25	V	High
	V_{RGLH}-V_{RGLL}			0.8	V	Low
Substrate Clock Voltage	$V_{\Phi SUB}$	20.0	23.5	25.0	V	Shutter

DRIVE CLOCK WAVEFORM CONDITIONS

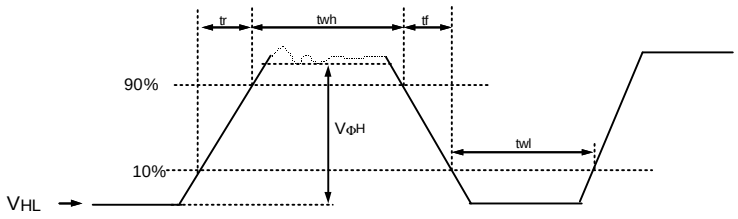
(1) Read out clock waveform



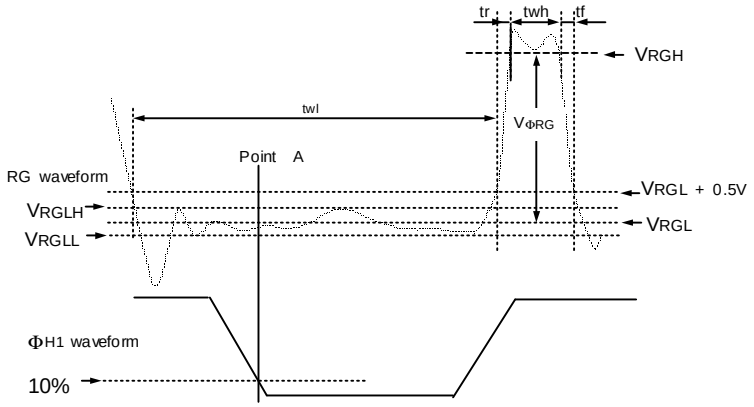
(2) Vertical transfer clock waveform



(3) Horizontal transfer clock waveform diagram



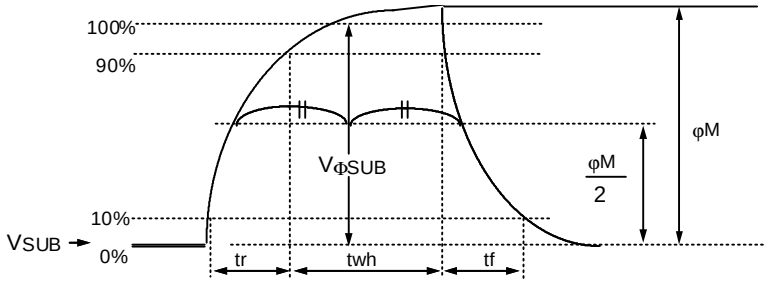
(4) Reset gate clock waveform diagram



V_{RGLH} is the maximum value and V_{RGLL} the minimum value of the coupling waveform in the period from Point A in the diagram about to RG rise

$V_{RGL}=(V_{RGLH}+V_{RGLL})/2$, $V_{\varphi RG}=V_{RGH}-V_{RGL}$

(5) Substrate clock waveform



CLOCK EQUIVALENT CIRCUIT CONSTANT

Item	Symbol	Typ.	Unit	Remark
Capacitance between Vertical Transfer Clock and GND	$C_{\phi V1}$, $C_{\phi V3}$	1,300	pF	
	$C_{\phi V2}$, $C_{\phi V4}$	1,300	pF	
Capacitance between Vertical Transfer Clocks	$C_{\phi V12}$, $C_{\phi V34}$	600	pF	
	$C_{\phi V23}$, $C_{\phi V41}$	230	pF	
	$C_{\phi V13}$	120	pF	
	$C_{\phi V24}$	90	pF	
Capacitance between Horizontal Transfer Clock and GND	$C_{\phi H1}$, $C_{\phi H2}$	38	pF	
Capacitance between Horizontal Transfer Clocks	$C_{\phi H12}$	38	pF	
Capacitance between Reset Gate Clock and GND	$C_{\phi RG}$	10	pF	
Capacitance between Substrate Clock and GND	$C_{\phi SUB}$	1120	pF	
Vertical Transfer Clock Serial Resistor	$R_{\phi V1}$ ~ $R_{\phi V4}$	40	Ω	
Vertical Transfer Clock Ground Resistor	R_{GND}	15	Ω	
Horizontal Transfer Clock Serial Resistor	$R_{\phi H1}$, $R_{\phi H2}$	10	Ω	
Reset Gate Clock Serial Resistor	$R_{\phi RG}$	100	Ω	

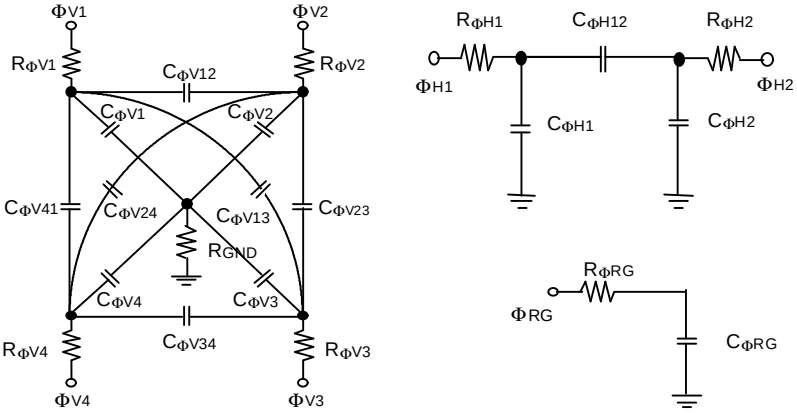


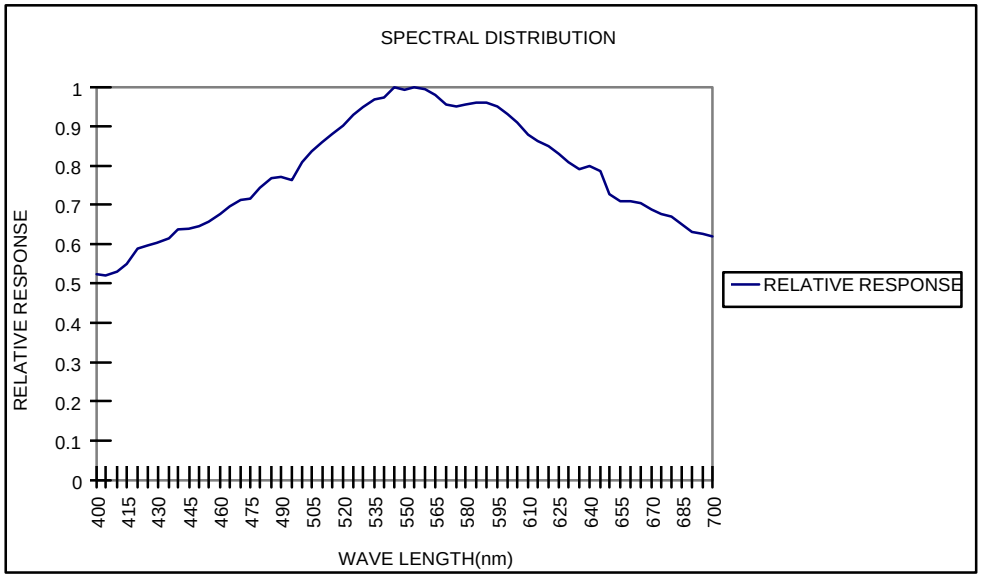
IMAGE SENSOR CHARACTERISTICS

(Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remark
Sensitivity	S	40	45		mV/lux	1	
Saturation Signal	Y_{SAT}		600		mV	2	
Smear	SM			0.015	%	3	
Blooming Margin	BM	1,000			times	4	
Uniformity	U			20	%	5	
Dark Signal	D			2	mV	6	Ta=50°C
Flicker Y	F_Y			2	%	7	

SPECTRAL RESPONSE CHARACTERISTICS

(Excluding light source characteristics)



TEST CONDITION

1) Use a light source with color temperature of 3,200K The light source is adjusted in accordance with the average value of Y signals indicated in each item.

2) Through the following tests the substrate voltage and reset gate clock are set to the value of bias condition while the device condition are at the typical value of the bias and clock conditions.

3) Through the following tests, defects are excluded and unless otherwise specified the optical black level (hence forth referred as OB) is set for the reference of the output signal which is taken as the Y signal output.

TEST METHODS

1. Measure the light intensities (L) when the averaged illuminance output value (Y) is the standard illuminance output value, 150mV (Y_A) and when half of 150mV (1/2 Y_A).

$$S = \frac{Y_A - \frac{1}{2}Y_A}{L_{Y_A} - L_{\frac{1}{2}Y_A}}$$

2. Adjust the light intensity to 10 times that of Y signal output average value (Y_A = 150mV) , then test Y signal minimum value ($Y=Y_{SAT}$).

3. Adjust the light intensity to 500 times that of Y signal output average value (Y_A=150mV), then remove the read-out clock and drain the signal in photosensors by the electronic shutter operation in al l the respective horizontal blanking times with the other clocks unchanged. Measure the maximum illuminance output value (Y_{SM}).

$$SM = \frac{Y_{SM}}{Y_A} \times \frac{1}{500} \times \frac{1}{10} \times 100(\%)$$

4. Adjust the light indensity to 1000 times that of Y signal output average vlaue (YA = 150mV), then confirm that Blooming dose not appear.

5. Measure the maximum and minimum illuminance output value (Y_{MAX}, Y_{MIN}) when the light Intensity is adjusted to make Y to be YA.

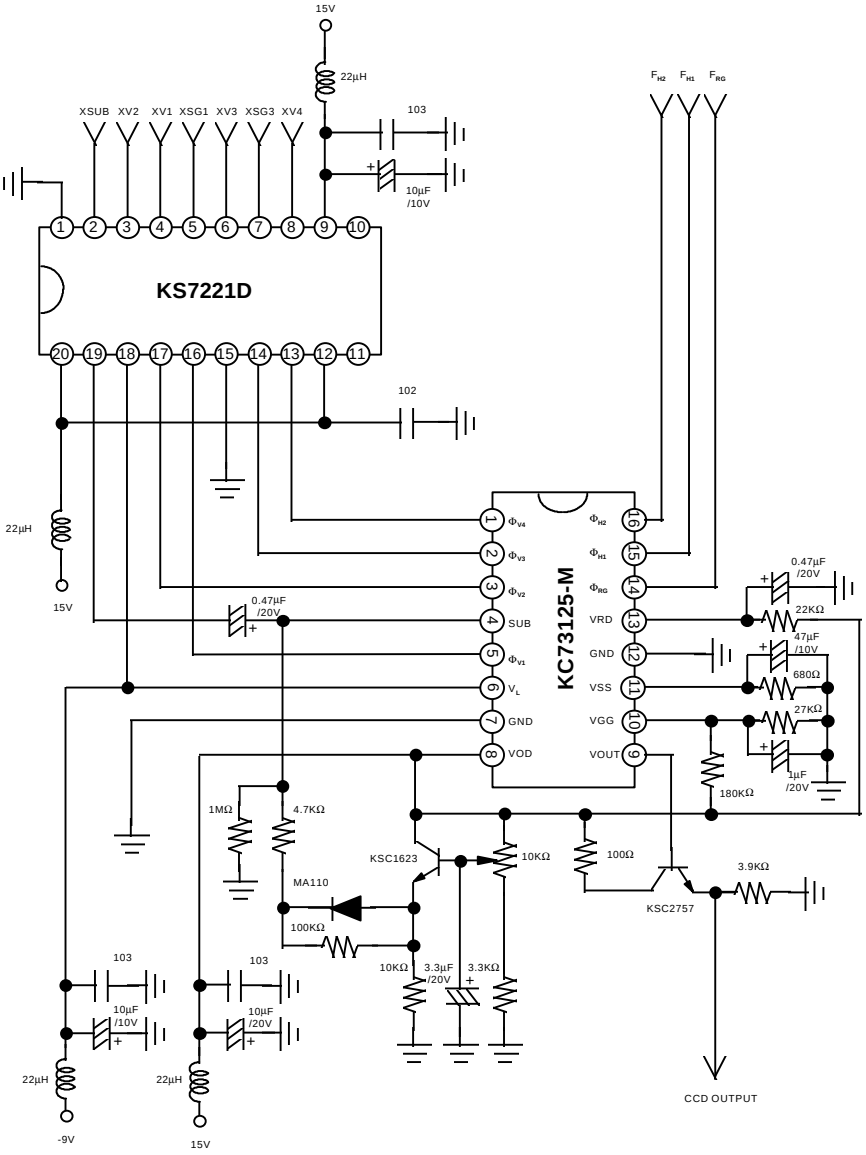
$$U = \frac{Y_{MAX} - Y_{MIN}}{Y_A} \times 100(\%)$$

6. Measure Y signal output average value Y_D [mV] with the horizontal idling time transfer level as reference, when the device ambient temperature is 50°C and all of the light sources are shielded.

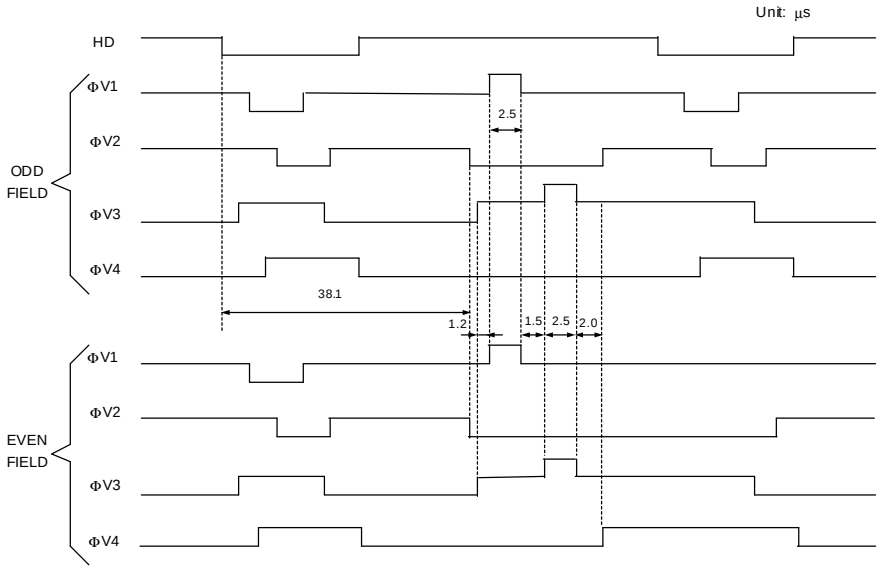
7. Adjust the light intensity to make $Y=Y_A$. Measure the difference value (ΔYF) between the averaged illuminance signal values of the even and odd fields.

$$F_Y = \frac{\Delta Y_F}{Y_A}$$

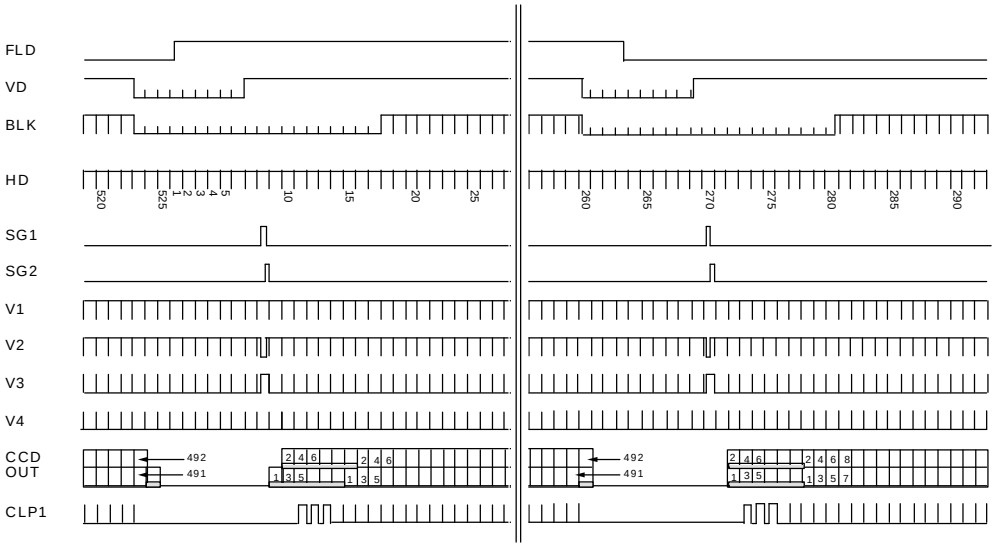
APPLICATION CIRCUITS



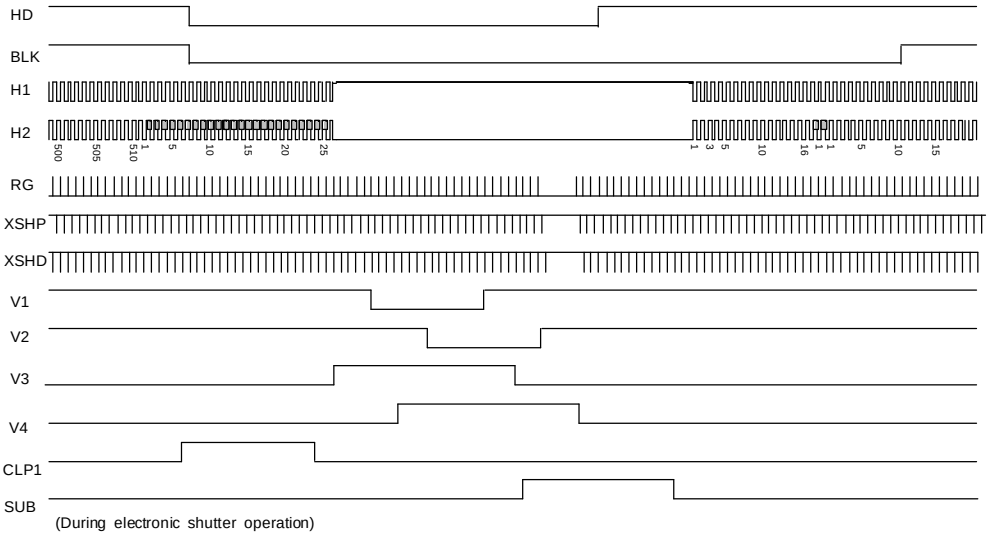
READ-OUT CLOCK TIMING CHART



CLOCK TIMING CHART (VERTICAL SYNC.)

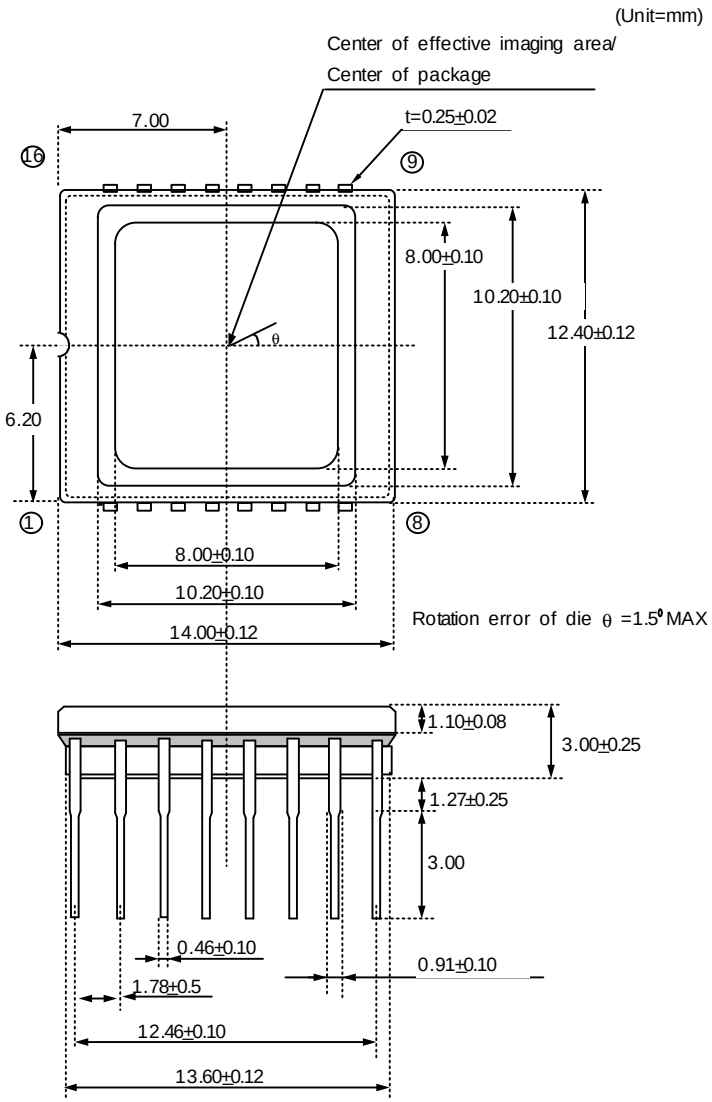


CLOCK TIMING CHART (HORIZONTAL SYNC.)



(During electronic shutter operation)

PACKAGE DIMENSIONS



1. Optical center deviation from mechanical center = ±0.15mm for X and Y direction.
2. Optical surface height from glass lid surface = 1.1 ±0.15mm
3. Optical surface height from package backside bottom = 1.7 ± 0.10mm

HANDLING INSTRUCTIONS

1. Static charge prevention

CCD image sensors can be easily damaged by static discharge. Before handling be sure to take the following protective measures.

1) Use non chargeable gloves, clothes or material. Also use conductive shoes.
2) When handling directly, use an earth band.
3) Install a conductive mat on the floor or working table to prevent generation of static electricity.
4) Ionized air is recommended for discharging when handling CCD image sensor.
5) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2. Soldering

1) Make sure the package temperature does not exceed 80°C
2) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
3) To dismount an imaging device, do not use a solder suction equipment. When using an electronic disoldering tool, use a thermal controler of the zero cross On/Off type and connect to ground

3. Dust and Dirt protection

1) Operate in the clean environments (around class 1000 will be appropriate).
2) Do not either touch glass plates by hand or have object come in contact with glass surface. Should dirt stick to a glass surface blow it off with an air blow (for dirt stuck through static electricity ionized air is recommended).
3) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be carful not to scratch the glass.
4) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room whith great temperature differences.
5) When a protective tape is applied before shipping, just before use remove the tape applied electrostatic protection. Do not reuse the tape.

4. Do not expose to strong light (sun rays) for long period, color filter are discolored

5. Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.