1. PRODUCT OVERVIEW

Overview

The KD16901, Audio Effect Processor, reproduces vivid sound of certain places and dynamic sound of movies. The KD16901 has over 15 sound effect modes including two kinds of Karaoke mode. In addition to the sound modes, the KD16901 provides mic-echo, vocal canceller, loudness function, graphic equalizer, spectrum analyzer interface, tone control and volume/balance control so that it can satisfy various sound requirements of audio systems including TV, stereo audio systems, etc. Furthermore, the KD16901 has built-in 16 bit stereo Σ–Δ ADC and DAC for easy application. The KD16901 also includes two digital source interface blocks and a host interface block supporting normal microcontroller and I^2C bus interfaces.

Key Features

- Over 15 Sound Effect Modes including two kinds of Karaoke mode
- 3/5/7-band Graphic Equalizer and 5/7-band Spectrum Analyzer Interface
- Mic-Echo, Loudness Function and Vocal Canceller
- Digital Volume/Balance/Tone Control
- Programmable Sound Mode
- 33 MIPS 16 bit fixed point DSP Core (SSP1610)
- Built-in Stereo 16 bit Σ–Δ ADC and DAC
- External Clock: 16.9344 MHz
- Sampling Frequency: 44.1 KHz
- Support Various Digital Audio Interface Formats
- Normal Microcontroller Interface and I^2C Bus Interface
- 0.5 Kword Internal Data RAM and 6 Kword Delay Memory for Sound Effect
- 6 Kword Internal Program ROM and 0.5 Kword Parameter ROM for Movie Mode
- 5 V Single Power Supply
- 0.5 μm Triple Metal CMOS Process
- Package: 100 QFP

Ordering Information

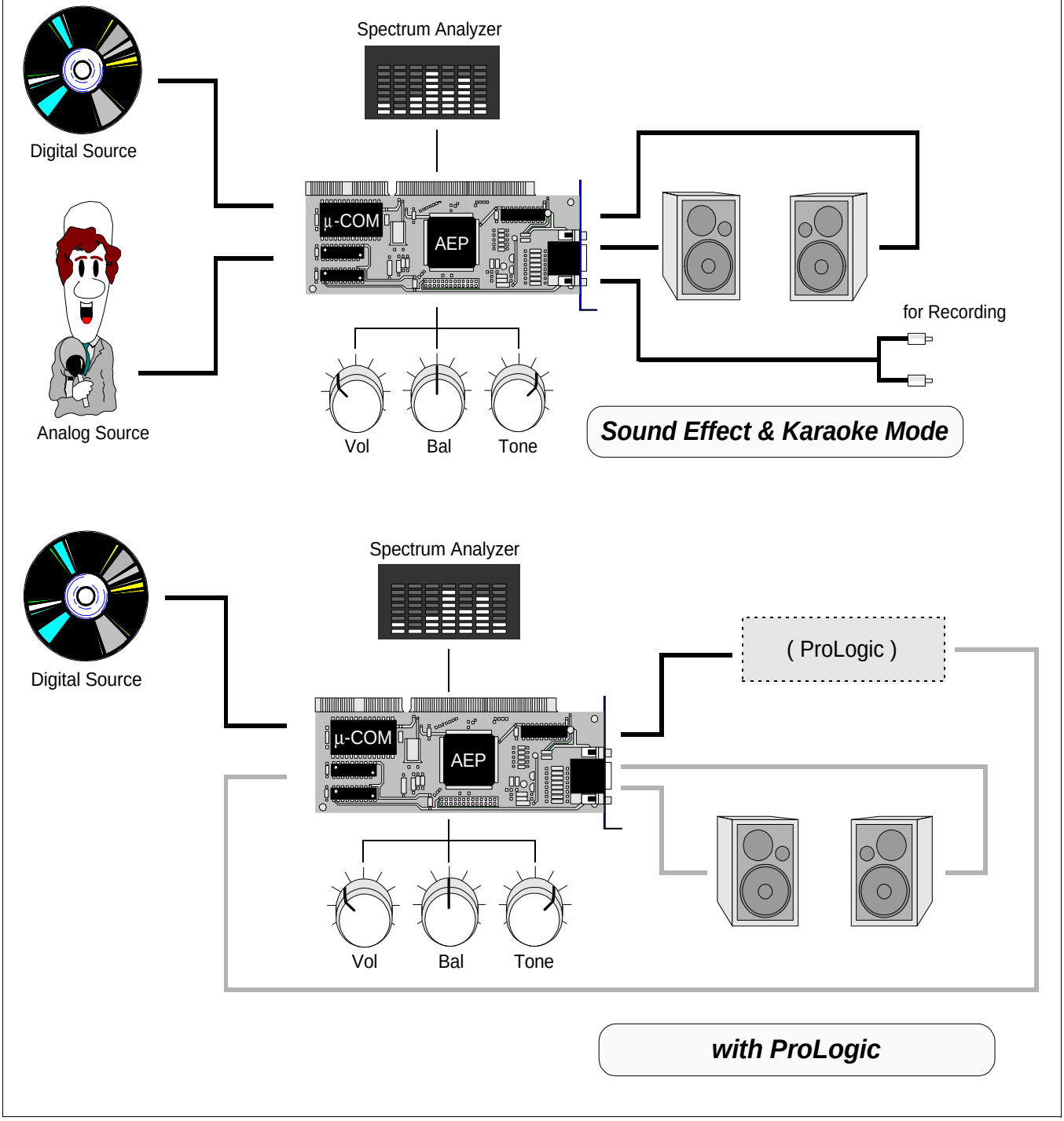
Table 1. Ordering Information

Device	Package	Temperature Range
KD16901 (Audio Effect Processor)	100 QFP	0°C – 70°C

Applications

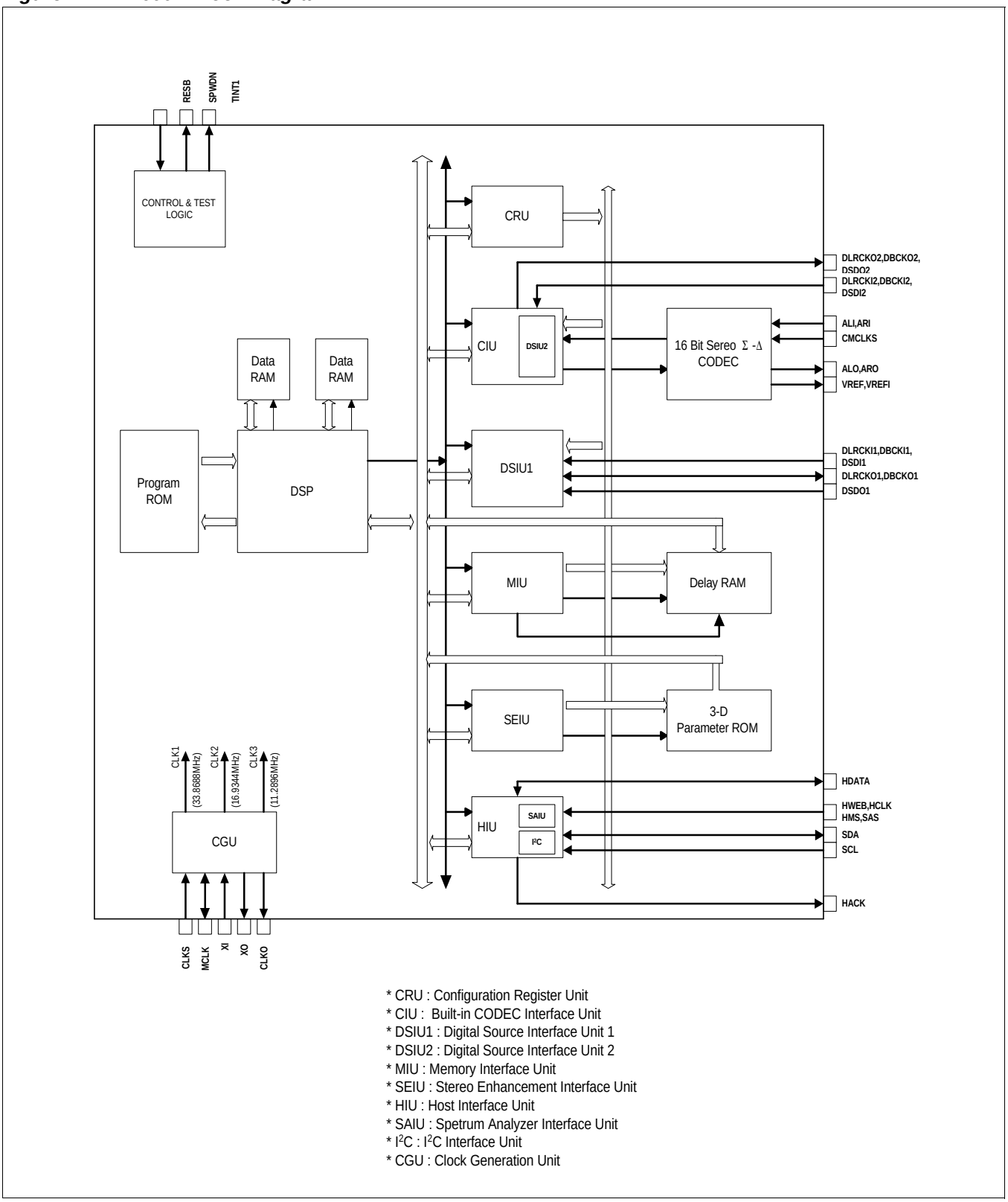
- CD Player
- Video CD
- TV
- Karaoke System
- Car Stereo System
- General Stereo Audio Systems

Typical Application



Block Diagram

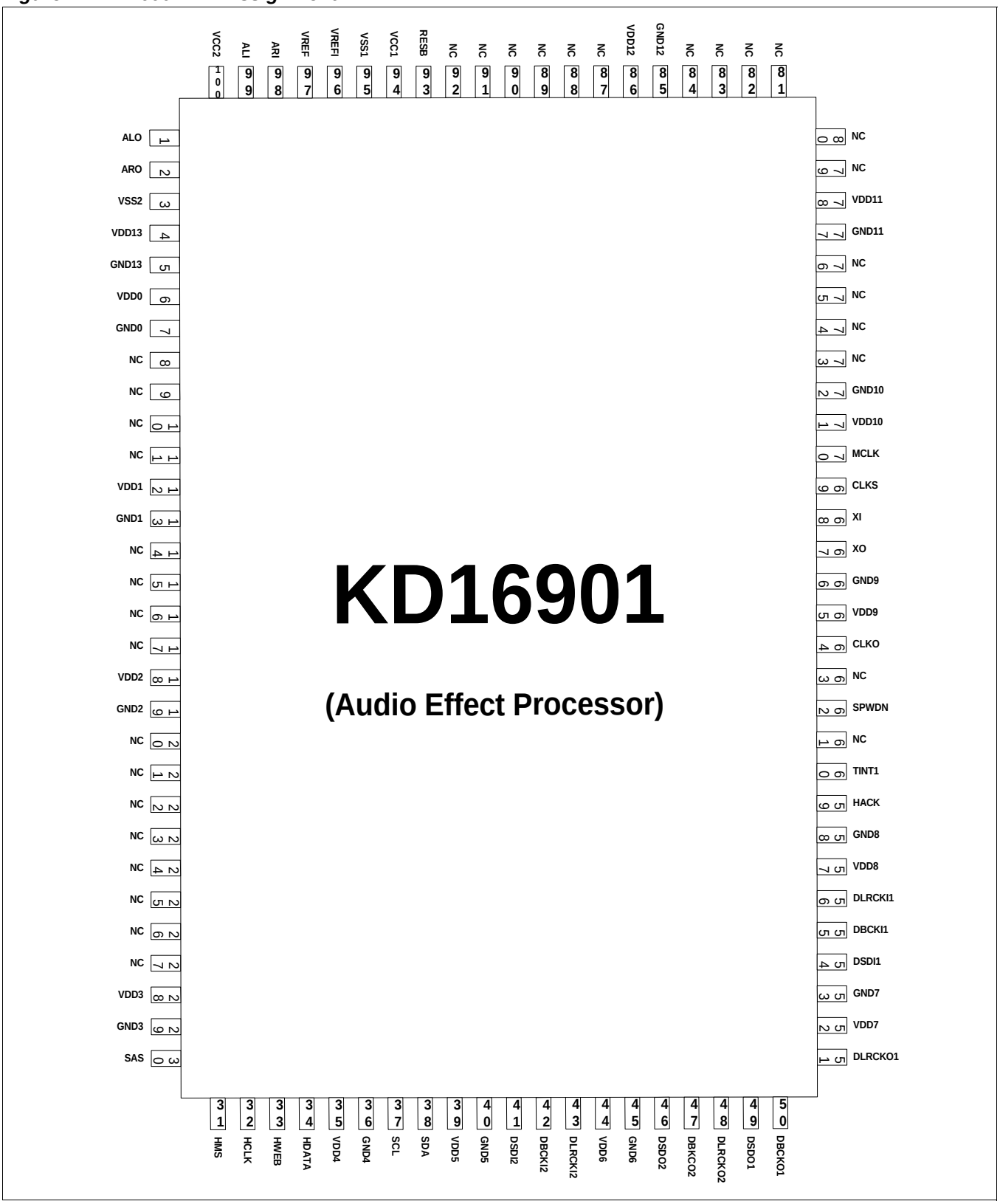
Figure 1. KD16901 Block Diagram



* CRU : Configuration Register Unit
* CIU : Built-in CODEC Interface Unit
* DSIU1 : Digital Source Interface Unit 1
* DSIU2 : Digital Source Interface Unit 2
* MIU : Memory Interface Unit
* SEIU : Stereo Enhancement Interface Unit
* HIU : Host Interface Unit
* SAIU : Spetrum Analyzer Interface Unit
* I^2C : I^2C Interface Unit
* CGU : Clock Generation Unit

Pin Assignment

Figure 2. KD16901 Pin Assignment



Pin Description

Table 2. KD16901 Pin Description

No	Pin Name	I/O	Function	Pad Type	Pull Up/Down
1	ALO	AO	D/A analog output: left channel, 1 Vrms magnitude centered around VREF	-	-
2	ARO	AO	D/A analog output: right channel, 1 Vrms magnitude centered around VREF	-	-
3	VSS2	AG	Codec analog ground	-	-
4	VDD13	DP	Codec digital power +5 V	-	-
5	GND13	DG	Codec digital ground	-	-
6	VDD0	DP	Codec digital power +5 V	-	-
7	GND0	DG	Codec digital ground	-	-
8~11	NC	-	Reserved for chip test	-	-
12	VDD1	DP	Digital power +5 V	-	-
13	GND1	DG	Digital ground	-	-
14~17	NC	-	Reserved for chip test	-	-
18	VDD2	DP	Digital power +5 V	-	-
19	GND2	DG	Digital ground	-	-
20~27	NC	-	Reserved for chip test	-	-
28	VDD3	DP	Digital power +5 V	-	-
29	GND3	DG	Digital ground	-	-
30	SAS	DI	I^2C bus interface slave address selection	-	Down
31	HMS	DI	Host interface mode selection (0: normal, 1: I^2C)	Schmitt trigger	Down
32	HCLK	DI	Normal host interface bit clock (max 400 KHz)	Schmitt trigger	Up
33	HWEB	DI	Normal host interface write enable (HWEB = 0: write, HWEB = 1: read)	Schmitt trigger	Up
34	HDATA	I/O	Normal host interface data In/Out (HWEB = 0: in, HWEB = 1: out)	Schmitt trigger	Down
35	VDD4	DP	Digital power +5 V	-	-
36	GND4	DG	Digital ground	-	-
37	SCL	DI	I^2C bus interface serial bit clock	Open drain	-
38	SDA	I/O	I^2C bus interface serial data in/out	Open drain	-
39	VDD5	DP	Digital power +5 V	-	-
40	GND5	DG	Digital ground	-	-
41	DSDI2	DI	Digital serial data input 2 (DSDI2)	Schmitt trigger	-
42	DBCKI2	DI	DSDI2 bit clock	Schmitt trigger	-
43	DLRCKI2	DI	DSDI2 left/right flag clock	Schmitt trigger	-

Table 2. KD16901 Pin Description

No	Pin Name	I/O	Function	Pad Type	Pull Up/Down
44	VDD6	DP	Digital power +5 V	-	-
45	GND6	DG	Digital ground	-	-
46	DSDO2	DO	Digital serial data output 2 (DSDO2)	-	-
47	DBCKO2	DO	DSDO2 bit clock	-	-
48	DLRCKO2	DO	DSDO2 left/right flag clock	-	-
49	DSDO1	DO	Digital serial data output 1 (DSDO1)	-	-
50	DBCKO1	I/O	DSDO1 bit clock	Schmitt trigger	Down
51	DLRCKO1	I/O	DSDO1 left/right flag clock	Schmitt trigger	Down
52	VDD7	DP	Digital power +5 V	-	-
53	GND7	DG	Digital ground	-	-
54	DSDI1	DI	Digital serial data input 1 (DSDI1)	Schmitt trigger	-
55	DBCKI1	DI	DSDI1 bit clock	Schmitt trigger	-
56	DLRCKI1	DI	DSDI1 left/right flag clock	Schmitt trigger	-
57	VDD8	DP	Digital power +5 V	-	-
58	GND8	DG	Digital ground	-	-
59	HACK	DO	Normal host interface acknowledge	-	-
60	TINT1	DO	Interrupt indicator	-	-
61	NC	-	Reserved for chip test	-	-
62	SPWDN	DO	System power down indicator	-	-
63	NC	-	Reserved for chip test	-	-
64	CLKO	DO	Clock output 33.8688 / 3 = 11.2896 MHz	-	-
65	VDD9	DP	Digital power +5 V	-	-
66	GND9	DG	Digital ground	-	-
67	XO	DO	Crystal oscillator output terminal (16.9344 MHz)	-	-
68	XI	DI	Crystal oscillator input terminal (16.9344 MHz)	-	-
69	CLKS	DI	System clock source selection (0: doubler, 1: external)	-	Down
70	MCLK	I/O	External clock input/doubler clock output according to CLKS	-	Down
71	VDD10	DP	Digital power +5 V	-	-
72	GND10	DG	Digital ground	-	-
73~76	NC	-	Reserved for chip test	-	-
77	GND11	DG	Digital ground	-	-
78	VDD11	DP	Digital power +5 V	-	-
79~84	NC	-	Reserved for chip test	-	-
85	GND12	DG	Digital ground	-	-

Table 2. KD16901 Pin Description

No	Pin Name	I/O	Function	Pad Type	Pull Up/Down
86	VDD12	DP	Digital power +5 V	-	-
87~92	NC	-	Reserved for chip test	-	-
93	RESB	DI	System reset (active low)	-	Up
94	VCC1	AP	Codec analog power +5 V	-	-
95	VSS1	AG	Codec analog ground	-	-
96	VREFI	AO	Codec 2.38 V reference to VSS1 (connect 10.1 μF on this pin)	-	-
97	VREF	AO	Codec 2.62 V reference to VSS1 (connect 0.47 μF on this pin)	-	-
98	ARI	AI	A/D right channel input magnitude centered around VREF should be less than or equal to 1 Vrms	-	-
99	ALI	AI	A/D left channel input magnitude centered around VREF should be less than or equal to 1 Vrms	-	-
100	VCC2	AP	Codec analog power +5 V	-	-

NOTES

- DI Digital Input
- DO Digital Output
- I/O Digital Input and Output
- AI Analog Input
- AO Analog Output
- DP Digital Power
- DG Digital Ground
- AP Analog Power
- AG Analog Ground

2. HARDWARE DESCRIPTION

DSP Core

- Up to 33 MIPS 16 bit fixed point High Performance DSP core (SSP1610)
- 16 x 16 multiplier with 32 bit product
- 32 bit ALU/accumulator
- 0.5 μm triple metal CMOS technology

Memory

- 0.5 Kword data RAM
- 6 Kword delay RAM for sound field effect
- 6 Kword program ROM
- 0.5 Kword parameter ROM for Movie Mode

Built-in A/D and D/A converters

- Stereo 16 bit Σ–Δ A/D converter
- Stereo 16 bit Σ–Δ D/A converter

Peripheral Interface Register Configuration

- EXT0: Hardware configuration register (extended to five registers using EXT0 [15:13])
- EXT1: Codec and DSIU2 interface register
- EXT2: DSIU1 interface register
- EXT3: Delay memory address register
- EXT4: Delay memory data read/write register
- EXT5: Parameter ROM used in Movie Mode interface register
- EXT6: Host interface register

Table 3. Extended Hardware Configuration Registers

EXT0 [15:13]	Register Name	Description
000	DSIU1ICR	Input format control of digital source interface unit 1
001	DSIU1OCR	Output format control of digital source interface unit 1
010	DSIU2ICR	Input format control of digital source interface unit 2
011	DSIU2OCR	Output format control of digital source interface unit 2/ Codec format control
100–110	Reserved	
111	CHIPCR	Chip Control: Interrupt control, DSDO1 clock source selection, Input Source Configuration Selection

Table 4. EXT0 setting for DSIU1ICR

[15:13]	[12:8]	[7:0]	Value	Description	Related Pin
000	Reserved	[7]	0	DLRCKI1 is low for L-ch	DLRCKI1 (LR Clock)
			1	DLRCKI1 is high for L-ch	
		[6]	0	DSDI1 is synchronized with falling edge of DBCKI1	DBCKI1 (Bit Clock)
			1	DSDI1 is synchronized with rising edge of DBCKI1	
		[5:4]	00	32 Fs	DSDI1 Serial Data Fs
			01	48 Fs	
			10	64 Fs	
			11	Reserved	
		[3:2]	00	16 bit	DSDI1 Data Length
			01	18 bit	
			10	20 bit	
			11	24 bit	
		[1:0]	00	I^2S	DSDI1 Data Position
			01	Reserved	
			10	Right Justified	
			11	Left Justified	

Table 5. EXT0 setting for DSIU1OCR

[15:13]	[12:8]	[7:0]	Value	Description	Related Pin
001	Reserved	[7]	0	DLRCKO1 is low for L-ch	DLRCKO1 (LR Clock)
			1	DLRCKO1 is high for L-ch	
		[6]	0	DSDO1 is synchronized with falling edge of DBCKO1	DBCKO1 (Bit Clock)
			1	DSDO1 is synchronized with rising edge of DBCKO1	
		[5:4]	00	32 Fs	DSDO1 Serial Data Fs
			01	48 Fs	
			10	64 Fs	
			11	Reserved	
		[3:2]	00	16 bit	DSDO1 Data Length
			01	18 bit	
			10	20 bit	
			11	24 bit	
		[1:0]	00	I^2S	DSDO1 Data Position
			01	Reserved	
			10	Right Justified	
			11	Left Justified	

Table 6. EXT0 setting for DSIU2ICR

[15:13]	[12:8]	[7:0]	Value	Description	Related Pin
010	Reserved	[7]	0	DLRCKI2 is low for L-ch	DLRCKI2 (LR Clock)
			1	DLRCKI2 is high for L-ch	
		[6]	0	DSDI2 is synchronized with falling edge of DBCKI2	DBCKI2 (Bit Clock)
			1	DSDI2 is synchronized with rising edge of DBCKI2	
		[5:4]	00	32 Fs	DSDI2 Serial Data Fs
			01	48 Fs	
			10	64 Fs	
			11	Reserved	
		[3:2]	00	16 bit	DSDI2 Data Length
			01	18 bit	
			10	20 bit	
			11	24 bit	
		[1:0]	00	I^2S	DSDI2 Data Position
			01	Reserved	
			10	Right Justified	
			11	Left Justified	

Table 7. EXT0 setting for DSIU2OCR[i] and Codec Format

[15:13]	[12:8]	[7:0]	Value	Description	Related Pin
011	Reserved	[7:3]	00000	Reserved	Reserved
		[2]	0	DLRCKO2 is low for L-ch	DLRCKO2 (LR Clock)
			1	DLRCKO2 is high for L-ch	
		[1]	0	DSDO2 is synchronized with falling edge of DBCKO2	DBCKO2 (Bit Clock)
			1	DSDO2 is synchronized with rising edge of DBCKO2	
		[0]	0	I^2S	Codec In/Out, DSDO2 Data Position
			1	Right Justified	

i. DSDO2 supports only 32 Fs and 16 bit format

Table 8. EXT0 setting for CHIPCR

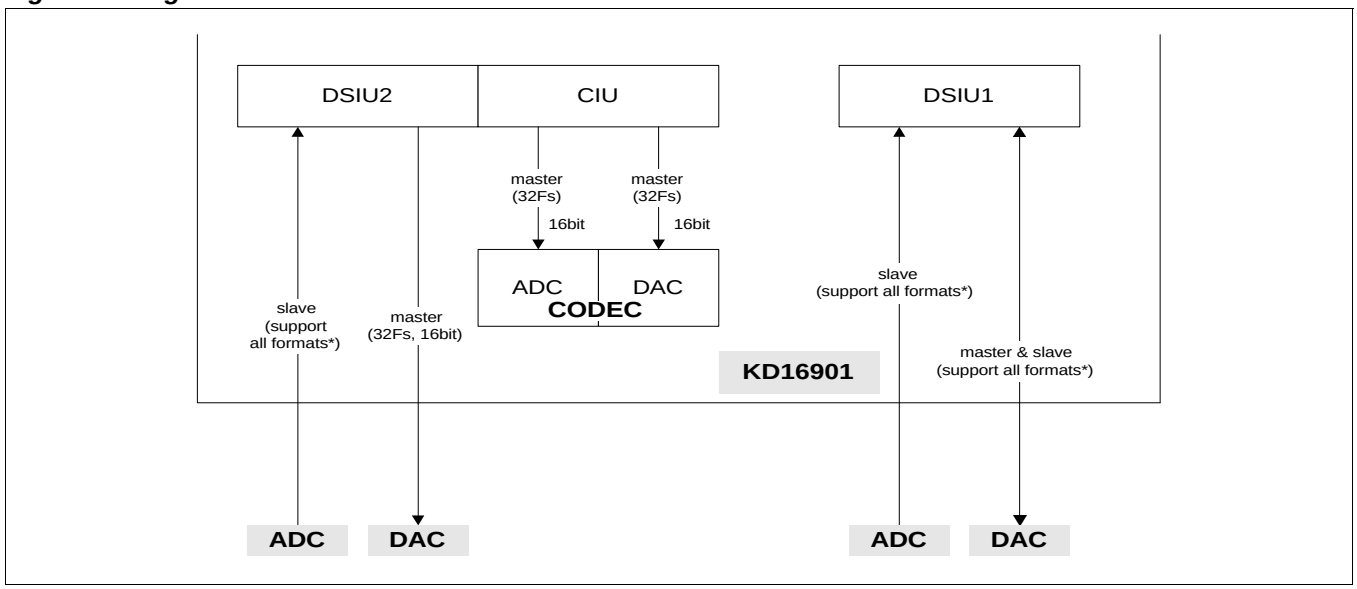
[15:13]	[12:8]	[7:0]	Value	Status	Description
111	Reserved	[7]	Always '1'		Reserved
		[6]	Always '1'		Reserved
		[5]	0	External	DLRCKO1/DBCKO1 Clock Source
			1	Internal	
		[4:3]		Reserved	Reserved
		[2:0]	000	ADC enable	Input Source Configurations
			001	DSIU1 enable	
			010	DSIU2 enable	
			011	ADC & DSIU1 enable	
			100	DSIU1 & DSIU2 enable	
			101–111	Reserved	

General Description of Digital Audio Interface of the KD16901

The digital audio interface of the KD16901 consists of 3 blocks mainly: CIU, DSIU1 and DSIU2. The CIU block is the interface block for the built-in codec. The DSIU1 and DSIU2 blocks are for external ADC and DAC interfaces. The DSIU2 and CIU are mutually exclusive in a sense that only one of the two is working. The interface blocks can work either slave or master mode (for DSIU1 output, both modes) depending on whether the KD16901 supplies the bit clocks and the LR clocks (master), or DAC (ADC) provides the clocks (slave). For example, the DSIU1 takes the digital audio outputs in master/32 Fs mode, which means that the KD16901 (or DSIU1) provides the bit and the LR clocks to the DAC and the audio data format 32 Fs (32 bit clocks in a LR clock period).

When an external ADC or (and) DAC is used, it is strongly recommended to use the clock, CLKO (pin #64), provided by KD16901 as the master clock for clock synchronization.

Figure 3. Digital Audio Interface Formats of the KD16901



NOTE "support all formats" means all formats of the data length and the sampling rate listed in Table 4 through Table 6

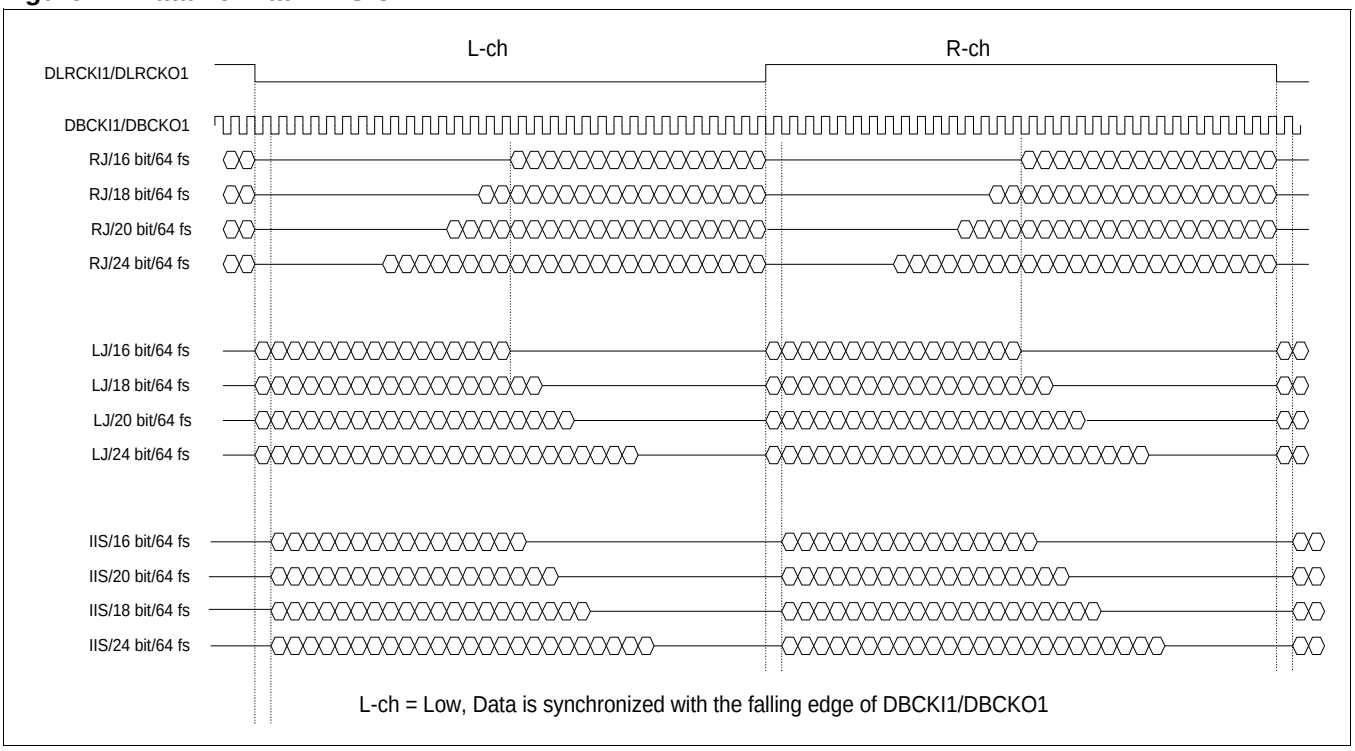
Codec Interface

The KD16901 has on-chip16 bit stereo ADC and DAC with digital filters and serial interfaces to provide CD quality sound for audio application. The digital A/D decimation filter takes in the encoded signals from Σ–Δ A/D modulator, and outputs 16 bit stereo digital audio data through the serial interface. The D/A interpolation filter takes 16 bit stereo audio data from the serial interface, and outputs one bit signal to the Σ–Δ D/A. The oversampling rate of the digital filter is 128xFs, where Fs can be varied from 4 KHz to 48 KHz and can be changed on the fly. The serial data interface is running at 32xFs and supports both right justified format and I^2S data format. To set input and output formats of codec, see Table 7.

Digital Source Interface Unit 1 (DSIU1)

The DSIU1 has a digital serial data input source (DSDI1) and a digital serial data output source (DSDO1). It supports 16/18/20/24 bit data length, and supports right justified, left justified or I^2S format in data position. The format of DSIU1 is controlled by a microcontroller through Host Interface Unit (HIU) and Configuration Register Unit (CRU) as in Table 4 and Table 5. In formats of DSDI1 and DSDO1, only 16 bit data length is supported when the data rate is 32xFs. The DSDO1 can operate either in slave or master mode while DSDI1 operates only in slave mode by Configuration Register Unit (CRU) setting. Note that the MSB is transferred first.

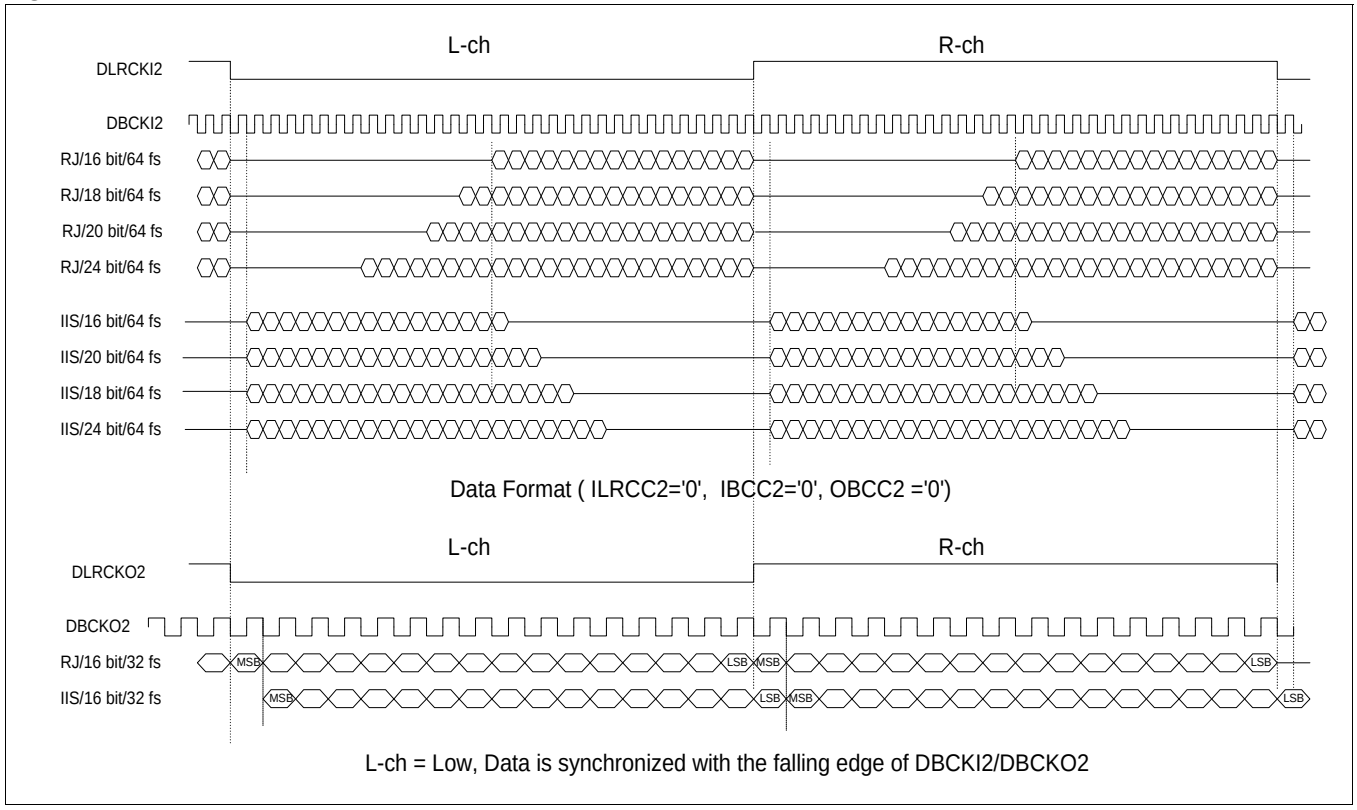
Figure 4. Data Format in DSIU1



Digital Source Interface Unit 2 (DSIU2)

The DSIU2 has a digital serial data input source (DSDI2) and a digital serial data output source (DSDO2). The DSDI2 operates in slave mode, while the DSDO2 operates in master mode. The format of DSDI2 is same as that of DSDI1. The format of DSDO2 is same as that of built-in codec. The format of DSDO2 supports 16 bit and 32xFs right-justified or IIS format. The format of DSIU2 is controlled by a microcontroller through Host Interface Unit (HIU) and Configuration Register Unit (CRU) as in Table 6 and Table 7. Note that the MSB is transferred first.

Figure 5. Data Format in DSIU2



Host Interface Unit (HIU)

The KD16901 receives commands and parameters in serial format from microcontroller through built-in HIU. The data must be in byte unit (8 bit). The host commands are composed of the following three types.

- Command Only
- Command followed by Parameter
- Command followed by Parameter #1 (high byte) followed by Parameter #2 (low byte)

The details on commands used in the KD16901 can be found in Chapter 4.

The HIU supports either normal microcontroller interface or I^2C bus interface. In normal host interface, the related pins are HCLK (Normal Host Interface Bit Clock), HWEB (Normal Host Interface Write Enable) and HDATA (Normal Host Interface Data In/Out). In I^2C bus interface, the related pins are SDA (Serial Data Line), SCL (Serial Clock Line) and SAS (I^2C Bus Interface Programmable Slave Address Selection). One can refer to I^2C Bus Specification by Philips. The I^2C bus interface in the KD16901 operates in Slave-Transmitter mode. The other function of HIU is the spectrum request function. The spectrum value is sent to microcontroller. The maximum bit clock (HCLK or SCL) is 400 KHz.

Figure 6. Data Format in Normal Host Interface

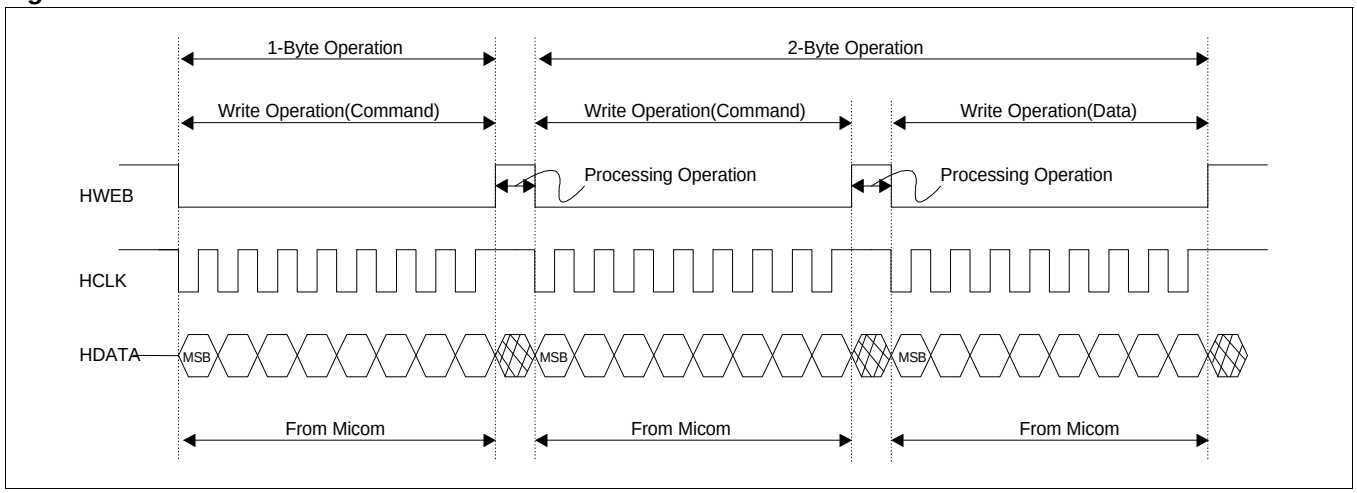
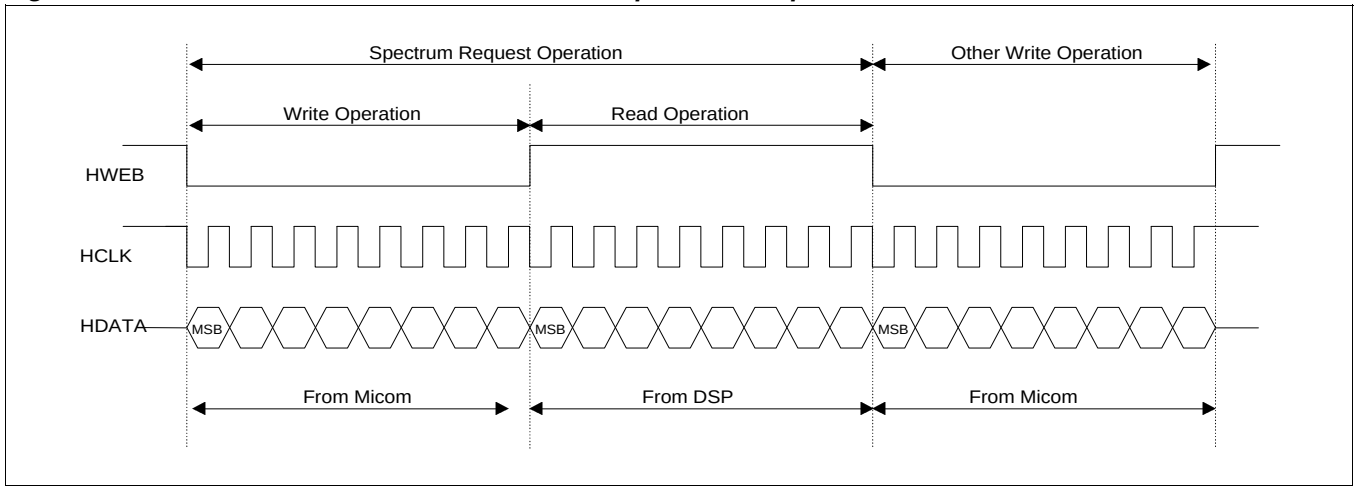


Figure 7. Data Format in Normal Host Interface-Spectrum Request



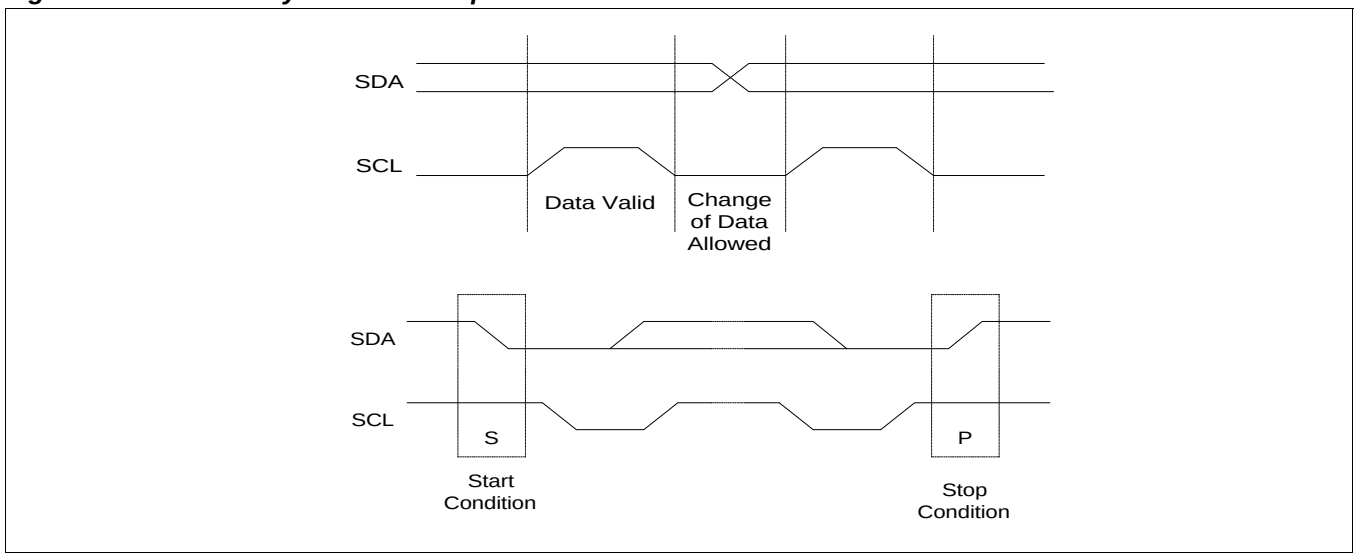
I²C Bus Interface

The KD16901 can be controlled by a microcontroller via the 2-line I²C bus, SDA (Serial Data Line) and SCL (Serial Clock Line). Both lines must be connected to a positive supply via pull-up resistor. Data transfer may be initiated only when the bus is not busy. When the bus is free, both lines are high. The data on the SDA line must be stable during the high period of clock, SCL. When the SCL is low, the SDA can change. Every byte transferred through the SDA line must contain 8 bits including programmable slave address and read/write direction control bit. Each byte must be followed by acknowledge bit which is sent back to the microcontroller by the KD16901 by pulling down the SDA line. The MSB is transferred first. The setup and hold time on the SCL and SDA lines can be found in I²C Specification by Philips.

- **I²C bus interface start and stop condition**

The start condition is high to low transition of the SDA line while the SCL is high. The stop condition is low to high transition of the SDA line while SCL is high.

Figure 8. Data Validity and Start/Stop Condition in I²C Bus



- **I²C Bus Interface Acknowledge**

The acknowledge related clock pulse is generated by a microcontroller. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse. The slave-transmitter generates negative acknowledge when read operation processes. The negative acknowledge is generated by a master (microcontroller).

- **I²C Bus Interface Slave Address Selection**

Table 9. I²C Bus Interface Slave Address Selection

Pin Name	Status	Selected Slave Address (Hex)	
		Write Address	Read Address
SAS	Low	80	81
	High	82	83

- **I²C Bus Interface Specification**

Figure 9. I²C Bus Interface Format-Write Operation (SAS = 0)

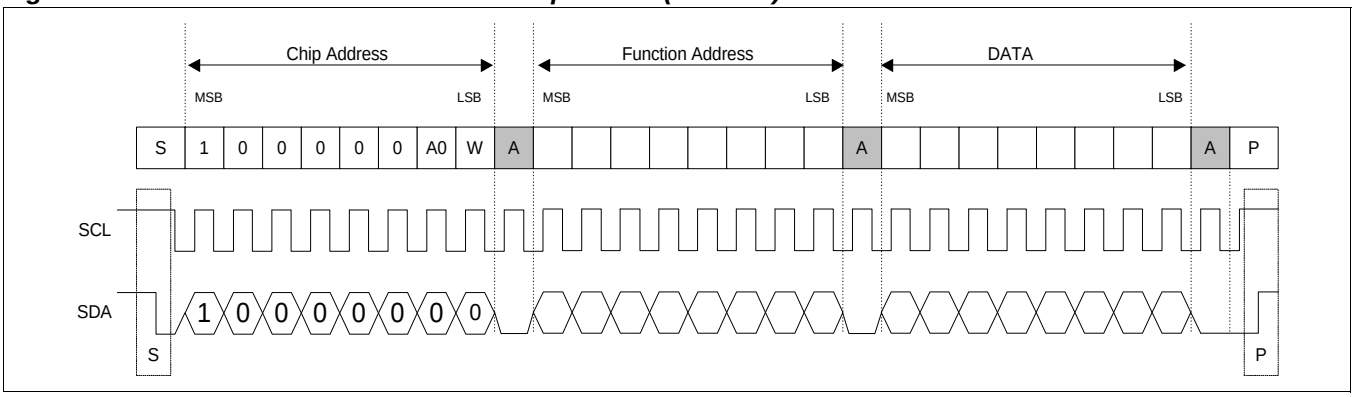
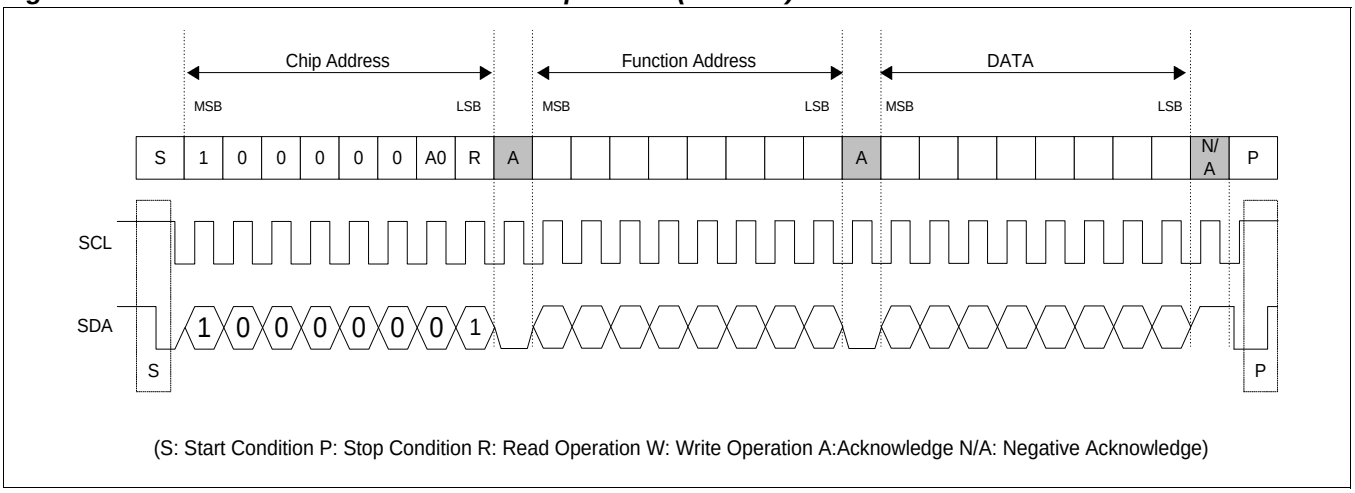


Figure 10. I²C Bus Interface Format-Read Operation (SAS = 0)



(S: Start Condition P: Stop Condition R: Read Operation W: Write Operation A:Acknowledge N/A: Negative Acknowledge)

System Clock

In the KD16901, there are two ways to supply the system clock,

- **Using X-tal Oscillator**

In this case, the clock doubler in the KD16901 is used. The CLKS should be set to LOW and X-tal oscillator of 16.9344 MHz is connected to XI and XO pins. Then, the clock doubler doubles 16.9344 MHz to 33.8688 MHz and outputs to MCLK.

- **Using External Clock Source**

The CLKS should be set to HIGH. In this case, the MCLK pin is the input which is the system clock of 33.8688 MHz.

Reset

The KD16901 provides hardware reset and software reset. In hardware reset using RESB pin, the reset signal has to be kept for L/R one cycle pulse width (approx. 22.67 μs) for stable initialization of built-in codec. In the software reset (command code: 0x00) through HIU, system initialization is internally processed.

Power Down

The system power down mode set by host command through HIU disables all hardware macro blocks in the KD16901, i.e., DSP, delay RAM, data RAM, program ROM, glue logic and codec. Every host command can wake-up the system power down mode.

3. FUNCTIONAL DESCRIPTION

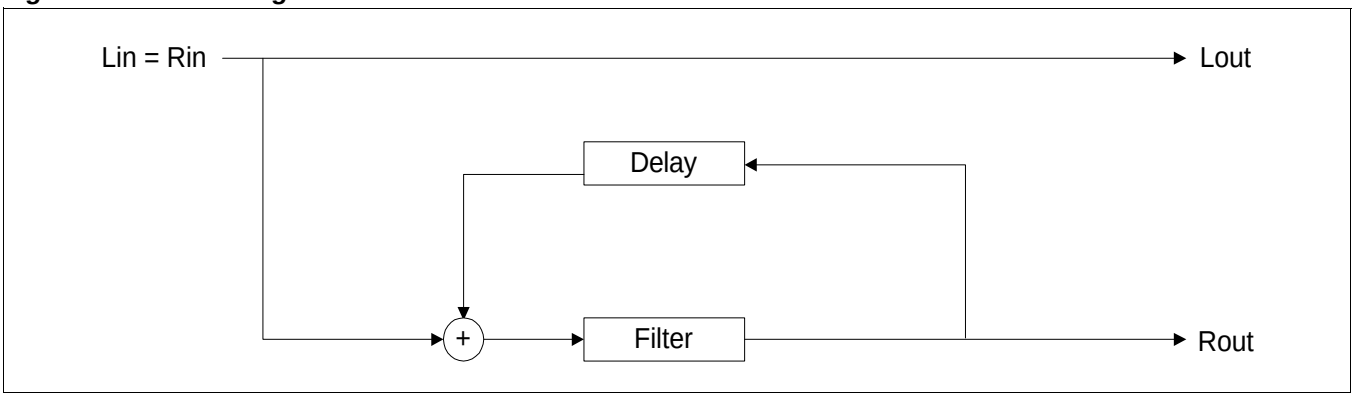
Bypass Mode

In bypass mode, the input is bypassed to the output with the control of volume, balance and tone.

Stereo Emulation Mode I, II

These modes emulate mono input signal to stereo signal. The block diagram realizing these modes is shown in Figure 11. The Stereo Emulation Mode I and II are different in the strength of effect. The Stereo Emulation Mode II produces more stereo effect than Stereo Emulation Mode I.

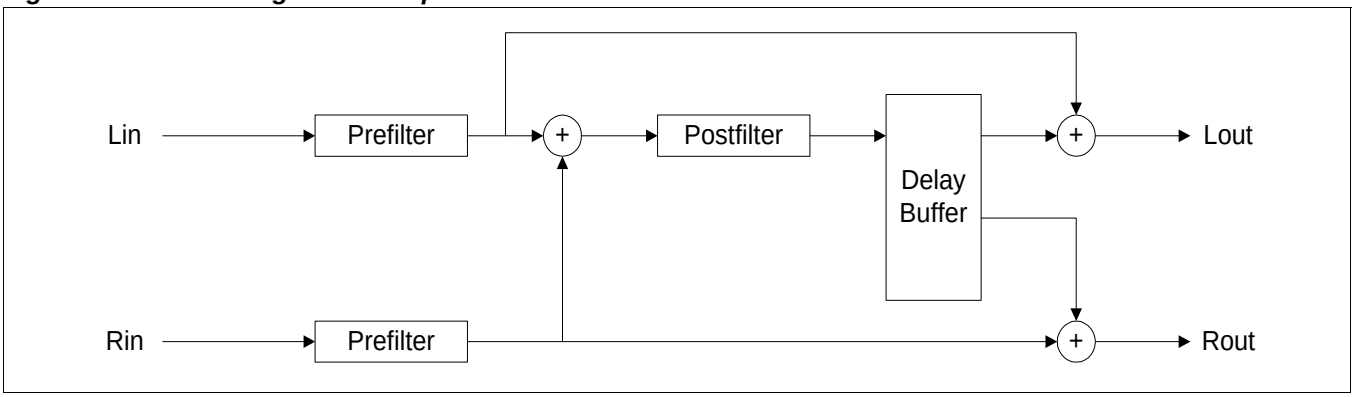
Figure 11. Block Diagram for Stereo Emulation Modes



Super Woofer Mode I, II, III

Super Woofer modes highly emphasize very low frequency component of input signal, and then, add echo effect. The block diagram realizing these modes is shown in Figure 12. The Super Woofer Mode I, II and III are different in the strength of the effect. The effect becomes stronger from Super Woofer I to Super Woofer III.

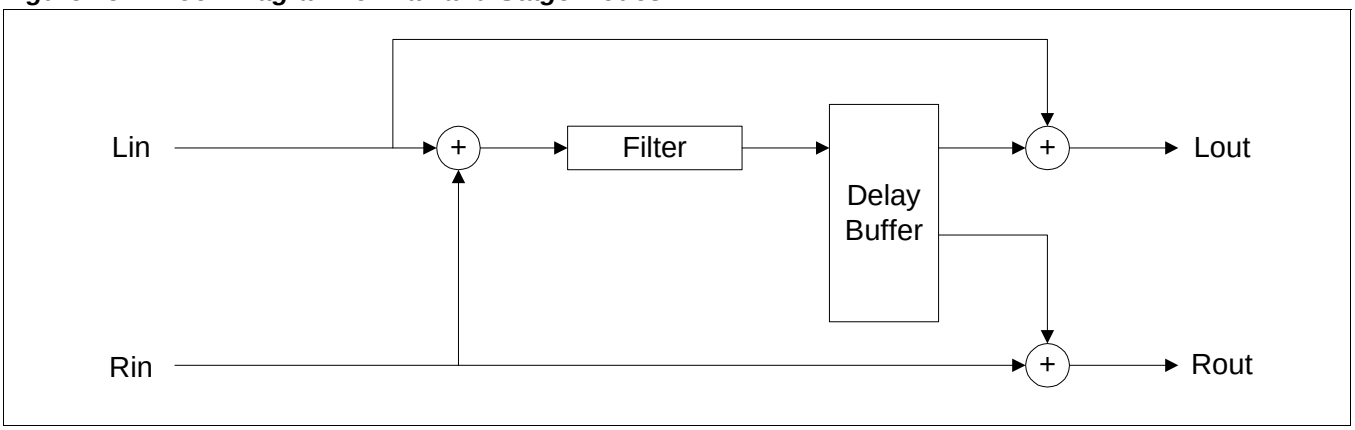
Figure 12. Block Diagram for Super Woofer Modes



Hall Mode I, II and Stage Mode

Hall modes and stage mode produce effects that one feels as if he or she is in a hall or a stage respectively. The block diagram realizing these modes is shown in Figure 13. The Hall Mode I and II are different in the hall size which one can feel. The Hall Mode II produces the effect of a larger hall than that of Hall Mode I.

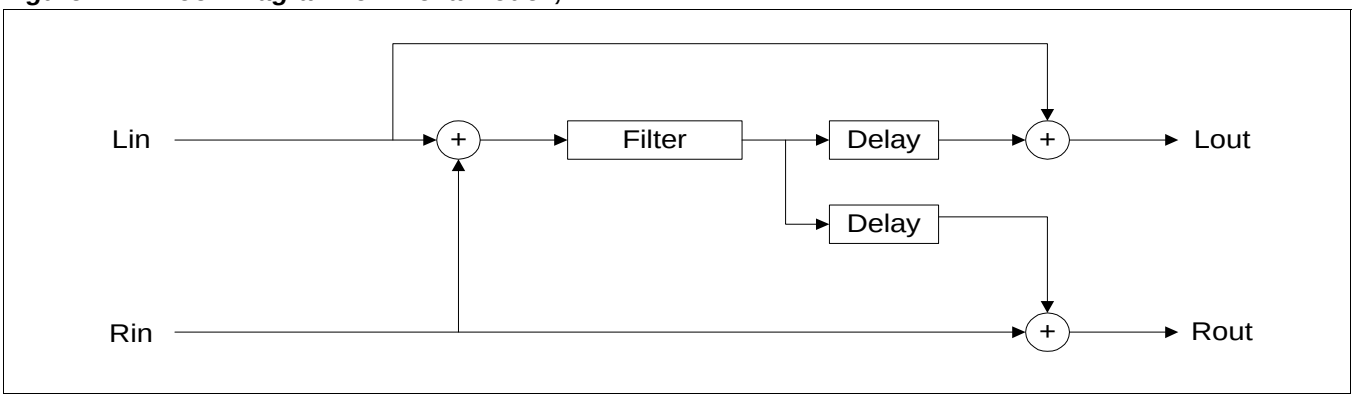
Figure 13. Block Diagram for Hall and Stage Modes



Arena Mode I, II

Arena modes produce effects that one feels as if he or she is in an arena. The block diagram realizing these modes is shown in Figure 14. The Arena Mode I and II are different in the arena size which one can feel. The Arena Mode I produces the effect of wider arena than that of Arena Mode II.

Figure 14. Block Diagram for Arena Mode I, II



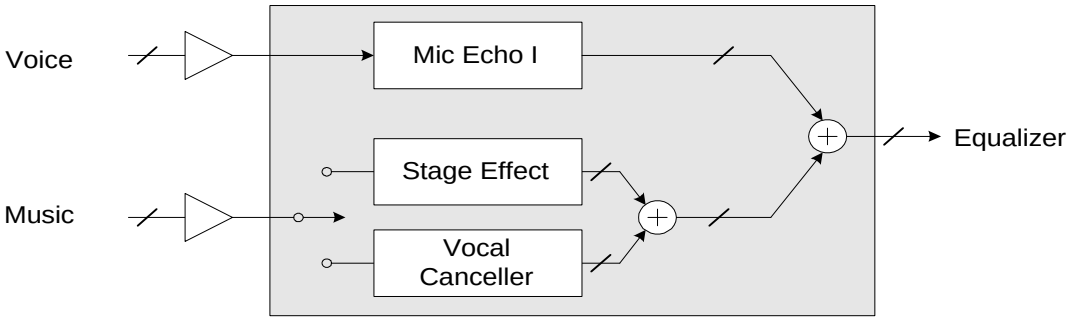
News/Drama Mode

This mode enhances high frequency component of signal to improve the speech recognizability for news or drama program.

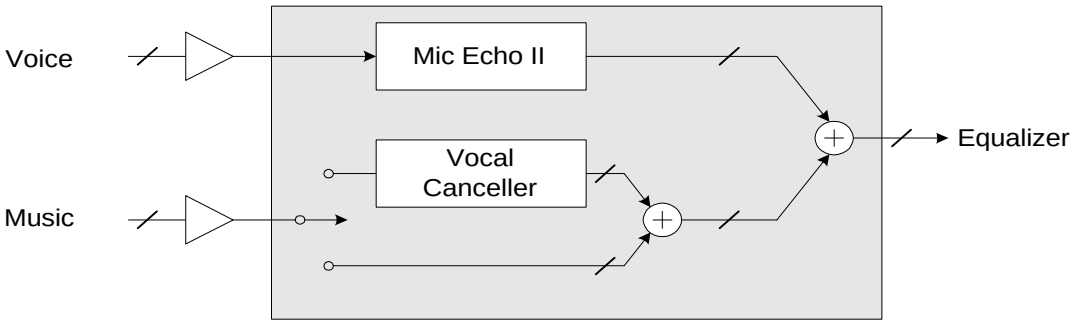
Karaoke Mode I, II

The Karaoke modes receive inputs from both a microphone and an audio source. In Karaoke Mode I, the microphone input is echoed by the echo filter 1 and the audio source input is effected with the stage mode. When the vocal canceller is selected, the audio source whose vocal component is cancelled is bypassed without stage effect. In Karaoke Mode II, the microphone input is echoed by the echo filter 2 and the audio source input is bypassed.

Figure 15. Karaoke Mode I, II



Karaoke Mode I



Karaoke Mode II

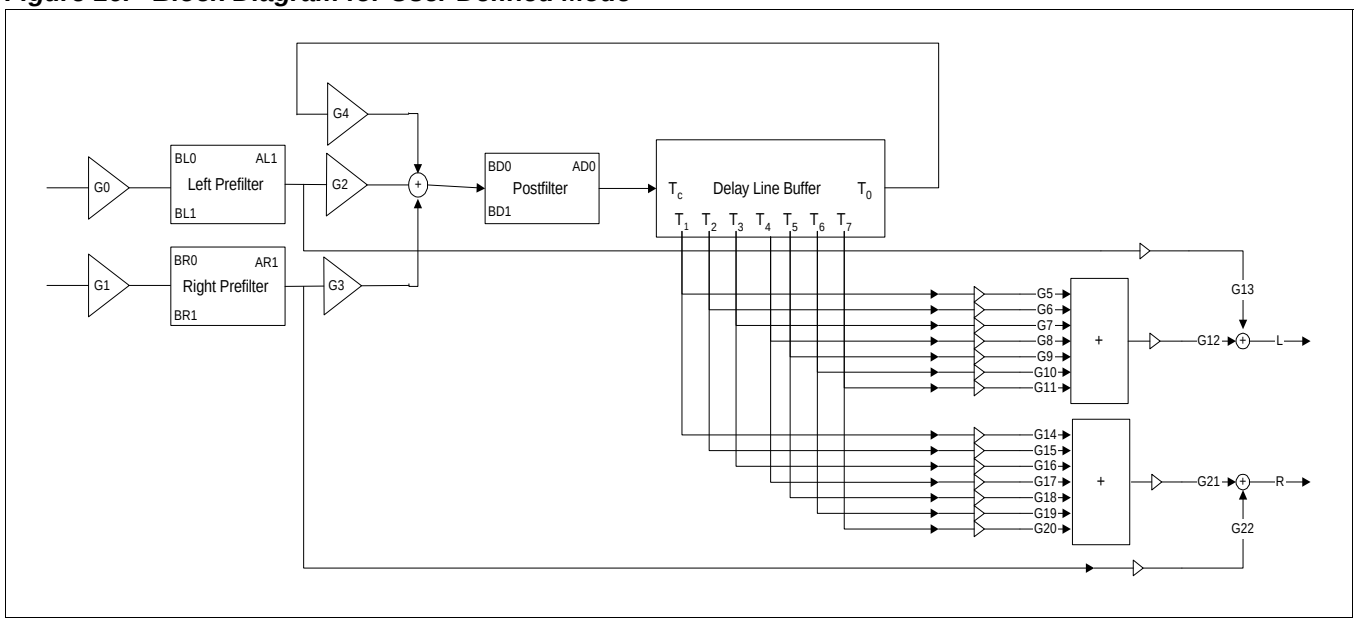
In Mic echo filter 1, the delay gains remain large and they are shortly decayed as time goes by. Thus, one can feel plenty of echo while there is little aliasing between echos and original sound. The Mic echo filter 2 has a similar structure to that of Hall mode. The effect is not stronger than that of Mic echo filter 1, but it produces a widely spread echo which is very impressive.

User Defined Mode

The User Defined Mode enables one to design a new sound effect mode by setting the parameters of existing filter structure. The block diagram of this filter structure is shown in Figure 16. One can set these parameters by sending host commands corresponding to each parameters. The commands used for this mode are listed in Chapter 4. The command codes from 0x49 to 0x71 are assigned to User Defined Mode. The usage of individual parameter in Figure 16 is as follows:

- The gain parameters, G0 and G1, are used to control left and right input gains respectively.
- The parameters, BL0, BL1 and AL1, are coefficients of the IIR filter used for left prefilter. The parameters, BR0, BR1 and AR1, are coefficients of the IIR filter used for right prefilter. The parameters, BD0, BD1 and AD1 are coefficients of the IIR filter used for postfilter. The structures of all three filters are realized by the first order IIR. The zero of the transfer function of each filter is – BX1 / BX0 and the pole is – AX1, where X is L or R or D.
- The parameters, G2, G3 and G4, are left term gain, right term gain and feed-back term gain respectively.
- The parameters, G5 to G11, are gains of delayed signals in the left channel. The parameters, G14 to G20, are gains of delayed signals in the right channel. The parameters, G12 and G21, are gains of effected output signals. The parameters, G13 and G22, are gains of directed output signals.
- The parameter, T0, is the pointer address of the feed-back signal in the delay memory. The parameter, Tc, is the pointer address of the current input signal. The parameters, T1 to T7, are pointers designating addresses of the 7 different delayed signals. Note that the pointer address is same as the amount of delay. Thus, T0 to T7 values can be simply determined as the amount of delay which one wants to set.

Figure 16. Block Diagram for User Defined Mode



Movie Mode I, II

The Movie Mode I and II create 3-dimensional sound images from 2-channel stereo input signals. The Movie Mode-I enhances stereo images dynamically using the Samsung proprietary TLA (Table Lookup Algorithm) method. One perceives as if he or she is in the live stage. The Movie Mode II uses a sound source relocalization technique based on Head Related Transfer Function (HRTF). Only using two front speakers, one can perceive as sound coming from various directions.

Graphic Equalizer

The KD16901 provides the graphic equalizer having following features.

- 3/5/7-band graphic equalizer
- 5/7-band spectrum analyzer display
- ± 12 dB adjustable range

The 3-band graphic equalizer can be used as a simple digital tone control (as bass and treble control).

Table 10. Center Frequencies of Equalizer Bands (Hz)

Band	3-Band Mode	5-Band Mode	7-Band Mode
Band0	63	100	63
Band1	1 K	300	160
Band2	16 K	1 K	400
Band3	-	3 K	1 K
Band4	-	10 K	2.5 K
Band5	-	-	6.4 K
Band6	-	-	16 K

The gain control of each band uses an attenuation table containing attenuation values, which has the size of 25 to implement ±12 dB with 1 dB step control

Figure 17. Dynamic Range of Each Control Band

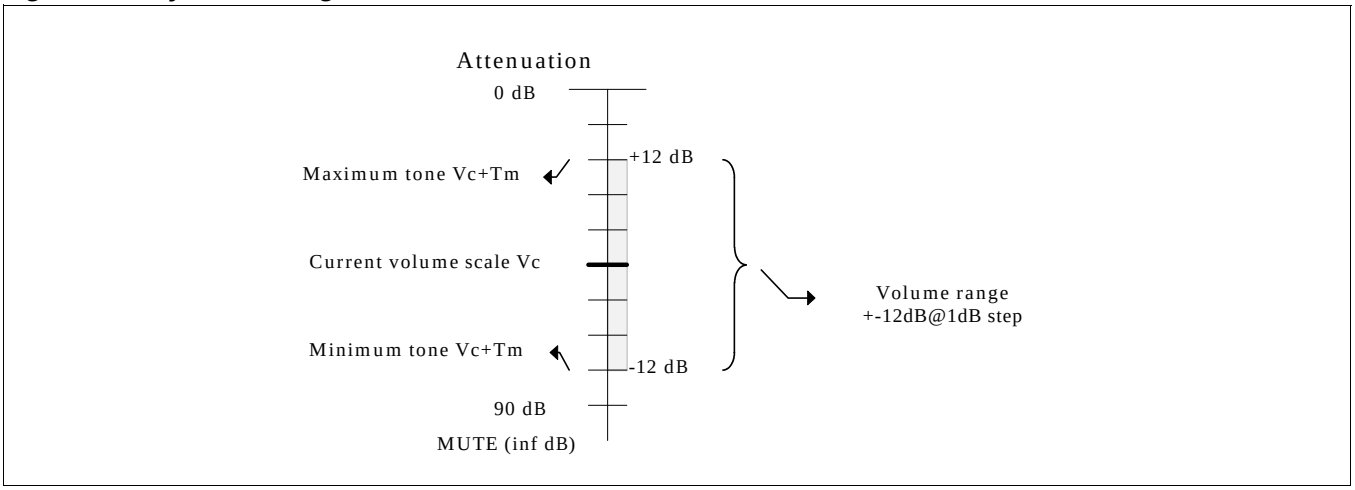


Table 11. Gain Table for Tone Level Control

Index	Gain Value (Hex)	Gain Scale (dB)	Index	Gain Value (Hex)	Gain Scale (dB)
0	0809	– 12	13	23e7	1
1	0904	– 11	14	2849	2
2	0a1e	– 10	15	2d33	3
3	0b5a	– 9	16	32b7	4
4	0cbd	– 8	17	38e7	5
5	0e4b	– 7	18	3fd9	6
6	1009	– 6	19	47a3	7
7	11fe	– 5	20	5061	8
8	1430	– 4	21	5a30	9
9	16a7	– 3	22	6531	10
10	196b	– 2	23	718a	11
11	1c85	– 1	24	7f64	12
12	2000	0			

Spectrum Analyzer

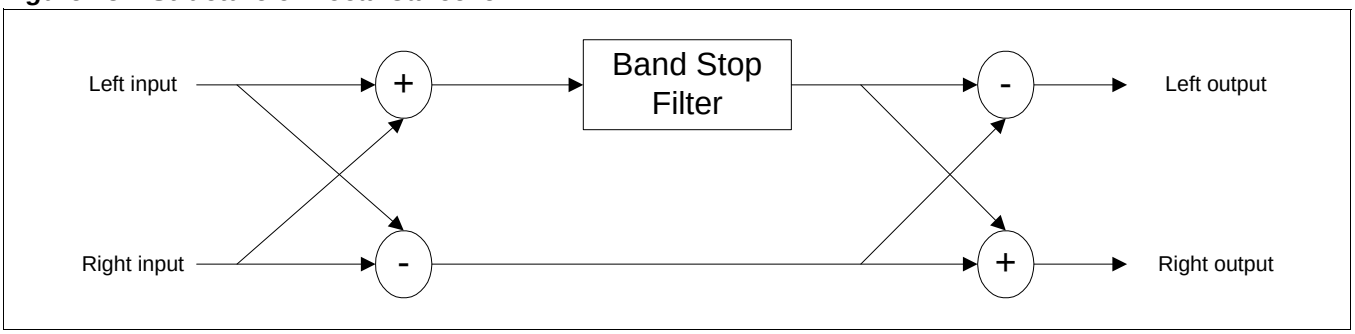
The spectrum analyzer displays the power of each equalizer band output. The band number in spectrum analyzer is identical to that in graphic equalizer except for the 3-band equalizer mode.

In this case, the spectrum analyzer follows 7-band equalizer mode in spite of the 3-band equalizer mode being selected. The 16 bit analyzer outputs are transformed to generate a byte value (256 levels), which can be applied to an external LCD or other display devices. At each input sample, only one band output power is calculated in every sampling period, because it is not necessary to display all band power at each sampling period. (At 44.1 KHz sampling frequency, the period is only 0.0227 msec)

Vocal Canceller

The structure of vocal canceller function used in the KD16901 is given in Figure 18.

Figure 18. Structure of Vocal Canceller



This structure is based on the fact that the vocal component in music sound is center channel component (i.e., mono). Thus, subtracting left signal from right signal, the signal in the low line from above diagram has no vocal component. However, there are lots of loss in other signal components. For instance, since drum beat is usually mono, it also disappears after the vocal cancellation. The process in the upper line compensates this loss of some components. The added two signal is filtered by a band stop filter in which the lower and upper cutoff frequencies are 120 Hz and 10 KHz respectively. Thus, the stereo components below 120 Hz and above 10 KHz are emphasized, whereas the vocal components between cutoff frequencies are eliminated. To obtain the left and the right signals, the filtered signal is subtracted from the lower part of signals to obtain the left signal, and is added to the lower part of signal to obtain the right signal.

Loudness Control

The loudness control compensates human aural insensitivity to low and high frequency components of low volume level. Loudness control increases the tone levels of low (lower than 100 Hz) and high frequency (higher than 10 KHz) signals according to the actual volume setting. When loudness control is on, the current equalizer mode is stored and does not work until loudness control is turned off.

Figure 19. Loudness gain according to the actual volume setting

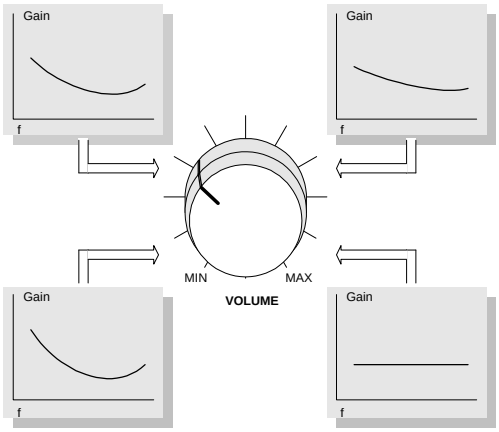
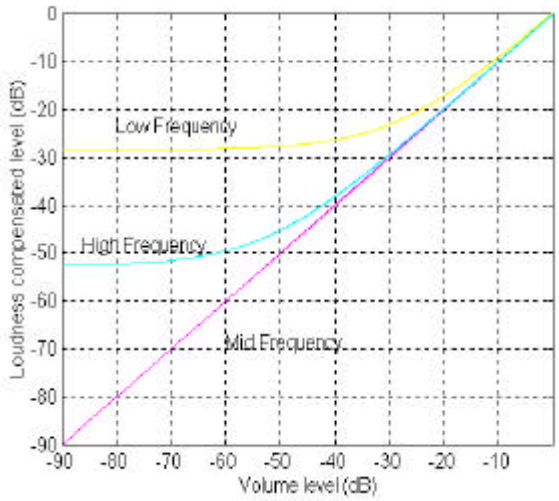


Figure 20. Loudness compensated level with respect to volume level



Volume Control

Volume control uses an attenuation table containing attenuation values, which has the size of 110 to implement 0 dB to –∞ dB attenuation.

Figure 21. Dynamic Range for Volume Control

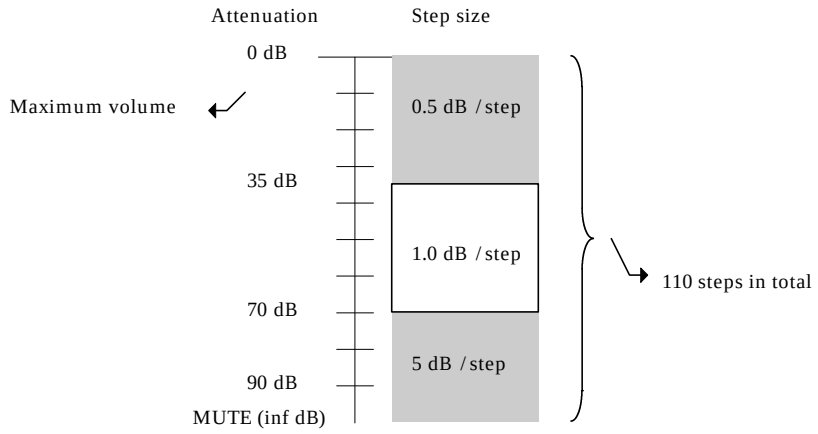


Table 12. Volume Gain Table

Index	Gain Value (Hex)	Gain Scale (dB)	Index	Gain Value (Hex)	Gain Scale (dB)
0	7fff	0	19	2ae0	-9.5
1	78d6	– 0.5	20	287a	-10.0
2	7214	– 1.0	21	2636	-10.5
3	6bb2	– 1.5	22	2413	-11.0
4	65ac	– 2.0	23	220e	-11.5
5	5ffc	– 2.5	24	2026	-12.0
6	5a9d	– 3.0	25	1e5a	-12.5
7	558c	– 3.5	26	1ca7	-13.0
8	50c3	– 4.0	27	1b0d	-13.5
9	4c3e	– 4.5	28	198a	-14.0
10	47fa	– 5.0	29	181c	-14.5
11	43f4	– 5.5	30	16c3	-15.0
12	4026	– 6.0	31	157d	-15.5
13	3c90	– 6.5	32	1449	-16.0
14	392c	– 7.0	33	1326	-16.5
15	35fa	-7.5	34	1214	-17.0
16	32f5	-8.0	35	1111	-17.5
17	301b	-8.5	36	101d	-18.0
18	2d6a	-9.0	37	0f36	-18.5

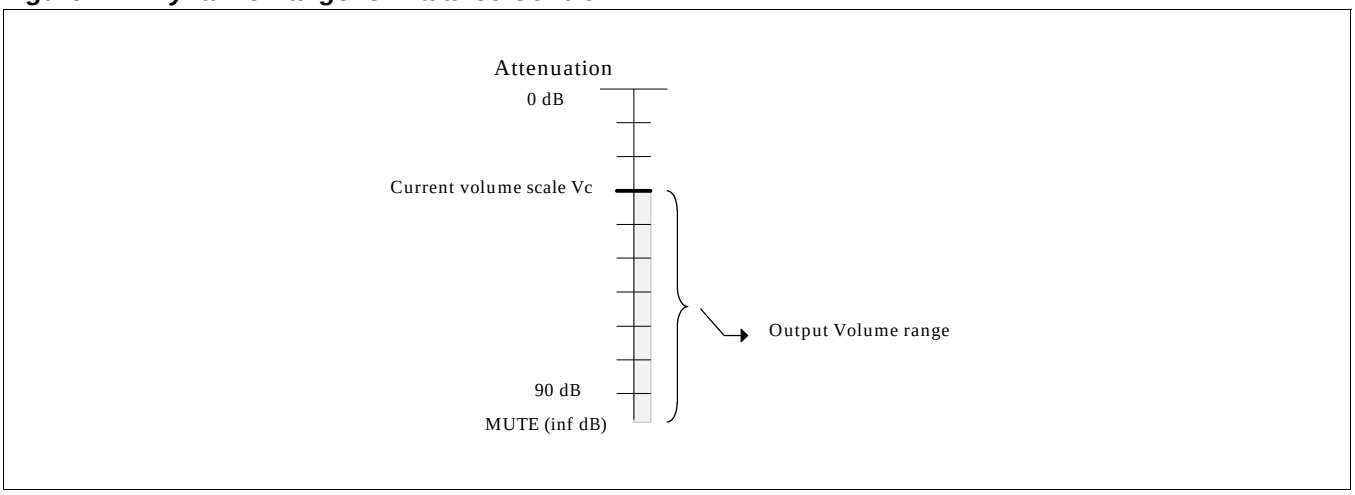
Table 12. Volume Gain Table

Index	Gain Value (Hex)	Gain Scale (dB)	Index	Gain Value (Hex)	Gain Scale (dB)
38	0e5c	-19.0	74	016f	-39.0
39	0d8e	-19.5	75	0147	-40.0
40	0ccc	-20.0	76	0124	-41.0
41	0c15	-20.5	77	0104	-42.0
42	0b68	-21.0	78	00e7	-43.0
43	0ac5	-21.5	79	00ce	-44.0
44	0a2a	-22.0	80	00b8	-45.0
45	0999	-22.5	81	00a4	-46.0
46	090f	-23.0	82	0092	-47.0
47	088e	-23.5	83	0082	-48.0
48	0813	-24.0	84	0074	-49.0
49	079f	-24.5	85	0067	-50.0
50	0732	-25.0	86	005c	-51.0
51	06cb	-25.5	87	0052	-52.0
52	066a	-26.0	88	0049	-53.0
53	060e	-26.5	89	0041	-54.0
54	05b7	-27.0	90	003a	-55.0
55	0565	-27.5	91	0033	-56.0
56	0518	-28.0	92	002e	-57.0
57	04cf	-28.5	93	0029	-58.0
58	048a	-29.0	94	0024	-59.0
59	0449	-29.5	95	0020	-60.0
60	040c	-30.0	96	001d	-61.0
61	03d2	-30.5	97	001a	-62.0
62	039b	-31.0	98	0017	-63.0
63	0367	-31.5	99	0014	-64.0
64	0337	-32.0	100	0012	-65.0
65	0309	-32.5	101	0010	-66.0
66	02dd	-33.0	102	000e	-67.0
67	02b4	-33.5	103	000d	-68.0
68	028d	-34.0	104	000b	-69.0
69	0269	-34.5	105	000a	-70.0
70	0246	-35.0	106	0005	-75.0
71	0207	-36.0	107	0003	-80.0
72	01ce	-37.0	108	0001	-85.0
73	019c	-38.0	109	0000	-∞

Balance Control

When balance control selects the left (right) channel, the right (left) channel diminishes. Balance control uses the same table that is used for volume control as in Table 12, which performs 0 dB to -∞ dB (mute) attenuation by 1 dB per step.

Figure 22. Dynamic Range for Balance Control

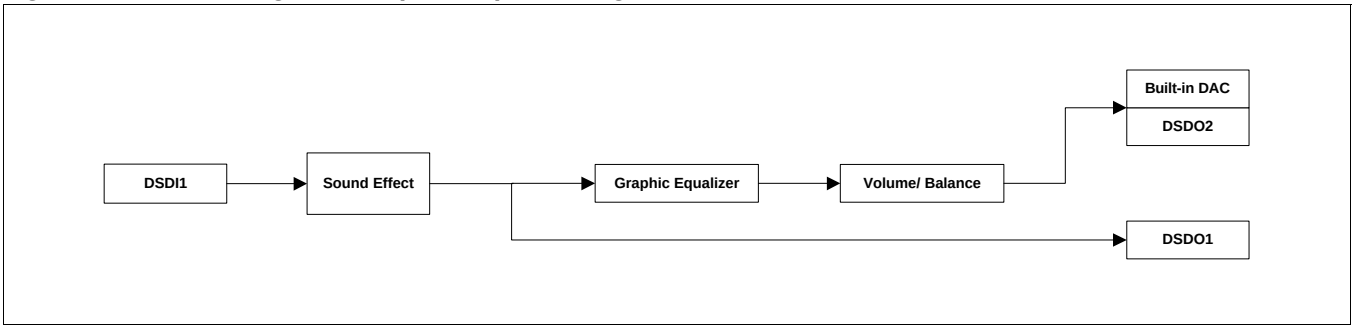


Input/Output Configurations

The KD16901 can receive one analog input from the built-in ADC and one digital input from DSDI1, or two digital inputs from DSDI1 and DSDI2 simultaneously. It can also send output to the built-in DAC, DSDO1 and DSDO2. As described in Chapter 4, the KD16901 has Mixing, Input/Output source selection and Bypass On-Chip Function to support a various Input/Output source configurations as described below.

- **Input/Output Configuration 1**

Figure 23. Block Diagram of Input/Output Configuration 1



For this configuration, one should set Mixing and Bypass On-Chip Function to be turned off while DSDI1 is enabled by using Chip Control Command as described in Chapter 4. The digital input from DSDI1 can be processed by one of sound effect modes. In output side, the signal effected by one of sound modes is passed to DSDO1, and the output after graphic equalizer followed by volume and balance control is passed to the built-in DAC and DSDO2. To obtain Configuration 1, one can send host commands from microcontroller in the order of the commands listed in Table 13.

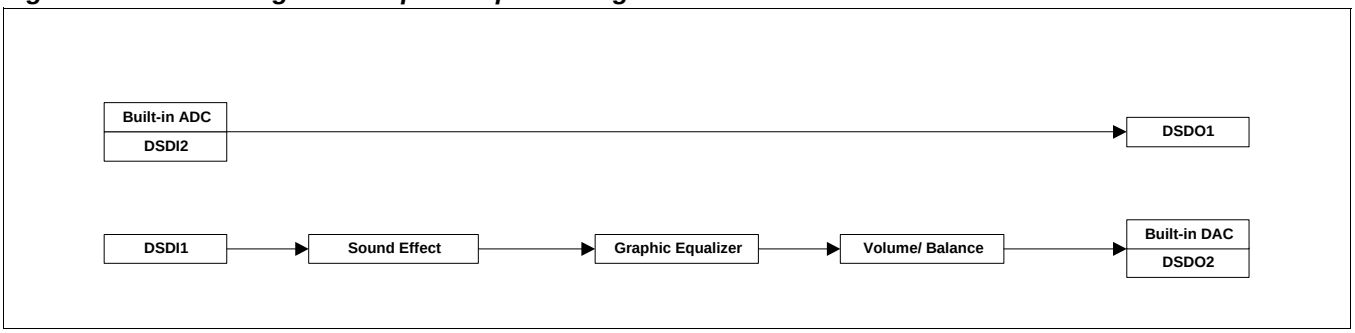
Table 13. Host Commands for Input/Output Configuration 1

Command Code (Hex)	Parameter	Description
34	c1 (e1)	Select DSDI1 (When DSDO1 uses internal clock)
2a	-	Bypass On-Chip Function: Off
2c	-	Mixing Function: Off
2d	-	Output Channel Selection: Normal

If one selects Output Channel Selection (command code: 0x2e) to be inverted, then two output connections are switched.

- **Input/Output Configuration 2**

Figure 24. Block Diagram of Input/Output Configuration 2



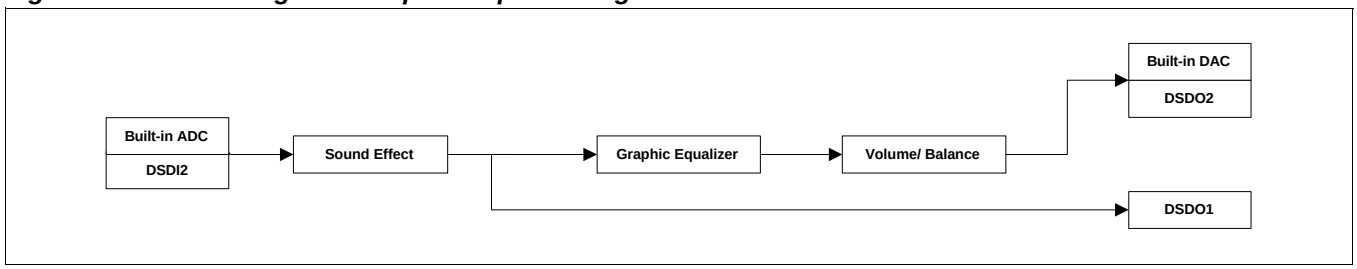
For this configuration, one should set Mixing to be turned off and Bypass On-Chip Function to be turned on. In this configuration, the KD16901 receives two digital input signals through DSDI1 and DSDI2, or one analog and one digital signals through the built-in ADC and DSDI1 respectively according to input channel configuration using Chip Control Command as described in Chapter 4. With this selection, the input from the built-in ADC or DSDI2 is bypassed to DSDO1 while the input from DSDI1 is processed by selected functions of the KD16901. Thus, it permits that other process, which the KD16901 does not provide, be applied to the digital signal from DSDO1. Also, this result can be an input to DSDI1 for further processing by functions of the KD16901 as shown in Figure 29. In this configuration, the Output Channel Selection cannot be inverted. To obtain Configuration 2, one can send host commands from microcontroller in the order of commands listed in Table 14.

Table 14. Host Commands for Input/Output Configuration 2

Command Code (Hex)	Parameter	Description
34	c3 (e3)	Select built-in ADC & DSDI1 (When DSDO1 uses internal clock)
	c4 (e4)	Select DSDI1 & DSDI2 (When DSDO1 uses internal clock)
29	-	Bypass On-Chip Function: On
2c	-	Mixing Function: Off

- **Input/Output Configuration 3**

Figure 25. Block Diagram of Input/Output Configuration 3



This configuration is exactly same as Configuration 1 except for input source. For this configuration, one should set Mixing and Bypass On-Chip Function to be turned off while the built-in ADC or DSDI2 is enabled.
To obtain Configuration 3, one can send host commands from microcontroller in the order of the commands listed in Table 15.

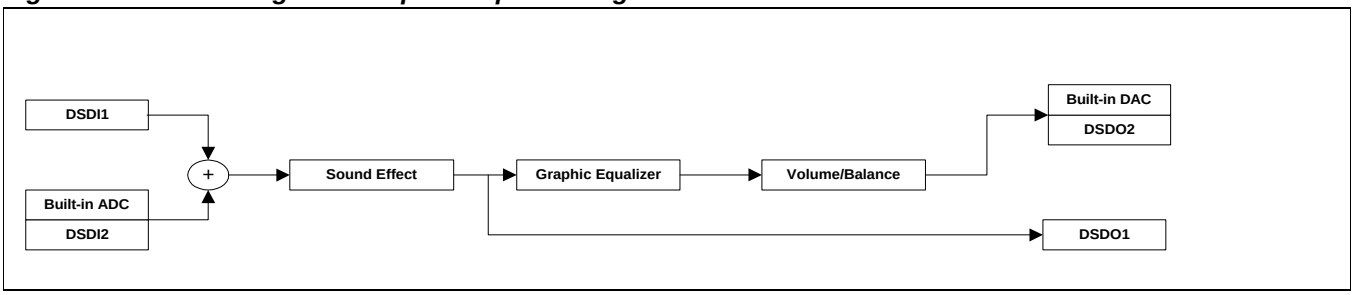
Table 15. Host Commands for Input/Output Configuration 3

Command Code (Hex)	Parameter	Description
34	c0 (e0)	Select built-in ADC (When DSDO1 uses internal clock)
	c2 (e2)	Select DSDI2 (When DSDO1 uses internal clock)
2a	-	Bypass On-Chip Function: Off
2c	-	Mixing Function: Off

If one selects Output Channel Selection (command code: 0x2e) to be inverted, then two output connections are switched.

- **Input/Output Configuration 4**

Figure 26. Block Diagram of Input/Output Configuration 4



For this configuration, one should set Mixing to be turned on and Bypass On-Chip Function to be turned off. Input signals from different sources can be mixed with controllable gains. After mixed, the flow is identical to Configuration 1 and 3. To obtain Configuration 4, one can send host commands from microcontroller in the order of the commands listed in Table 16.

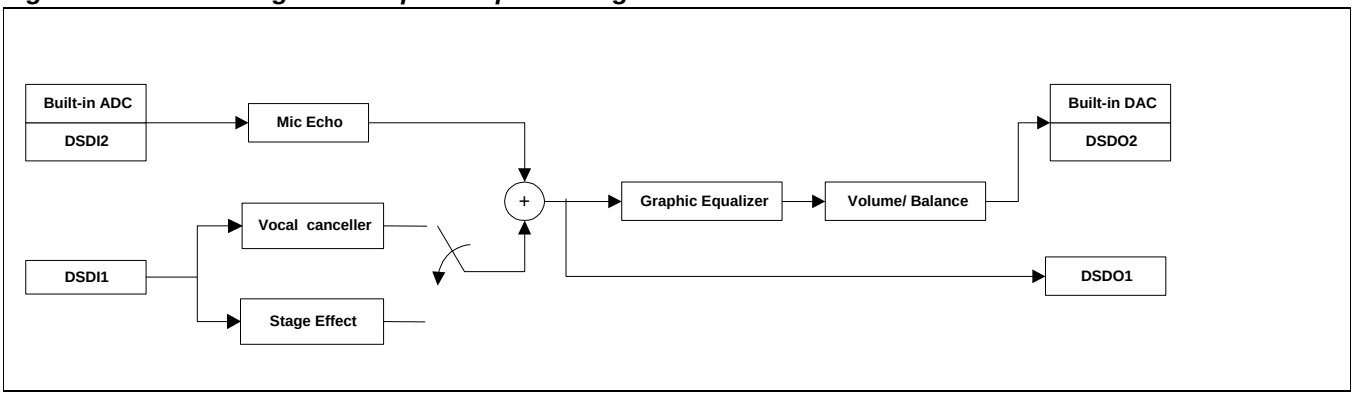
Table 16. Host Commands for Input/Output Configuration 4

Command Code (Hex)	Parameter	Description
34	c3 (e3)	Select built-in ADC & DSDI1 (When DSDO1 uses internal clock)
	c4 (e4)	Select DSDI1 & DSDI2 (When DSDO1 uses internal clock)
2a	-	Bypass On-Chip Function: Off
2b	-	Mixing Function: On
2d	-	Output Channel Selection: Normal

If one selects Output Channel Selection (command code: 0x2e) to be inverted, then two output connections are switched.

- **Input/Output Configuration 5**

Figure 27. Block Diagram of Input/Output Configuration 5



This configuration is for Karaoke Mode I. To have this configuration, one should set Mixing and Bypass On-Chip Function to be turned off. According to input channel source setting, one of inputs from the built-in ADC or DSDI2 is processed by mic-echo, and the other input from DSDI1 is processed by stage effect mode or by vocal canceller. After mixed, the result is bypassed to DSDO1. This signal is also passed to the built-in DAC and DSDO2 after processed by graphic equalizer, volume and balance control. To obtain Configuration 5, one can send host commands from microcontroller in the order of the commands listed in Table 17.

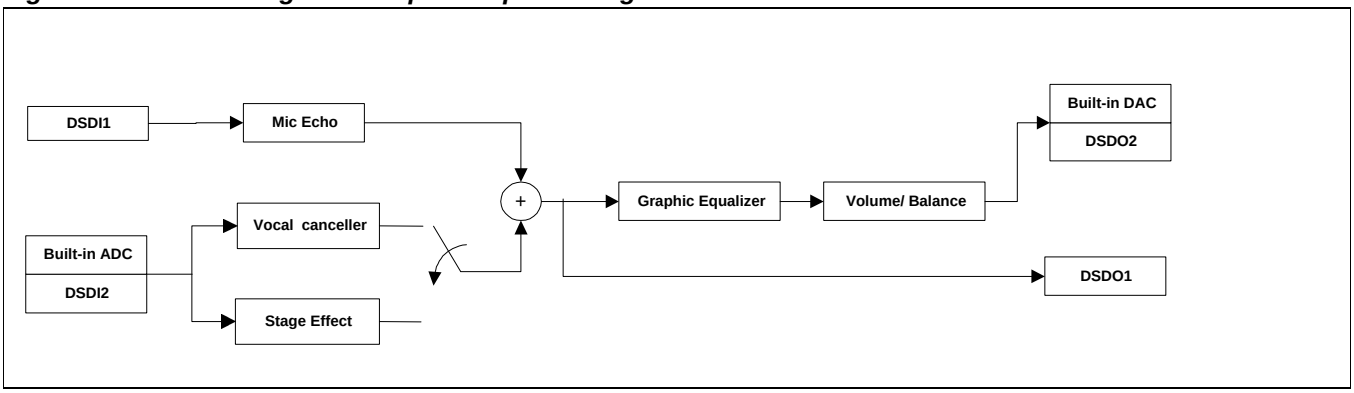
Table 17. Host Commands for Input/Output Configuration 5

Command Code (Hex)	Parameter	Description
34	c3 (e3)	Select built-in ADC & DSDI1 (When DSDO1 uses internal clock)
	c4 (e4)	Select DSDI1 & DSDI2 (When DSDO1 uses internal clock)
11	-	Select Karaoke Mode I
16	-	Source Selection in Karaoke Mode I: Normal
23 (24)	-	Vocal Canceller: On (Off)
2a	-	Bypass On-Chip Function: Off
2c	-	Mixing Function: Off
2d	-	Output Channel Selection: Normal

If one selects Output Channel Selection (command code: 0x2e) to be inverted, then two output connections are switched.

- **Input/Output Configuration 6**

Figure 28. Block Diagram of Input/Output Configuration 6



This configuration is also for Karaoke mode I as shown in Configuration 5. The difference between them is that sources for mic-echo and stage effect mode are exchanged. To obtain this configuration, one should set Input Source Selection in Karaoke I to be inverted and other switches (Mixing, Bypass On-Chip Function) to be turned off. To obtain Configuration 6, one can send host commands from microcontroller in the order of the commands listed in Table 18.

Table 18. Host Commands for Input/Output Configuration 6

Command Code (Hex)	Parameter	Description
34	c3 (e3)	Select built-in ADC & DSDI1 (When DSDO1 uses internal clock)
	c4 (e4)	Select DSDI1 & DSDI2 (When DSDO1 uses internal clock)
11	-	Select Karaoke Mode I
17	-	Source Selection in Karaoke Mode I: Inversion
23 (24)	-	Vocal Canceller: On (Off)
2a	-	Bypass On-Chip Function: Off
2c	-	Mixing Function: Off
2d	-	Output Channel Selection: Normal

If one selects Output Channel Selection (command code: 0x2e) to be inverted, then two output connections are switched.

Default Setting in KD16901

Table 19. Default Setting in KD16901

Functions	Selection	Remark
Sound Mode	Bypass	
Graphic Equalizer Mode	7-band	
Spectrum Analyzer	7-band	
Tone Level	0x0c	0 dB
Vocal Canceller	Off	
Loudness	Off	
Bypass On-Chip Function	Off	
Mixing	Off	
Output Channel Selection	Normal	
Input Gain (ADC/DSDI2)	0x3fff	–6 dB
Input Gain (DSDI1)	0x3fff	–6 dB
Output Gain (DSDO1)	0x3fff	–6 dB
Volume level	0x46	–35 dB
DSIU1ICR [7:0]	0x00	see Table 4
DSIU1OCR [7:0]	0x00	see Table 5
DSIU2ICR [7:0]	0x00	see Table 6
DSIU2OCR [7:0]	0x00	see Table 7
CHIPCR [7:0]	0xc3	see Table 8

4. COMMAND SET

The KD16902 receives data from and sends data to microcontroller through its HIU (Host Interface Unit) in the length of byte. It provides I^2C bus interface as well as normal microcontroller interface. To design and program a microcontroller, one may refer to the specification of host interface described in Chapter 2. The commands used in the KD16901 are classified into the three types as follows:

- Type1: Command Only (1 Byte Command)
- Type2: Command followed by Parameter (2 Byte Command)
- Type3: Command followed by Parameter 1 and Parameter 2 (3 Byte Command)

Note that all data regardless of types must be sent to the KD16901 in the length of byte. In type3, the high byte is followed by the low byte. The command class contained in each type are listed in the following table. (see also Table 44)

Table 20. Classification of Command

Type	Class
TYPE1	System Control
	Sound Mode Selection
	Source Selection in Karaoke I
	Graphic Equalizer Mode Selection
	Band Spectrum Request
	Vocal Canceller
	Loudness
	Mute/Release
	Bypass On-Chip Function
	Mixing
	Output Channel Selection
TYPE2	Digital Data Format & Input Configuration
	Volume
	Balance
	Mic-echo Scale
	Equalizer Tone Level Control
TYPE3	Input Gain Control
	Output Gain Control
	Parameters for User Defined Mode

Command Set Description

1) Reset

Format

Table 21. Command for Reset

Command Code (Hex)	Command Name
00	Reset

Description

All parameters are changed to default values and no sound mode is selected.

2) System Power Down

Format

Table 22. Command for System Power Down

Command Code (Hex)	Command Name
03	System Power Down

Description

Disable DSP and built-in peripherals. Enabled by any host interrupt.

3) Sound Mode Selection

Format

Table 23. Commands for Sound Mode Selection

Command Code (Hex)	Command Name	Command Code (Hex)	Command Name
05	Bypass	0e	Arena I
06	Stereo Emulation I	0f	Arena II
07	Stereo Emulation II	10	News/Drama
08	Super Woofer I	11	Karaoke I
09	Super Woofer II	12	Karaoke II
0a	Super Woofer III	13	User Defined Mode
0b	Hall I	14	Movie I
0c	Hall II	15	Movie II
0d	Stage		

Description

The KD16901 presents various sound effect and Movie modes as listed above. For detailed description on each mode, refer to ‘Functional Description”in Chapter 3.

4) Source Selection in Karaoke Mode I

Format

Table 24. Commands for Source Selection in Karaoke Mode I

Command Code (Hex)	Command Name
16	Normal
17	Inversion

Description

In Karaoke mode I, two input sources are processed by mic-echo and stage effect mode respectively, and then, they are mixed. In normal selection, the signal coming from built-in ADC or DSDI2 is the input for mic-echo, and the signal coming from DSDI1 is the input for stage effect mode. In inversion selection, the signal coming from built-in ADC or DSDI2 is the input for stage mode, and the signal coming from DSDI1 is the input for mic-echo.

Source Selection	Input Source	
	Mic-Echo	Stage Effect
Normal	ADC or DSDI2	DSDI1
Inversion	DSDI1	ADC or DSDI2

5) Graphic Equalizer Mode Selection

Format

Table 25. Commands for Graphic Equalizer Mode Selection

Command Code (Hex)	Command Name
18	3-band Tone Control
19	5-band Tone Control
1a	7-band Tone Control
1b	Defeat

Description

The KD16901 provides 3, 5 or 7-band equalizer mode and tone control. For detailed description on graphic equalizer and tone control, refer to "Functional Description" in Chapter 3.

Note that if loudness function is selected, then any equalizer mode cannot be selected. After an equalizer mode is selected, tone level of each band is controlled by Tone Control Command.

- To select an equalizer mode, the loudness function should be turned off

6) Spectrum Value Request

Format

Table 26. Commands for Spectrum Value Request

Command Code (Hex)	Command Name
1c	Band0 in 5/7-band equalizer mode
1d	Band1 in 5/7-band equalizer mode
1e	Band2 in 5/7-band equalizer mode
1f	Band3 in 5/7-band equalizer mode
20	Band4 in 5/7-band equalizer mode
21	Band5 in 7-band equalizer mode
22	Band6 in 7-band equalizer mode

Description

The KD16901 provides spectrum data corresponding to 5/7-band equalizer mode to host (microcontroller). The spectrum value of each band is calculated in every sampling period. When the spectrum value of a specific band is requested by host, the one-word spectrum value (16 bit) is transformed to a byte value (8 bit) through built-in spectrum interface unit to transfer to host.

Requested Spectrum Value	Transferred Spectrum Value	Condition
Spectrum [Band [i]] [15:0]	Spectrum [Band [i]] [11:4]	Spectrum [Band [i]] < 2^{12}
	2^7	Spectrum [Band [i]] > 2^{11}

7) Vocal Canceller

Format

Table 27. Commands for Vocal Canceller

Command Code (Hex)	Command Name
23	Vocal Canceller On
24	Vocal Canceller Off

Description

The vocal canceller function is used to decrease the level of vocal component from a music source. It is useful function for Karaoke modes to distinct the vocal component from a microphone and the vocal component from music sound. In Movie modes, the vocal canceller is not supported since input source is usually movie sound.

8) Loudness

Format

Table 28. Commands for Loudness

Command Code (Hex)	Command Name
25	Loudness On
26	Loudness Off

Description

The loudness function compensates the low and high frequency components for relatively low volume level so that one can listen a sound evenly for all frequency ranges. Note that while the loudness is on, the tone level control does not work because it uses specified tone levels. The changed tone values are updated after the loudness is turned off.

9) Mute/Release

Format

Table 29. Commands for Mute and Release

Command Code (Hex)	Command Name
27	Mute
28	Release

Description

In mute, the volume level is set to – ∞ dB. Selecting release, the volume level before mute is recovered. By changing volume level in mute, the mute release is also invoked. In this case, the volume level is not recovered by the volume level before mute, but updated by selected volume level.

10) Bypass On-Chip Function

Format

Table 30. Commands for Bypass On-Chip Function

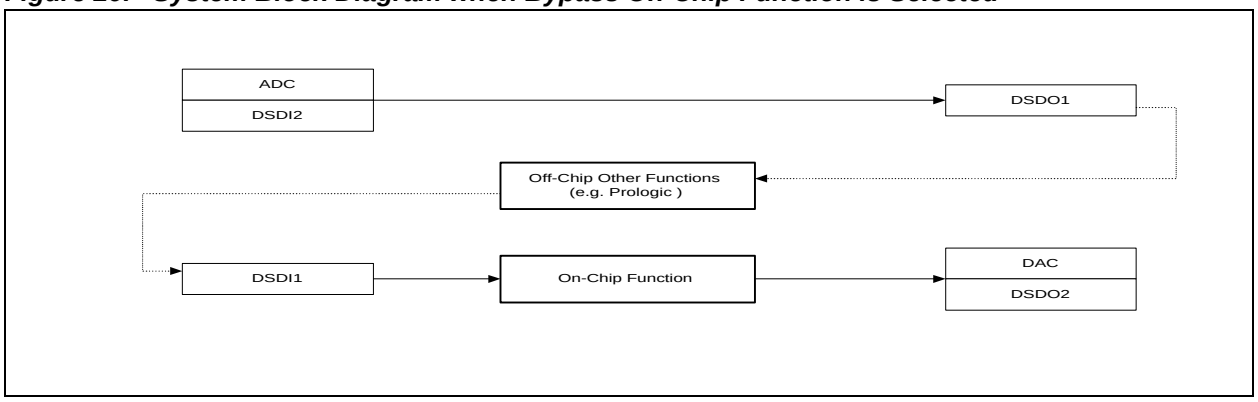
Command Code (Hex)	Command Name
29	Selection
2a	No Selection

Description

With the selection of this function, the input from built-in ADC or DSDI2 is bypassed to DSDO1 while the input from DSDI1 is processed by functions of the KD16901. Thus, it permits that other functions, which are not available in the KD16901, can be applied to the digital output from DSDO1. This result can also be an input to DSDI1 for further processing by functions of the KD16901. Note that this function cannot be selected in Karaoke modes since these modes require two input sources. If the mixing function is selected previously, it is automatically turned off with the selection of Bypass On-Chip Function.

- In Karaoke modes, Bypass On-Chip Function cannot be selected
- When Bypass On-Chip Function is selected, the Mixing is automatically turned off if it is on.

Figure 29. System Block Diagram when Bypass On-Chip Function is Selected



11) Mixing

Format

Table 31. Commands for Mixing

Command Code (Hex)	Command Name
2b	Mixing On
2c	Mixing Off

Description

This function is to mix two inputs with appropriate mixing gains using input gain control commands, and the result is processed by functions of the KD16901. After mixed, the result is the input for a sound mode, and thus, the mixing function cannot be selected in Karaoke modes. If Bypass On-Chip Function is selected previously, it is automatically turned off with the selection of mixing function.

- In Karaoke modes, the mixing function cannot be selected
- When the mixing function is selected, the Bypass On-Chip Function is automatically turned off if it is on.

12) Output Channel Inversion

Format

Table 32. Commands for Output Channel Inversion

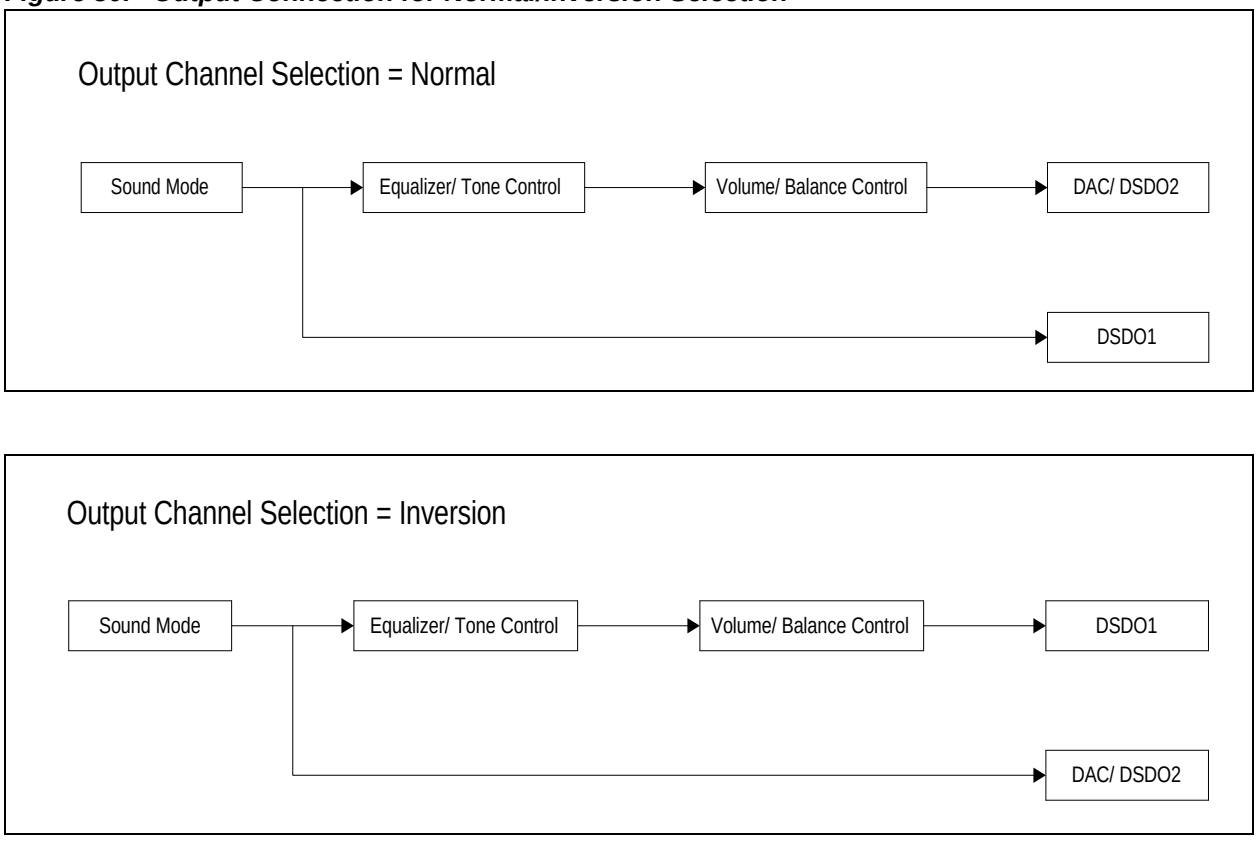
Command Code (Hex)	Command Name
2d	Normal
2e	Inversion

Description

In normal selection of output channel, the output of a sound mode is passed to DSDO1 for recording before processed by equalizer, volume and balance. After further processed by equalizer, volume and balance, this result is passed to built-in DAC and DSDO2. In the case of inversion, the outputs to DSDO1 and built-in DAC/DSDO2 are switched. Note that this function cannot be selected if Bypass On-Chip Function is selected already.

- The output channel cannot be inverted if the Bypass On-Chip Function is selected.

Figure 30. Output Connection for Normal/Inversion Selection



13) DSIU1 Input Format

Format

Table 33. Command for DSIU1 Input Format

Command Code (Hex)	DSIU1ICR	Command Name
30	[7:0]	DSIU1 Input Format

Description

The KD16901 supports various input and output digital formats. After the command, desired format can be set using DSIU1ICR [7:0]. (see Table 4 for setting)

14) DSIU1 Output Format

Format

Table 34. Command for DSIU1 Output Format

Command Code (Hex)	DSIU1OCR	Command Name
31	[7:0]	DSIU1 Output Format

Description

The KD16901 supports various input and output digital formats. After the command, desired format can be set using DSIU1OCR [7:0]. (see Table 5 for setting)

15) DSIU2 Input Format

Format

Table 35. Command for DSIU2 Input Format

Command Code (Hex)	DSIU2ICR	Command Name
32	[7:0]	DSIU2 Input Format

Description

The KD16901 supports various input and output digital formats. After the command, desired format can be set using DSIU2ICR [7:0]. (see Table 6 for setting)

16) DSIU2 Output Format

Format

Table 36. Command for DSIU2 Output Format

Command Code (Hex)	DSIU2OCR	Command Name
33	[7:0]	DSIU2 Output Format

Description

The data length and bit rate for DSDO2 are fixed to 16 bit and 32xFs respectively. Note that the data position for DSDO2 supports IIS or right justified. The data position for built-in ADC and DAC also follows that of DSDO2. After the command, desired format can be set using DSIU2OCR [7:0]. (see Table 7 for setting)

17) Chip Control

Format

Table 37. Command for Chip Control

Command Code (Hex)	CHIPCR	Command Name
34	[7:0]	Chip Control

Description

The format for chip control sets input channel configuration and interrupt control, and selects clock source for DSDO1 using CHIPCR [7:0]. (see Table 8 for setting)

18) Volume Control

Format

Table 38. Command for Volume Control

Command Code (Hex)	Volume_index	Command Name
35	[7:0]	Volume Control

Description

The KD16901 provides 110 levels in volume control. The desired volume level is invoked by selecting its index using incoming byte, Volume_index [7:0]. The index of the highest volume level corresponds to 0x00 (0 dB attenuation), and that of the lowest volume level corresponds to 0x6d (–∞ dB attenuation).

- Minimum volume index 0x6d corresponds to –∞ dB attenuation
- Maximum volume index 0x00 corresponds to 0 dB attenuation

19) Balance Control

Format

Table 39. Command for Balance Control

Command Code (Hex)	Balance_index	Command Name
36	[7:0]	Balance Control

Description

The MSB of Balance_control [7:0] represents balance left if it is 0 and balance right if it is 1. The volume index used in volume control is also used for balance control, i.e., 0x00 to 0x6d as follows:

- For balance left, Balance_control [7:0] has the range of 0x00 (equal balance) to 0x6d (max balance)
- For balance right: Balance_control [7:0] has the range of 0x80 (equal balance) to 0xed (max balance)

In balance left (right), the volume level of the left (right) channel is kept, whereas the volume of the right (left) channel is attenuated by the scale corresponding to Balance_index [7:0].

20) Tone Control

Format

Table 40. Commands for Tone Control

Command Code (Hex)	Tone_index	Command Name
38	[7:0]	Band0 Tone Value in 3/5/7-band equalizer mode
39		Band1 Tone Value in 3/5/7-band equalizer mode
3a		Band2 Tone Value in 3/5/7-band equalizer mode
3b		Band3 Tone Value in 5/7-band equalizer mode
3c		Band4 Tone Value in 5/7-band equalizer mode
3d		Band5 Tone Value in 7-band equalizer mode
3e		Band6 Tone Value in 7-band equalizer mode

Description

The KD16901 provides 25 levels of tone level for each band according to selected equalizer mode. This tone level is set by using incoming byte, Tone_index [7:0], after the command. Levels have the range of 0x00 (min) to 0x18 (max). Note that if the loudness function is on, then the tone control does not work since tone levels are preset in this case. Changed tone values while the loudness function is on, are updated as soon as the loudness function is turned off.

- While the loudness function is being selected, the tone control is not permitted

21) Input Gain Control

Format

Table 41. Commands for Input Gain Control

Command Code (Hex)	High Byte	Low Byte	Command Name
46	Ingain_adc [15:8]	Ingain_adc [7:0]	Input Gain Control of ADC or DSDI2
47	Ingain_dsdi1 [15:8]	Ingain_dsdi1 [7:0]	Input Gain Control of DSDI1

Description

The KD16901 permits to control the input gains of ADC (or DSDI2) and DSDI1 using incoming two bytes after the command. The preset values for input gains are 0x3fff (6 dB attenuation) in both.

22) Output Gain Control

Format

Table 42. Command for Output Gain Control

Command Code (Hex)	High Byte	Low Byte	Command Name
48	Outgain_dsdo1 [15:8]	Outgain_dsdo1 [7:0]	Output Gain Control of DSDO1

Description

The KD16901 permits to control the output gain of DSDO1 using incoming two bytes after the command. The preset value for output gain is 0x3fff (6 dB attenuation). Note that to control the output gain of DAC and DSDO2, the volume control can be used.

23) Parameters for User Defined Mode

Format

Table 43. Commands for Setting Parameters of User Defined Mode

Command Code (Hex)	High Byte	Low Byte	Command Name
49	G0 [15:8]	G0 [7:0]	Gain for Left Input
4a	G1 [15:8]	G1 [7:0]	Gain for Right Input
4b	BL0 [15:8]	BL0 [7:0]	Prefilter Coeff. (Left)
4c	BL1 [15:8]	BL1 [7:0]	Prefilter Coeff. (Left)
4d	AL1 [15:8]	AL1 [7:0]	Prefilter Coeff. (Left)
4e	BR0 [15:8]	BR0 [7:0]	Prefilter Coeff. (Right)
4f	BR1 [15:8]	BR1 [7:0]	Prefilter Coeff. (Right)
50	AR1 [15:8]	AR1 [7:0]	Prefilter Coeff. (Right)
51	G2 [15:8]	G2 [7:0]	Gain for Left Term
52	G3 [15:8]	G3 [7:0]	Gain for Right Term
53	G4 [15:8]	G4 [7:0]	Gain for Feedback Term
54	BD0 [15:8]	BD0 [7:0]	Postfilter Coeff.
55	BD1 [15:8]	BD1 [7:0]	Postfilter Coeff.
56	AD1 [15:8]	AD1 [7:0]	Postfilter Coeff.
57	G5 [15:8]	G5 [7:0]	Gain for T1 Delay Term (Left)
58	G6 [15:8]	G6 [7:0]	Gain for T2 Delay Term (Left)
59	G7 [15:8]	G7 [7:0]	Gain for T3 Delay Term (Left)
5a	G8 [15:8]	G8 [7:0]	Gain for T4 Delay Term (Left)
5b	G9 [15:8]	G9 [7:0]	Gain for T5 Delay Term (Left)
5c	G10 [15:8]	G10 [7:0]	Gain for T6 Delay Term (Left)
5d	G11 [15:8]	G11 [7:0]	Gain for T7 Delay Term (Left)
5e	G12 [15:8]	G12 [7:0]	Gain for Left Effected Term
5f	G13 [15:8]	G13 [7:0]	Gain for Left Original Term
60	G14 [15:8]	G14 [7:0]	Gain for T1 Delay Term (Right)
61	G15 [15:8]	G15 [7:0]	Gain for T2 Delay Term (Right)
62	G16 [15:8]	G16 [7:0]	Gain for T3 Delay Term (Right)
63	G17 [15:8]	G17 [7:0]	Gain for T4 Delay Term (Right)
64	G18 [15:8]	G18 [7:0]	Gain for T5 Delay Term (Right)
65	G19 [15:8]	G19 [7:0]	Gain for T6 Delay Term (Right)
66	G20 [15:8]	G20 [7:0]	Gain for T7 Delay Term (Right)
67	G21 [15:8]	G21 [7:0]	Gain for Right Effected Term
68	G22 [15:8]	G22 [7:0]	Gain for Right Original Term
69	T0 [15:8]	T0 [7:0]	Delay Buffer Pointer of T0
6a	Tc [15:8]	Tc [7:0]	Current Delay Buffer Pointer

Table 43. Commands for Setting Parameters of User Defined Mode

Command Code (Hex)	High Byte	Low Byte	Command Name
6b	T1 [15:8]	T1 [7:0]	Delay Buffer Pointer of T1
6c	T2 [15:8]	T2 [7:0]	Delay Buffer Pointer of T2
6d	T3 [15:8]	T3 [7:0]	Delay Buffer Pointer of T3
6e	T4 [15:8]	T4 [7:0]	Delay Buffer Pointer of T4
6f	T5 [15:8]	T5 [7:0]	Delay Buffer Pointer of T5
70	T6 [15:8]	T6 [7:0]	Delay Buffer Pointer of T6
71	T7 [15:8]	T7 [7:0]	Delay Buffer Pointer of T7

Description

These parameters are provided for user to design his or her own sound mode. The list of parameters (see Block Diagram for User Defined Mode in Chapter 3.) is one of sound modes provided in the KD16901. In fact, most of sound modes in the KD16901, e.g., hall, super woofer and so on, have similar structure. By changing parameters given in Figure 16, one can obtain completely different sound mode. Loading parameters which are redefined by user can be done in running of any sound mode since the memory site for these parameters does not overlap with that for any other modes. Designed mode after loading all parameters to DSP is defined as User Defined Mode. To run this mode, simply select the command code 0x13 (see Command for Mode Selection).

Command Summary

Table 44. The List of Commands for Audio Effect Processor (KD16901)

Command Code (Hex)	Class	Command Name	Function
00	System Control	Reset	Reset parameters to default values and select no sound mode
01		Reserved	
02		Reserved	
03		System Power Down	Disable DSP and built-in peripherals
04	Reserved		
05	Sound Mode	Bypass	For sound mode description, see Chapter 3
06		Stereo Emulation I	
07		Stereo Emulation II	
08		Super Woofer I	
09		Super Woofer II	
0a		Super Woofer III	
0b		Hall I	
0c		Hall II	
0d		Stage	
0e		Arena I	
0f		Arena II	
10		News/Drama	
11		Karaoke I	
12		Karaoke II	
13		User Defined Mode	
14		Movie I	
15		Movie II	
16	Source Selection in Karaoke I	Normal	Input for mic-echo comes from built-in ADC or DSDI2. Input for stage mode comes from DSDI1
17		Inversion	The above input sources are exchanged
18	Equalizer Mode	3-band mode	3-band tone control
19		5-band mode	5-band tone control
1a		7-band mode	7-band tone control
1b		Defeat	No selection

Table 44. The List of Commands for Audio Effect Processor (KD16901)

Command Code (Hex)	Class	Command Name	Function
1c	Spectrum Request	Band0	Request band0 spectrum value in 5/7-band tone mode
1d		Band1	Request band1 spectrum value in 5/7-band tone mode
1e		Band2	Request band2 spectrum value in 5/7-band tone mode
1f		Band3	Request band3 spectrum value in 5/7-band tone mode
20		Band4	Request band4 spectrum value in 5/7-band tone mode
21		Band5	Request band5 spectrum value in 7-band tone mode
22		Band6	Request band6 spectrum value in 7-band tone mode
23	Vocal Canceller	On	Cancel vocal component in a sound mode except for Movie I, II
24		Off	No selection
25	Loudness	On	Emphasis low & high freq. components according to volume level
26		Off	No selection
27	Mute	On	Set volume level to – ∞ dB
28		Off	Recover the volume level
29	Bypass On Chip Function	On	Bypass input from built-in ADC or DSDI2 to DSDO1
2a		Off	No selection
2b	Mixing	On	Two input signals are added to produce an input for sound mode
2c		Off	No selection
2d	Output Channel Selection	Normal	The result effected by sound mode is passed to DSDO1 for recording The result further controlled by equalizer, volume and balance is passed to built-in DAC and DSDO2 for speaker output
2e		Inversion	The above connection is exchanged
2f	Reserved		

Table 44. The List of Commands for Audio Effect Processor (KD16901)

Command Code (Hex)	Class	Command Name	Function
30	Digital data format & Input Configuration	Format for DSDI1	Select format for digital input source1 using incoming byte
31		Format for DSDO1	Select format for digital output source1 using incoming byte
32		Format for DSDI2	Select format for digital input source2 using incoming byte
33		Format for DSDO2	Select format for digital output source2 using incoming byte
34		Format for Chip Control	Define Input Configuration & Control Interrupt using incoming byte
35	Volume	Volume Control	Set volume level using incoming byte 0 x 00: max level, 0 x 6d: min level
36	Balance	Balance Left/Right Control	Set left/right balance level using incoming byte Balance left: 0 x 00 (min) to 0 x 6d (max) Balance right: 0 x 80 (min) to 0 x ed (max)
37	Mic-echo scale	Mic-echo scale	Select mic-echo delay using incoming byte 0 x 01 (min delay) to 0 x 05 (max delay)
38	Equalizer Tone Level Control	Band0 Tone Level	Set band0 tone level in 3/5/7-band mode using incoming byte 0 x 00 (min level) to 0 x 18 (max level)
39		Band1 Tone Level	Set band1 tone level in 3/5/7-band mode using incoming byte
3a		Band2 Tone Level	Set band2 tone level in 3/5/7-band mode using incoming byte
3b		Band3 Tone Level	Set band3 tone level in 5/7-band mode using incoming byte
3c		Band4 Tone Level	Set band4 tone level in 5/7-band mode using incoming byte
3d		Band5 Tone Level	Set band5 tone level in 7-band mode using incoming byte
3e		Band6 Tone Level	Set band6 tone level in 7-band mode using incoming byte
3f	Reserved for Host Test		
40			

Table 44. The List of Commands for Audio Effect Processor (KD16901)

Command Code (Hex)	Class	Command Name	Function
41	Reserved		
42			
43			
44			
45			
46	Input Gain control	Built-in ADC & DSDI2 Input Gain Value	Set input gain value for built-in ADC & DSDI2 using incoming two bytes
47		DSDI1 Input Gain Value	Set input gain for DSDI1 using incoming two bytes
48	Output Gain Control	DSDO1 Output Gain Value	Set output gain for DSDO1 using incoming two bytes
49	Parameters for User Defined Mode (see Block Diagram in Chapter 3)	G0	Set left input gain using incoming 2 bytes
4a		G1	Set right input gain using incoming two bytes
4b		BL0	Set left prefilter coeff. using incoming two bytes
4c		BL1	
4d		AL1	
4e		BR0	Set right prefilter coeff. using incoming two bytes
4f		BR1	
50		AR1	
51		G2	Set left term gain using incoming two bytes
52		G3	Set right term gain using incoming two bytes
53		G4	Set feedback term gain using incoming two bytes
54		BD0	Set postfilter coeff. using incoming two bytes
55		BD1	
56		AD1	
57		G5	Set left delay gains using incoming two bytes
58		G6	
59		G7	
5a		G8	
5b		G9	
5c		G10	
5d		G11	

Table 44. The List of Commands for Audio Effect Processor (KD16901)

Command Code (Hex)	Class	Command Name	Function
5e	Parameters for User Defined Mode (see Block Diagram in Chapter 3)	G12	Set left effected term gain using incoming two bytes
5f		G13	Set left original term gain using incoming two bytes
60		G14	Set right delay gains using incoming two bytes
61		G15	
62		G16	
63		G17	
64		G18	
65		G19	
66		G20	
67		G21	Set right effected term gain using incoming two bytes
68		G22	Set right original term gain using incoming two bytes
69		T0	Set delay buffer pointer using incoming two bytes (Delay pointer should follow inequality: 0 x 1800 > T0 > T7 > T6 > T5 > T4 > T3 > T2 > T1)
6a		Tc	
6b		T1	
6c		T2	
6d		T3	
6e		T4	
6f		T5	
70		T6	
71		T7	

Notification for microcontroller programming

Fade-in/ Fade-out:

To avoid noise due to abrupt change of signal, hardware configuration or filter coefficients, the fade-out and fade-in processes in the KD16901 happen in following situations.

- Change sound mode
- Change equalizer mode
- Change hardware configuration related to 'Digital data format and Input configuration".
- Change 'Source selection in Karaoke mode I"
- 'Vocal Canceller" is turned on or off
- 'Loudness Function" is turned on or off
- "Mixing Function" is turned on or off
- 'Bypass On-chip Function" is turned on or off
- 'Output channel selection" is turned into reversion from normal, or vise versa.

The time for finishing fade-out and fade-in processes needs about 0.9 ms for sound mode change and about 0.4 ms for other cases. Note that the KD16901 denies process of any function received from microcontroller during fade-out or fade-in process.

Sound Mode Selection:

- When one of Karaoke modes is selected, 'Bypass On-chip Function" or "Mixing Function" is automatically turned off if one of them is turned on and 'Source selection in Karaoke I" is set to normal. Thus, the microcontroller should change the status of "Mixing Function", 'Bypass On-chip Function" and 'Source selection in Karaoke I" at this time. Note that 'Source selection in Karaoke I" can be inverted only in Karaoke mode I.

Equalizer Mode Selection:

- Equalizer modes and loudness function are exclusive, and thus, equalizer mode cannot be selected while loudness function is working. To select equalizer mode, the loudness function should be turned off first.

Equalizer Tone Control:

- Due to the bug of the KD16901, careful programming is needed to control tone value of the sixth filter in seven band equalizer mode. In the seven band graphic equalizer mode, the tone value of the seventh band is first saved before changing the tone value of the sixth band. For example, if the desired tone value of the sixth band is 0x12 (0dB scale), then give the command for tone control of the seventh band with this parameter. Then, give the command for tone control of the sixth band again. At this time, the parameter can be arbitrary since it is ignored. Finally, the saved tone value of the seventh band is recovered. This problem is not involved in 3-band and 5-band equalizer modes. Even in 7-band equalizer mode, this problem is restricted in the tone control of the sixth band, and also restricted in evaluation samples.

Vocal Canceller:

- Movie modes do not work with this function. In KD16901, this function is ignored in one of Movie modes. Thus, if the sound mode is one of Movie modes, the microcontroller dose not make this function to be selected.

5. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Characteristics	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.3 ~ +7.0	V
DC Input Voltage	V_I	– 0.3 ~ V_{DD} + 0.3	V
DC Input Current	I_{IN}	±10	mA
Storage Temperature	T_{stg}	– 40 ~ +125	°C

Recommended Operating Conditions

Characteristics	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	4.75 ~ 5.25	V
DC Input Voltage	V_I	0 ~ V_{DD}	V
Commercial Temperature	T_A	0 ~ +70	°C
Industrial Temperature		-40 ~ +85	°C

DC Characteristics (V_{DD} = 4.75 ~ 5.25 V, T_a = 0 ~ 70 °C)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}	CMOS	0.7 V_{DD}	-	-	V
Low Level Input Voltage	V_{IL}	CMOS	-	-	0.3 V_{DD}	V
Switching Threshold	V_T	CMOS	-	2.5	-	V
Schmitt trigger, positive-going threshold	V_{T+}	CMOS	-	-	4.0	V
Schmitt trigger, negative-going threshold	V_{T-}	CMOS	1.0	-	-	V
High Level Input Current	I_{IH}	V_{IN} = V_{DD} (Input Buffer)	-10		10	µA
		V_{IN} = V_{DD} (with pull-down)	10	50	100	µA
Low Level Input Current	I_{IL}	V_{IN} = V_{SS} (Input Buffer)	-10		10	µA
		V_{IN} = V_{SS} (with pull-up)	-100	-50	-10	µA
High Level Output Voltage	V_{OH}	I_{OH} = -1mA	2.4	-	-	V
Low Level Output Voltage	V_{OL}	I_{OL} = 1mA	-	-	0.4	V
Operating Current	I_{DD}	XI = 16.9344 MHz		120	150	mA
Static Current	I_{ST}	XI = 16.9344 MHz		10		mA
Operating Frequency	F_{OSC}	CLKS = 0		16.9344 MHz	±5	%

Codec Analog Characteristics

Parameter	Min	Typ	Max	Unit
Sampling Rate (Fs)	4	44.1	50	KHz
Over Sampling Rate	-	128	-	Fs
Master Clock Frequency	-	256	-	Fs
ADC Resolution	-	16	-	bits
DAC Resolution	-	16	-	bits
Passband	0	-	0.4 Fs	Hz
Stopband	0.4 Fs	-	0.6 Fs	Hz
Common Mode Voltage	-	2.38	-	V
Output Capacitive Load	-	-	10	pF
Output Resistive Load	50	-	-	KΩ

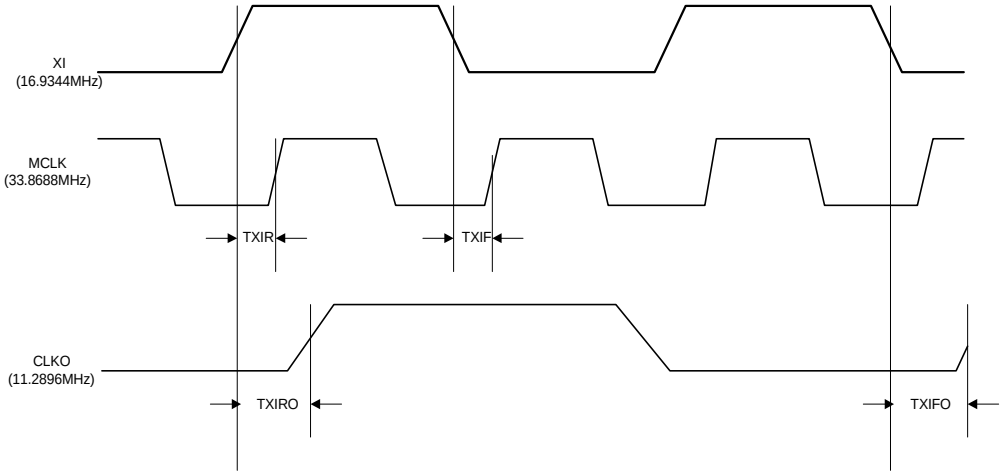
Analog Input Characteristics (ADC)

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage @ -2dB	-	-	1	Vrms
ADC Signal to Noise Ratio (SNR)	90	95	-	dB
ADC Signal to (Noise + Distortion) Ratio (SNDR), measurement bandwidth is 20Hz ~ 20KHz with 1 Vrms @ 1.1 KHz	75	80	-	dB
ADC Offset Error	-	-	80	mV
Total Harmonic Distortion (THD)	-	0.01	0.02	%

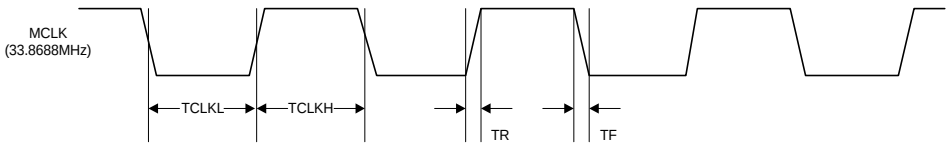
Analog Output Characteristics (DAC)

Parameter	Min	Typ	Max	Unit
Full Scale Output Voltage @ 0dB	-	1	-	Vrms
DAC Signal to Noise Ratio (SNR)	90	95	-	dB
DAC Signal to (Noise + Distortion) Ratio (SNDR)	60	65	-	dB
DAC Offset Error	-	-	80	mV

System Clock and Reset



X-tal Oscillator SYSTEM CLOCK(CLKS=0)

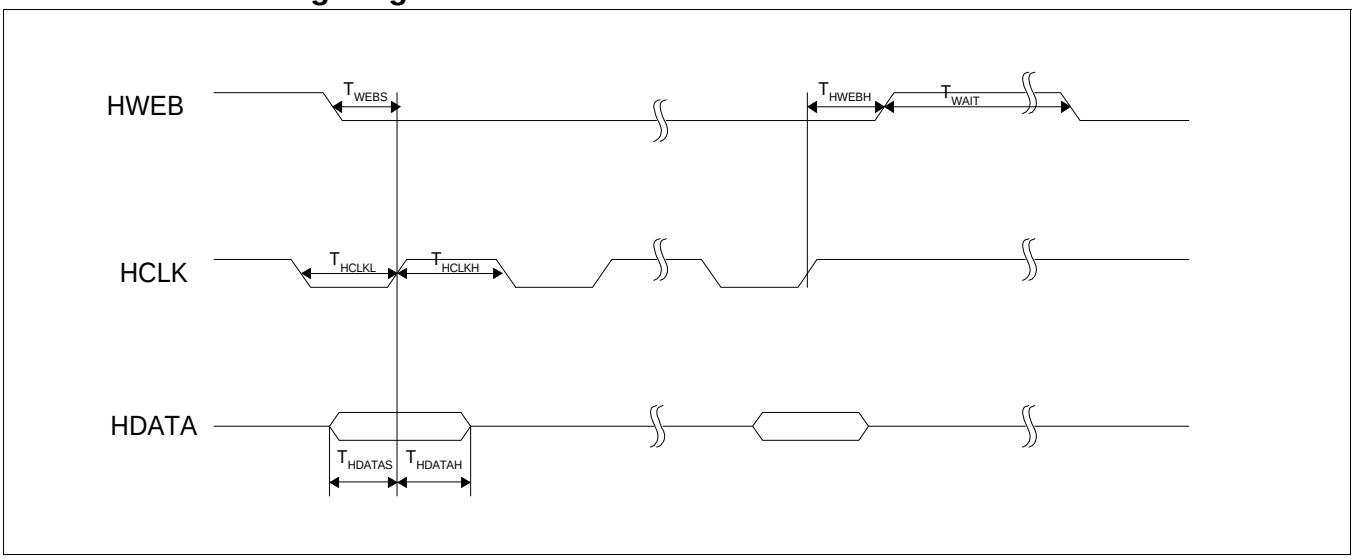


External SYSTEM CLOCK(CLKS=1)

SYSTEM RESET

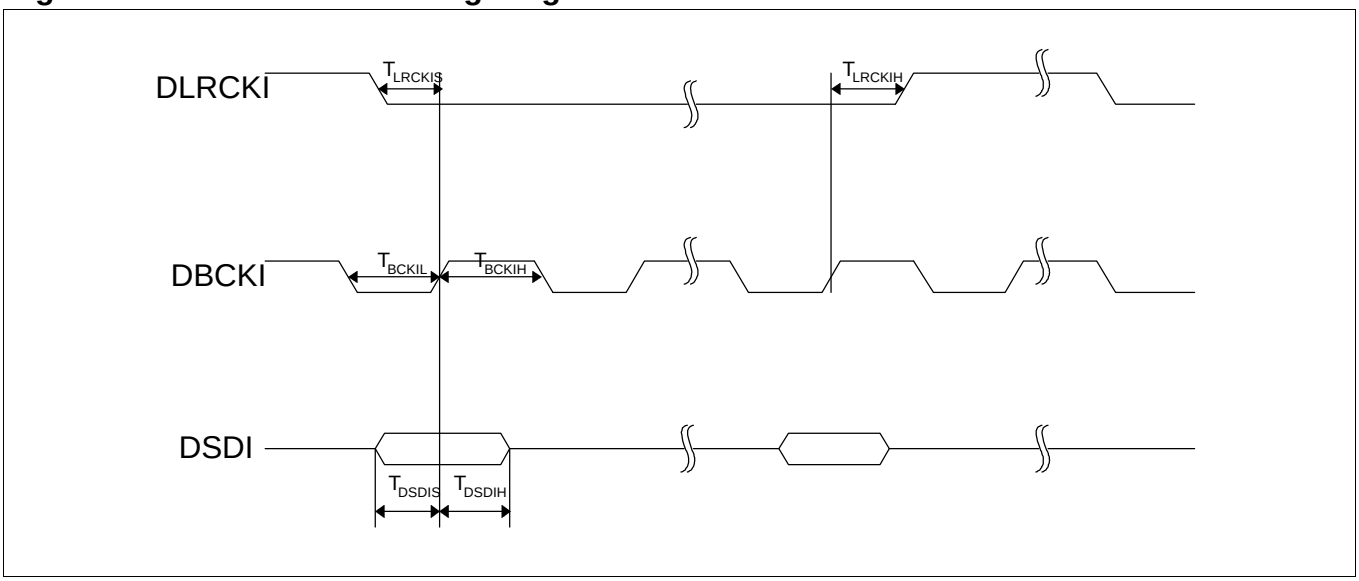
AC Characteristics	Symbol	Min	Typ	Max	Unit
XI Rise Edge to MCLK	T_{XIR}	-	10	-	ns
XI Fall Edge to MCLK	T_{XIF}	-	11	-	ns
XI Rise to CLKO	T_{XIRO}	-	12	-	ns
XI Fall to CLKO	T_{XIFO}	-	13	-	ns
External Clock High Width	T_{CLKH}	-	14.75	-	ns
External Clock Low Width	T_{CLKL}	-	14.75	-	ns
External Clock Rise Time	T_R	-	-	2	ns
External Clock Fall Time	T_F	-	-	2	ns
Reset Pulse Width	T_{RESB}	22.6	-	-	µs

Host Interface Timing Diagram

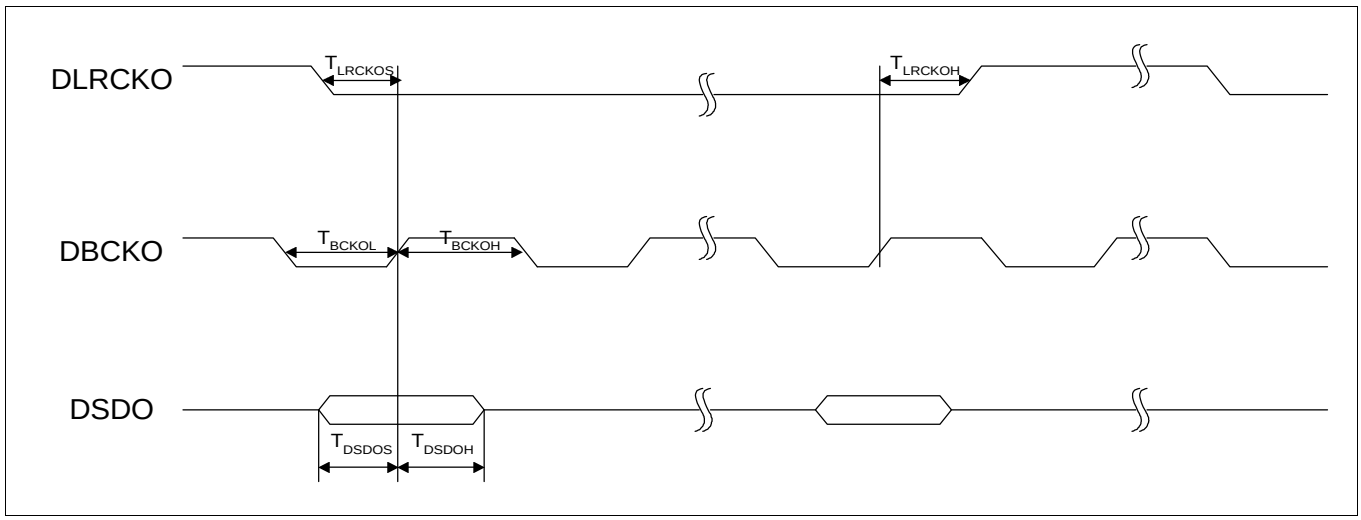


AC Characteristics	Symbol	Min	Typ	Max	Unit
HWEB Setup to First HCLK Edge	T_{WEBS}	50	-	-	ns
HWEB Hold to Last HCLK Edge	T_{WEBH}	50	-	-	ns
HCLK Pulse Width High	T_{HCLKH}	1.25	-	-	µs
HCLK Pulse Width Low	T_{HCLKL}	1.25	-	-	µs
HDATA Input Setup Time	T_{HDATAS}	50	-	-	ns
HDATA Input Hold Time	T_{HDATAH}	50	-	-	ns
HWEB Wait Time	T_{WAIT}	1	-	-	ms

Digital Audio Interface 1 Timing Diagram



AC Characteristics	Symbol	Min	Typ	Max	Unit
DLRCKI Setup to First DBCKI Edge	T_{LRCKIS}	20	-	-	ns
DLRCKI Hold to Last DBCKI Edge	T_{LRCKIH}	20	-	-	ns
DBCKI Pulse Width High	T_{DBCKIH}	177	-	354	ns
DBCKI Pulse Width Low	T_{DBCKIL}	177	-	354	ns
DSDI Input Setup Time	T_{DSDIS}	10	-	-	ns
DSDI Input Hold Time	T_{DSDIH}	10	-	-	ns



AC Characteristics	Symbol	Min	Typ	Max	Unit
DLRCKO Setup to First DBCKO Edge	T_{LRCKOS}	20	-	-	ns
DLRCKO Hold to Last DBCKO Edge	T_{LRCKOH}	20	-	-	ns
DBCKO Pulse Width High	T_{DBCKOH}	177	-	354	ns
DBCKO Pulse Width Low	T_{DBCKOL}	177	-	354	ns
DSDO Output Setup Time	T_{DSDOS}	10	-	T_{BCKOL} - 10	ns
DSDO Output Hold Time	T_{DSDOH}	10	-	T_{BCKOH}	ns