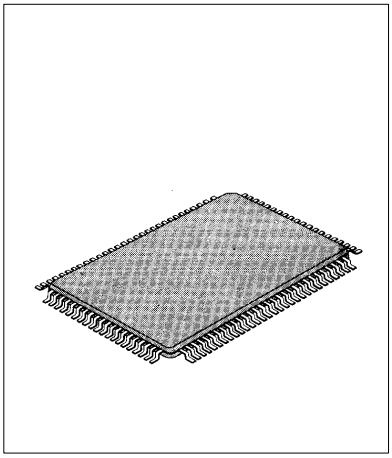
## INTRODUCTION

**100 QFP**



KS0083/84 is a graphic type LCD driver LSl which is fabricated by CMOS process for high voltage. In case of segment driver, can be selected 4 bit, 1 bit data transfer or chip select mode. KS0084 is reverse type of KS0083

## FUNCTION

- Dot matrix LCD driver with 80 channel output.
- lnput/Output
  - Output: 80 channel waveform for LCD driving
  - Intput: • parallel display data and control signal from controller
    • bias voltage ($V_3$, $V_4$, $V_{SS}$, $V_{EE}$ )

## FEATURES

- Power supply voltage: + 5V±10% ($V_{DD}$)
- LCD driving voltage: -24V(typ) ($V_{EE}$)
- Interface

| type 1 | | type 2 | | type 3 | |
|---|---|---|---|---|---|
| COMMON | SEGMENT | COMMON | SEGMENT | COMMON | SEGMENT |
| KS0083/84<br>KS0086 | KS0083/84<br>KS0086 | KS0103 | KS0083/84<br>KS0086 | KS0083/84<br>KS0086 | KS0104/B |

- l00QFP and bare chip available

## BLOCK DIAGRAM

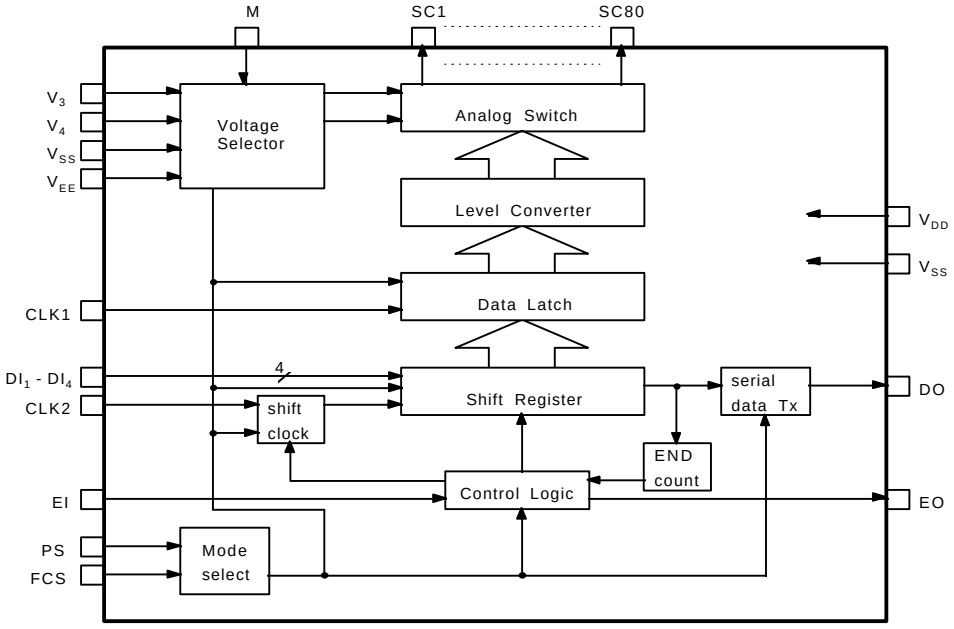



Fig. 1 KS0083/84 functional block diagram.

## PIN CONFIGURATION

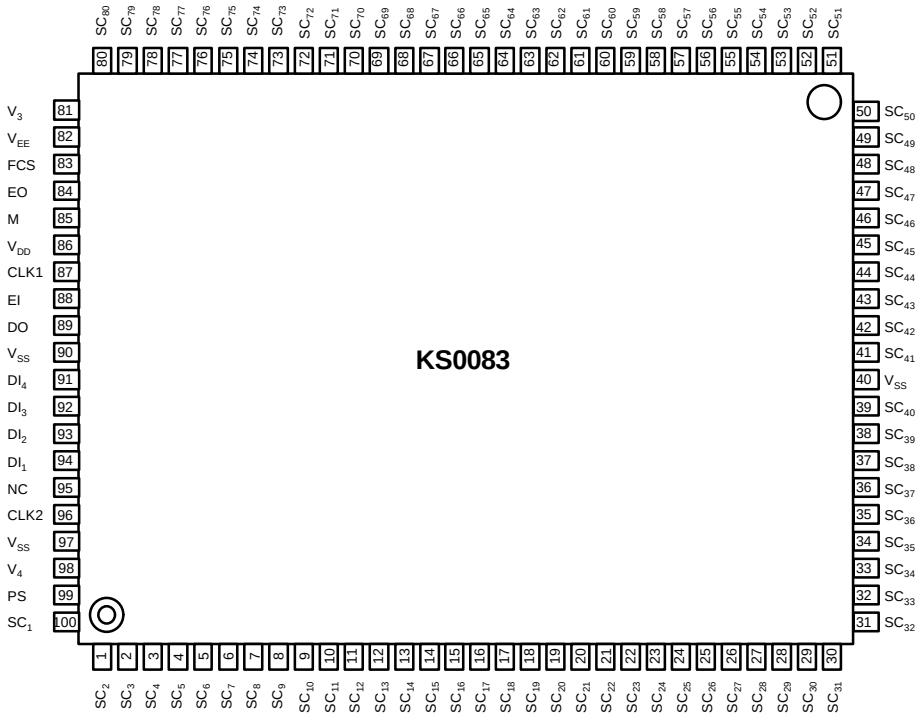



Fig. 2. 100 QFP Top View

## PIN CONFIGURATION

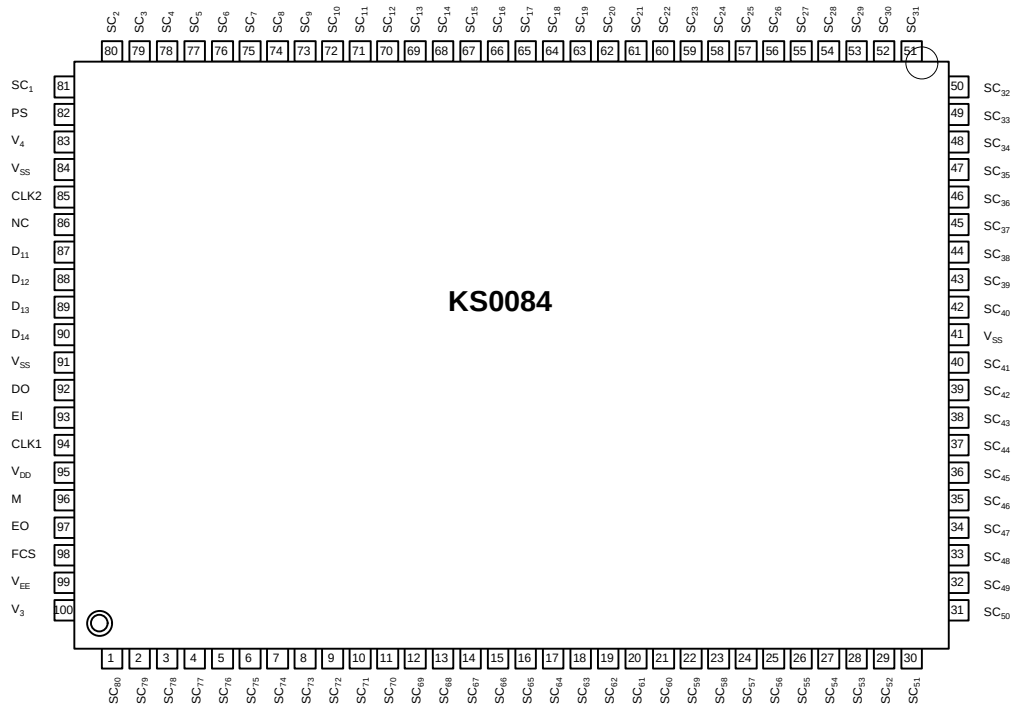
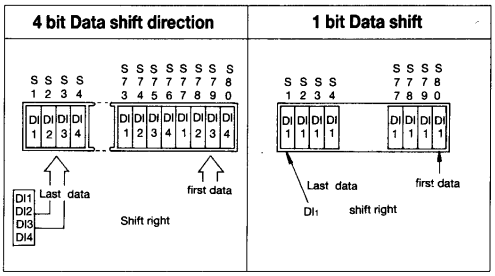



**Fig.3 100QFP Top View.**

## PIN FUCTIONAL DESCRIPTION

<table>
<tr><th colspan="2">PIN</th><th>INPUT OUTPUT</th><th>DESCRIPTION</th><th>INTERFACE</th></tr>
<tr><td rowspan="3">Power Supply</td><td>$V_{SS}$</td><td rowspan="3">Power</td><td>GND(0V)</td><td rowspan="3"></td></tr>
<tr><td>$V_{EE}$</td><td>LCD drivingvoltage (typ.-24V)</td></tr>
<tr><td>$V_{DD}$</td><td>Internal logic driving voltage (typ.-5V)</td></tr>
<tr><td colspan="2">$V_3$,$V_4$</td><td>Input</td><td>Bias Voltage input for LCD drive: Non-selct Level (Must maintain VSS>V3>V4>VEE.)</td><td>LCD</td></tr>
<tr><td colspan="2">$SC_1$ ~ $SC_{80}$</td><td>Output</td><td>LCD driver output terminal (80 Channel)</td><td>LCD</td></tr>
<tr><td colspan="2">FCS, PS</td><td>Input</td><td>Mode select inputs. (refer to application circuit)
<table>
<tr><th>FCS</th><th>PS</th><th>Com/Seg driver</th><th>Input mode</th><th>Chip select mode</th><th>DO Output</th></tr>
<tr><td>L</td><td>L</td><td>Segment driver</td><td>1 bit serial input</td><td>X</td><td>O</td></tr>
<tr><td>L</td><td>H</td><td>Segment driver</td><td>4 bit parallel input</td><td>O</td><td>H</td></tr>
<tr><td>H</td><td>L</td><td>Segment driver</td><td>1 bit serial input</td><td>X</td><td>H</td></tr>
<tr><td>H</td><td>H</td><td>Common driver</td><td>Serial input</td><td>O</td><td>O</td></tr>
</table>
- In case of serial input mode, DI1 is data input pin and DO is data output pin<br>
- In case of 4 bit parallel input mode, Data input and output are;
<table>
<tr><td>$DI_1$</td><td>$SC_1$, $SC_5$, ... $SC_{77}$</td><td>$DI_2$</td><td>$SC_2$, $SC_6$, ... $SC_{78}$</td></tr>
<tr><td>$DI_3$</td><td>$SC_3$, $SC_7$, ... $SC_{70}$</td><td>$DI_4$</td><td>$SC_4$, $SC_8$, ... $SC_{80}$</td></tr>
</table>


- In case of the common driver, the data transfer clock is CLK2<br>
- Non-used data input pins are set to $V_{SS}$ or $V_{DD}$ to minimize current consumption</td><td></td></tr>
</table>

**PIN DESCRIPTION**(continued)

<table>
<tr><th>PIN</th><th>INPUT<br>OUTPUT</th><th>DESCRIPTION</th><th>INTERFACE</th></tr>
<tr><td>EO, EI</td><td>Input<br>Output</td><td>Input/Output for Chip Select.<br>1) EO becomes low by (CLK1, CLK2) timing.<br>2) When “HIGH” data is input to EI, the device becomes select mode and reads input data at CLK2 falling timing.<br>Synchronized at the fall of CLK2. Input data is shifted.<br>3) After reading 80 input data(equivalent to 80 CLK2 clock cycle in the serial mode or 20 CLK2 clock cycles in the 4 bit parallel,mode) ,EO automatically becomes“ HIGH” level and data reading is complete. EO is reset 1.5 cycles later.<br>4) When two or more devices are used in the chip select mode, EO of each state is connected to EI of the next state.<br>(1) EO of all device connected is reset and device becomes non-select state and waits for EI input after the previous 1).<br>(2) When “HIGH” level is input to the first EI in the cascade connection, the first device performs the operation in 2) and 3).<br>(3) When EI of the second device is connected to EO of the first device, the second device perform the operations 2) and 3) after the first device. This operation is repeated in the same method subsequently</td><td>Controller<br>or<br>KS0083/84</td></tr>
<tr><td>M</td><td>Input</td><td>LCD waveform AC conversion signal input
<table>
<tr><th>Latch data</th><th>M</th><th>SC</th></tr>
<tr><td rowspan="2">L<br>(non-select)</td><td>L</td><td>$V_3$</td></tr>
<tr><td>H</td><td>$V_4$</td></tr>
<tr><td rowspan="2">H<br>(select)</td><td>L</td><td>GND</td></tr>
<tr><td>H</td><td>$V_{EE}$</td></tr>
</table>
(segment signal drive mode)
<table>
<tr><th>Latch data</th><th>M</th><th>SC</th></tr>
<tr><td rowspan="2">L<br>(non-select)</td><td>L</td><td>$V_3$</td></tr>
<tr><td>H</td><td>$V_4$</td></tr>
<tr><td rowspan="2">H<br>(select)</td><td>L</td><td>$V_{EE}$</td></tr>
<tr><td>H</td><td>GND</td></tr>
</table>
(common signal drive mode)</td><td>Controller</td></tr>
<tr><td>CLK1</td><td>Input</td><td>Clock pulse input terminal for data latch</td><td>Controller</td></tr>
<tr><td>CLK2</td><td>Input</td><td>Clock pulse input terminal for data shift</td><td>Controller</td></tr>
<tr><td>DI1 ~ DI4</td><td>Input</td><td>Display data input from the LCD controller LSI.<br>In case of the common driver mode or serial input mode, supply the input data to DI1 and DI2 ~ DI4 have to be set to $V_{SS}$ level or $V_{DD}$ level.</td><td>Controller</td></tr>
<tr><td>DO</td><td>Output</td><td>DO is high level in the chip select mode</td><td>KS0083/84</td></tr>
<tr><td>NC</td><td></td><td>Non-Connection</td><td>NC</td></tr>
</table>

## MAXIMUM ABSOLUTE LIMIT

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Operating Voltage | $V_{DD}$ | -7 ~ +0.3 | V |
| Driver Supply Voltage | $V_{LCD}$ | -30 ~ +0.3 | |
| Input Voltage | $V_{IN}$ | $V_{DD}$-0.3 ~ +0.3 | |
| Operating Temperature | $T_{OPR}$ | - 30 ~ + 85 | °C |
| Storage Temperature | $T_{STG}$ | - 55 ~ +150 | |

* Voltage greater than above may damage to the circuit.
Maximum absolute ilmits are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device beyond them is not implied. Long exposure to these conditions may affect device reliability.

## ELECTRICAL CHARACTERISTICS

### DC Characteristics ($V_{DD}$= -5V±10%, Vss=0V, $V_{EE}$= -24V$_i$±V, Ta=-30 ~ +85°C)

| Characteristiec | | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Operating Current | | $I_{DD}$ | 1 bit serial (3.3MHz) | - | - | 5.0 | mA |
| | | | 4 bit parallel (2.0MHz) | - | - | 10.0 | mA |
| Input Voltage | High | $I_{IH}$ | - | 0.2$V_{DD}$ | - | - | V |
| | Low | $I_{IL}$ | - | - | - | 0.8$V_{DD}$ | V |
| Output Voltage | High | $I_{OH}$ | $I_{OH}$=-0.4mA | -0.4 | - | - | V |
| | Low | $I_{OL}$ | $I_{OL}$=0.4mA | - | - | $V_{DD}$+0.4 | V |
| Voltage | | $V_{D1}$ | $I_{ON}$=1mA for one of SCi | - | - | 1.0 | V |
| Descending (Vi-SCi) | | $V_{D2}$ | $I_{ON}$=0.08mA for each SCi | - | - | 1.5 | V |
| Leakage Current | Input | $I_{LKG}$ | - | - | - | 1.0 | µA |
| | Output | $I_{O(LKG)}$ | - | - | - | 10.0 | µA |

## AC Characteristics

($V_{DD}$=-5V±10%, $V_{SS}$=0V, $V_{EE}$=-24V±3V; Ta=-30 ~ +85°C)

(1) Segment driver1; 1 bit serial data input (PS=Low, FCS=Low) (refer to: Fig. 3)

| Characteristic | Symbol | condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Clock Cycle Time | $t_{CY}$ | - | 300 | - | ns |
| Clock Pulse Width High Level | $t_{WCKH}$ | - | 130 | - | |
| Clock Pulse Width Low Level | $t_{WCKL}$ | - | 130 | - | |
| Set Up Time D Before CLK2¡é | $t_{SU}$ | - | 70 | - | |
| Hold Time D After CLK2¡é | $t_H$ | - | 50 | - | |
| Clock Margin Time 1 (From CLK1¡éTo CLK2¡é) | $t_{C1}$ | - | 20 | - | |
| Clock Margin Time 2 (From CLK2¡éTo CLK1¡é) | $t_{C2}$ | - | 200 | - | |
| Clock Margin Time 3 (From CLK2¡èTo CLK1¡è) | $t_{C3}$ | - | 20 | - | |
| Clock Rise/Fall Time | $t_R$, $t_F$ | - | - | 50 | |
| Output Delay Time | $t_D$ | $C_L$=15pF | - | 230 | |
| High Level Latch Clock Width | $t_{LWH}$ | - | 130 | - | |
| Overlap Time Of CLK2 "L" And CLK1 "H" | $t_{OV}$ | - | 130 | - | |

(2) segment driver; 4 bit data input (PS=High, FCS=Low) (refer to: fig. 4)

| Characteristic | Symbol | condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Clock Cycle Time | $t_{CY}$ | - | 500 | - | ns |
| Clock Pulse Width High Level | $t_{WCKH}$ | - | 230 | - | |
| Clock Pulse Width Low Level | $t_{WCKL}$ | - | 230 | - | |
| Set Up Time D Before CLK2↓ | $t_{SU}$ | - | 70 | - | |
| Hold Time D After CLK2↓ | $t_H$ | - | 50 | - | |
| Clock Margin Time 1 (From CLK1¡éTo CLK2↓) | $t_{C1}$ | - | 20 | - | |
| Clock Margin Time 2 (From CLK2¡éTo CLK1↓) | $t_{C2}$ | - | 200 | - | |
| Clock Margin Time 3 (From CLK2¡èTo CLK1↓) | $t_{C3}$ | - | 20 | - | |
| Clock Rise/Fall Time | $t_R$, $t_F$ | - | | 50 | |
| Output Delay Time | $t_D$ | $C_L$=15pF | | 230 | |
| High Level Latch Clock Width | $t_{LWH}$ | - | 130 | - | |
| Overlap Time Of CLK2 "L" And CLK1 "H" | $t_{OV}$ | - | 130 | - | |

(3) Common Driver (PS=High, FCS=High) (refer to: Fig. 5)

| Characteristic | | Symbol | condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Clock Cycle Time | | $t_{CY}$ | - | 1000 | - | ns |
| Clock Pulse Width | High Level | $t_{WCKH}$ | - | 130 | - | |
| | Low Level | $t_{WCKL}$ | - | 830 | - | |
| Set-Up Time D before CLK↓ | | $t_{SU}$ | - | 70 | - | |
| Hold Time D after CLK↓ | | $t_H$ | - | 50 | - | |
| Output Delay Time | | $t_D$ | $C_L$=15pF | - | 500 | |
| Clock Rise/Fall Time | | $t_R$, $t_F$ | - | - | 50 | |

(4) segment driver 2; 1 bit serial data input (PS=Low, FCS=High) (refer to: Fig. 6)

| Characteristic | | Symbol | condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Clock Cycle Time | | $t_{CY}$ | - | 380 | - | ns |
| Clock Pulse Width | High Level | $t_{WCKH}$ | - | 170 | - | |
| | Low Level | $t_{WCKL}$ | | | | |
| Set Up Time D Before CLK↓ | | $t_{SU}$ | - | 70 | - | |
| Hold Time D After CLK↓ | | $t_H$ | - | 50 | - | |
| Clock Margin Time 1 (From CLK1↓To CLK2↓) | | $t_{C1}$ | - | 20 | - | |
| Clock Margin Time 2 (From CLK2↓To CLK1↓) | | $t_{C2}$ | - | 200 | - | |
| Clock Margin Time 3 (From CLK2↓To CLK1↓) | | $t_{C3}$ | - | 20 | - | |
| Clock Rise/Fall Time | | $t_R$, $t_F$ | - | | 50 | |
| Output Delay Time | | $t_D$ | $C_L$=15pF | | 230 | |
| High Level Latch Clock Width | | $t_{LWH}$ | - | 130 | - | |
| Overlap Time Of CLK2 "L" And CLK1 "H" | | $t_{OV}$ | - | 130 | - | |

NOTE : Input frequency, I/O reference level; $0.8V_{DD}$, $0.2V_{DD}$
1; Valid time (internal shift register)
2; $(t_c x 1.5)-(t_{C1})-(t_{C3})-(t_R x 3)$

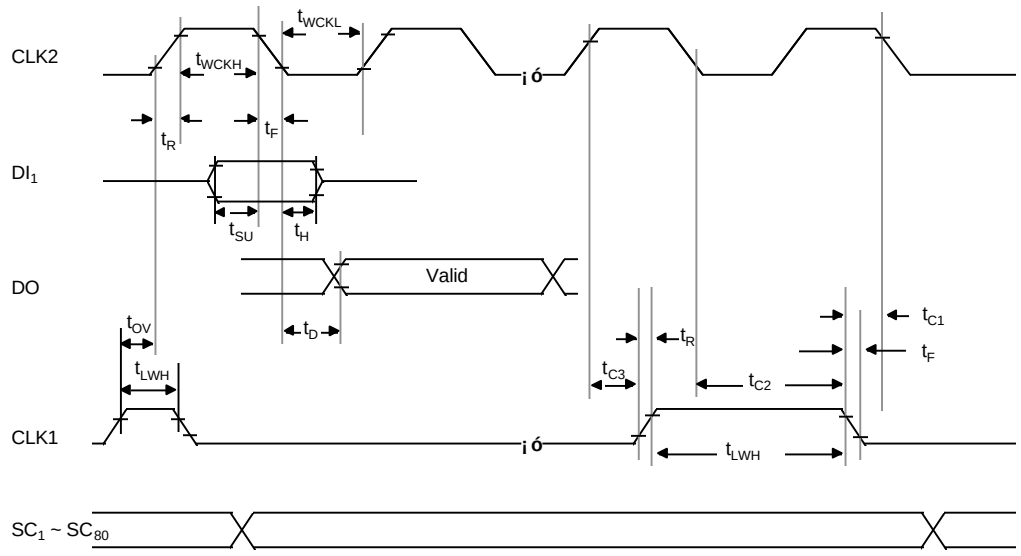



Fig. 3 Segment driver ( 1 bit serial input )

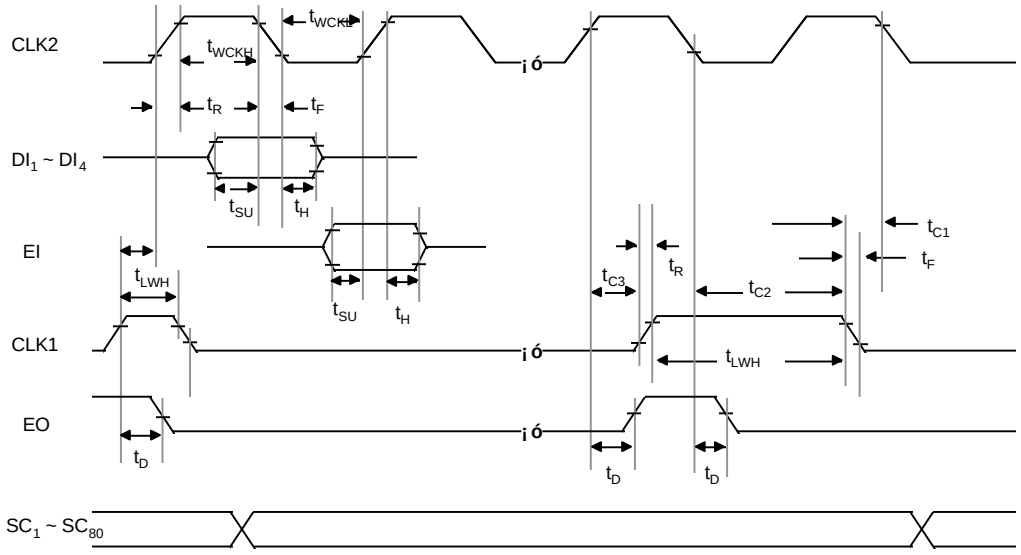



Fig. 4. 4 - bit input segment driver
Fig . 4. Segment driver (4 bit input)

**TIMING CHARACTERISTICS** (continued)

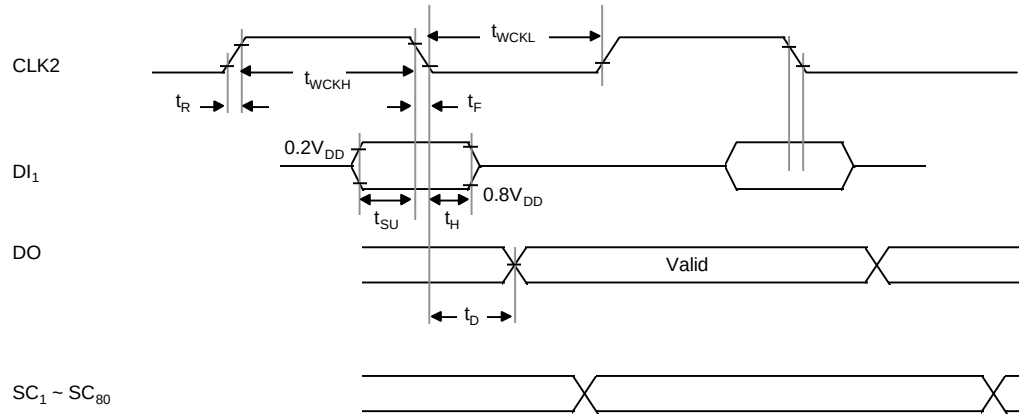



Fig. 5. Common driver

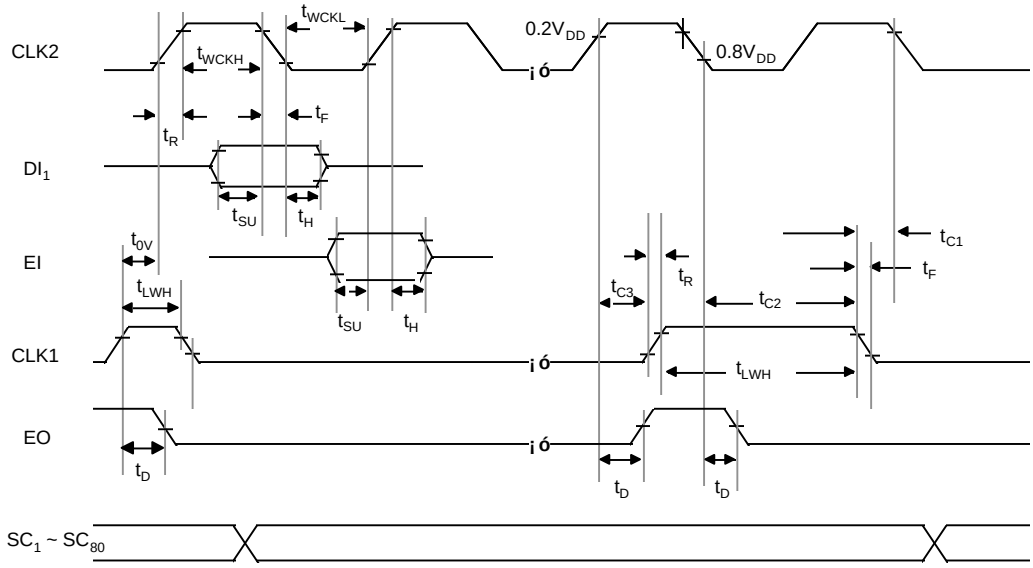
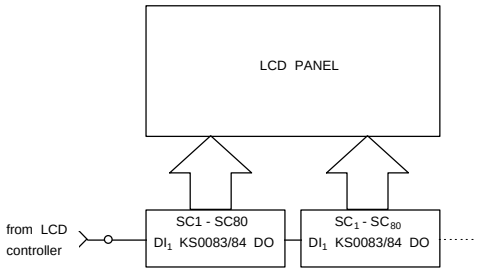



Fig. 6. Segment driver ( 1 bit serial data input )

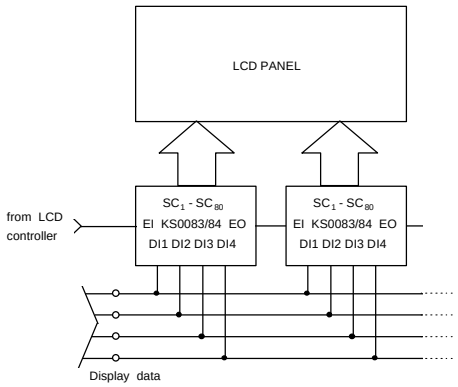
## APPLICATION CIRCUIT

**Mode Select**

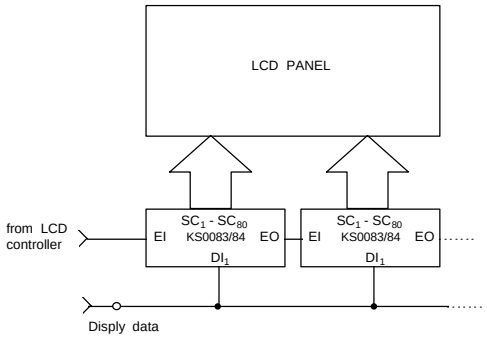
1. segment driver 1;1 bit serial data input (FCS=L, PS=L)



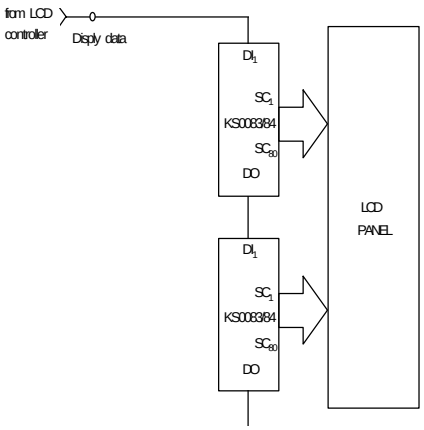

2. segment driver;4 bit serial data input (FCS=L, PS=H)

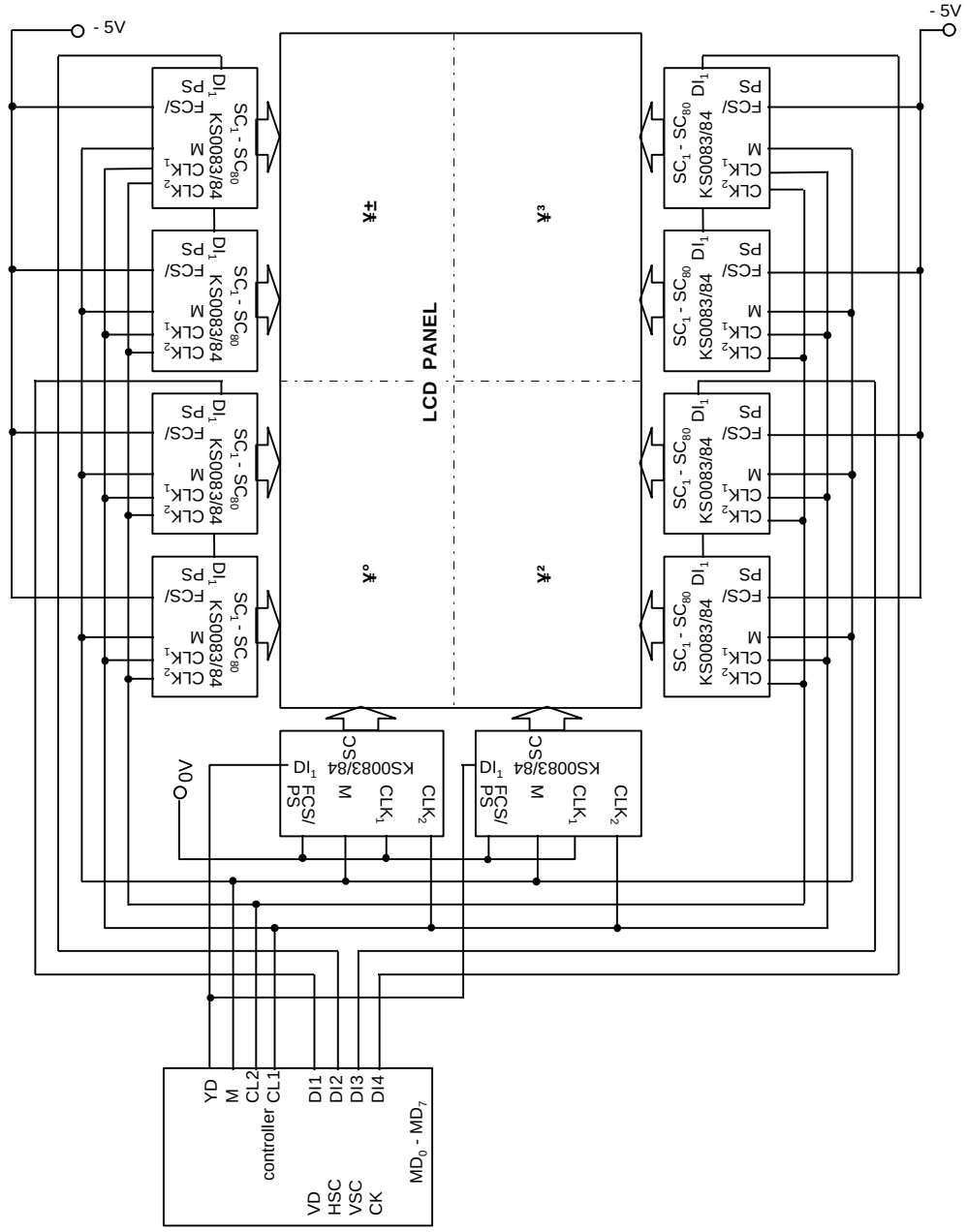



3. segment driver 2;1 bit serial data input (FCS=H, PS=L)



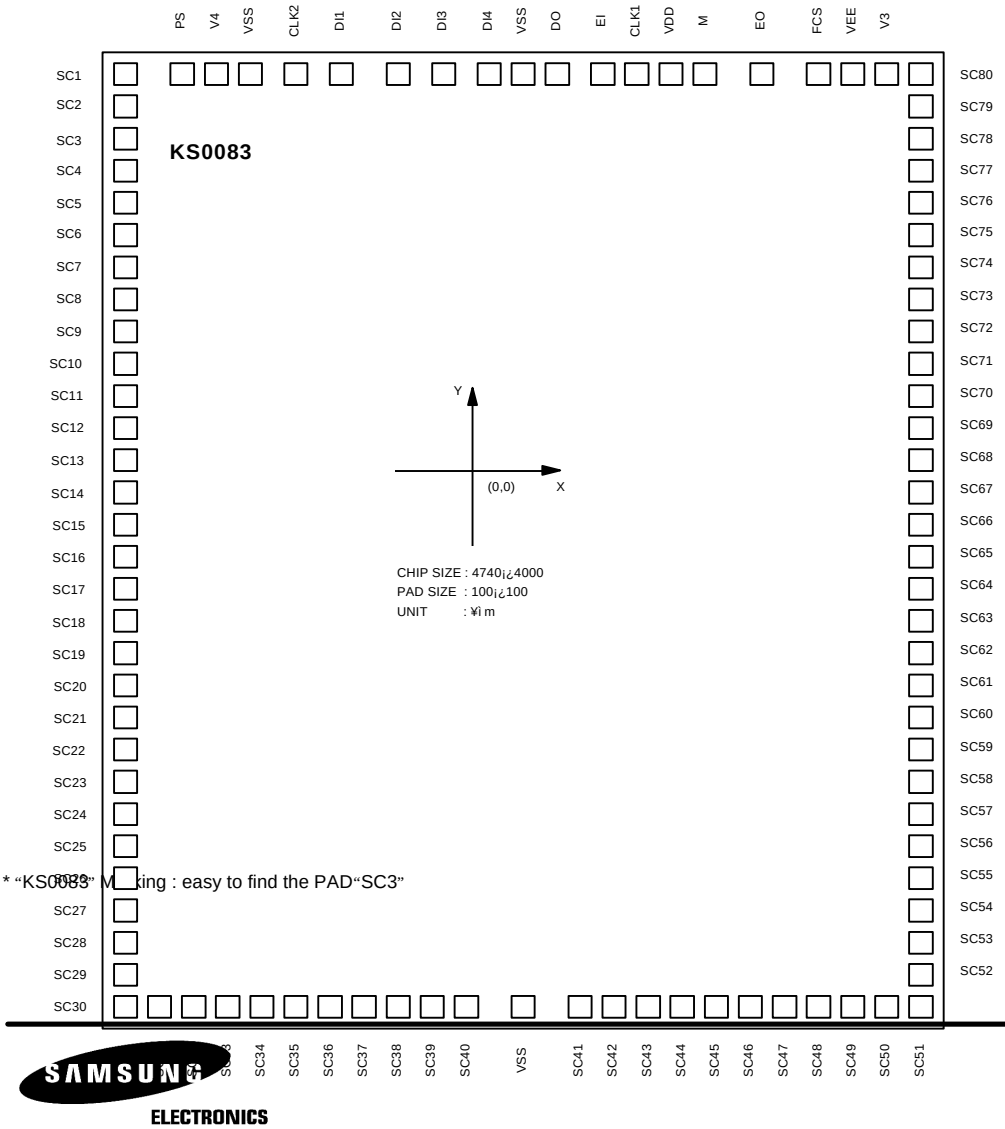

4. common driver (FCS=H, PS=H)




- 5V
- 5V
LCD PANEL
KS0083/84
SC1 - SC80
DI1
FCS/PS
M
CLK1
CLK2
0V
YD
M
CL2
CL1
DI1
DI2
DI3
DI4
controller
VD
HSC
VSC
CK
MD0 - MD7

## APPLICATION CIRCUIT

## PAD DIAGRAM

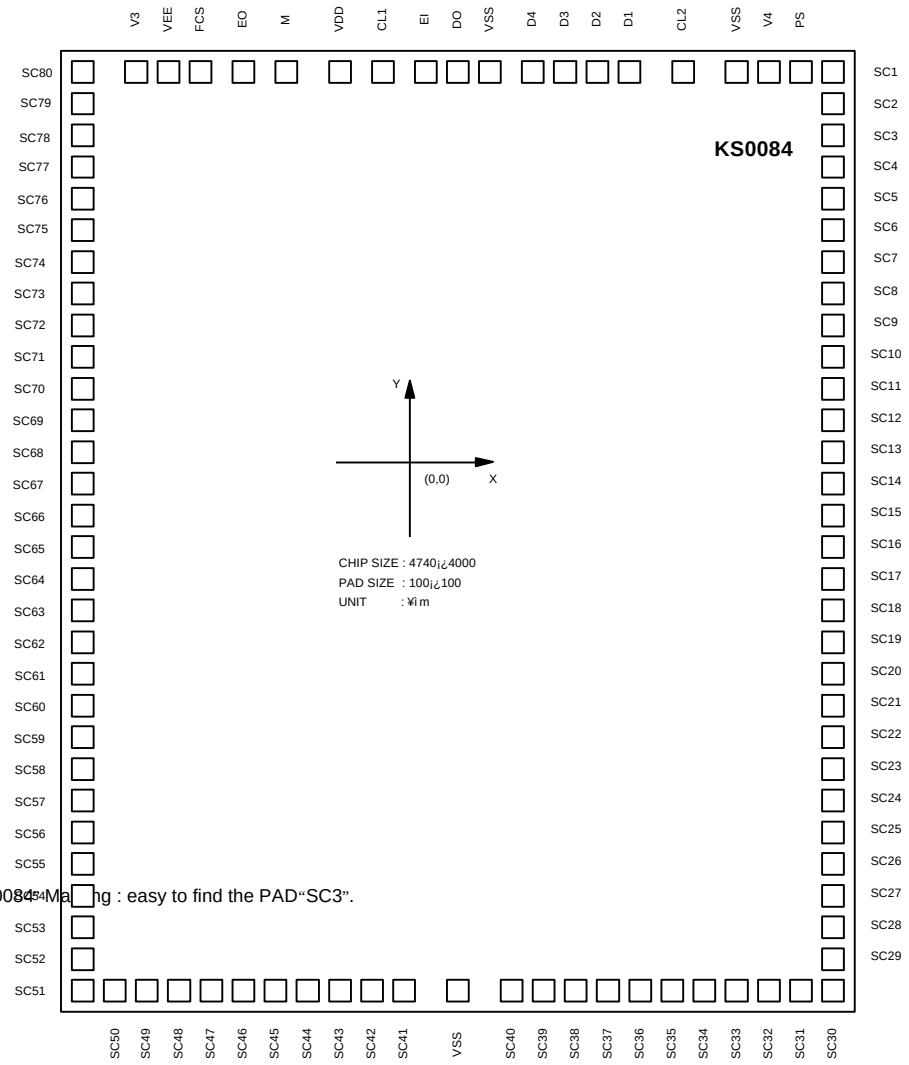



* "KS0083" Marking : easy to find the PAD"SC3"

## PAD LOCATION

| PAD NUMBER | PAD NAME | COORDINATE | | PAD NUMBER | PAD NAME | COORDINATE | | PAD NUMBER | PAD NAME | COORDINATE | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | X | Y | | | X | Y | | | X | Y |
| 1 | SC2 | -1880 | 2095 | 35 | SC36 | -950 | -2250 | 69 | SC69 | 1880 | 540 |
| 2 | SC3 | -1880 | 1940 | 36 | SC37 | -795 | -2250 | 70 | SC70 | 1880 | 695 |
| 3 | SC4 | -1880 | 1785 | 37 | SC38 | -640 | -2250 | 71 | SC71 | 1880 | 850 |
| 4 | SC5 | -1880 | 1625 | 38 | SC39 | -485 | -2250 | 72 | SC72 | 1880 | 1005 |
| 5 | SC6 | -1880 | 1470 | 39 | SC40 | -330 | -2250 | 73 | SC73 | 1880 | 1160 |
| 6 | SC7 | -1880 | 1315 | 40 | VSS | 15 | -2250 | 74 | SC74 | 1880 | 1315 |
| 7 | SC8 | -1880 | 1160 | 41 | SC41 | 330 | -2250 | 75 | SC75 | 1880 | 1470 |
| 8 | SC9 | -1880 | 1005 | 42 | SC42 | 485 | -2250 | 76 | SC76 | 1880 | 1625 |
| 9 | SC10 | -1880 | 850 | 43 | SC43 | 640 | -2250 | 77 | SC77 | 1880 | 1785 |
| 10 | SC11 | -1880 | 695 | 44 | SC44 | 795 | -2250 | 78 | SC78 | 1880 | 1940 |
| 11 | SC12 | -1880 | 540 | 45 | SC45 | 950 | -2250 | 79 | SC79 | 1880 | 2095 |
| 12 | SC13 | -1880 | 385 | 46 | SC46 | 1105 | -2250 | 80 | SC80 | 1880 | 2250 |
| 13 | SC14 | -1880 | 230 | 47 | SC47 | 1260 | -2250 | 81 | V3 | 1725 | 2250 |
| 14 | SC15 | -1880 | 75 | 48 | SC48 | 1415 | -2250 | 82 | VEE | 1570 | 2250 |
| 15 | SC16 | -1880 | -80 | 49 | SC49 | 1570 | -2250 | 83 | FCS | 1389 | 2250 |
| 16 | SC17 | -1880 | 235 | 50 | SC50 | 1725 | -2250 | 84 | EO | 1140 | 2250 |
| 17 | SC18 | -1880 | -390 | 51 | SC51 | 1880 | -2250 | 85 | M | 909 | 2250 |
| 18 | SC19 | -1880 | -545 | 52 | SC52 | 1880 | -2095 | 86 | VDD | 718 | 2250 |
| 19 | SC20 | -1880 | -700 | 53 | SC53 | 1880 | -1940 | 87 | CLK1 | 527 | 2250 |
| 20 | SC21 | -1880 | -855 | 54 | SC54 | 1880 | -1785 | 88 | EI | 337 | 2250 |
| 21 | SC22 | -1880 | -1010 | 55 | SC55 | 1880 | -1630 | 89 | DO | 88 | 2250 |
| 22 | SC23 | -1880 | -1165 | 56 | SC56 | 1880 | -1475 | 90 | VSS | -111 | 2250 |
| 23 | SC24 | -1880 | -1320 | 57 | SC57 | 1880 | -1320 | 91 | DI4 | -283 | 2250 |
| 24 | SC25 | -1880 | -1475 | 58 | SC58 | 1880 | -1165 | 92 | DI3 | -511 | 2250 |
| 25 | SC26 | -1880 | -1630 | 59 | SC59 | 1880 | -1010 | 93 | DI2 | -701 | 2250 |
| 26 | SC27 | -1880 | -1785 | 60 | SC60 | 1880 | -855 | 94 | DI1 | -929 | 2250 |
| 27 | SC28 | -1880 | -1940 | 61 | SC61 | 1880 | -700 | 96 | CLK2 | -1119 | 2250 |
| 28 | SC29 | -1880 | -2095 | 62 | SC62 | 1880 | -545 | 97 | VSS | -1319 | 2250 |
| 29 | SC30 | -1880 | -2250 | 63 | SC63 | 1880 | -390 | 98 | V4 | -1474 | 2250 |
| 30 | SC31 | -1725 | -2250 | 64 | SC64 | 1880 | -235 | 99 | PS | -1655 | 2250 |
| 31 | SC32 | -1570 | -2250 | 65 | SC65 | 1880 | -80 | 100 | SC1 | -1880 | 2250 |
| 32 | SC33 | -1415 | -2250 | 66 | SC66 | 1880 | 75 | | | | |
| 33 | SC34 | -1260 | -2250 | 67 | SC67 | 1880 | 230 | | | | |
| 34 | SC35 | -1105 | -2250 | 68 | SC68 | 1880 | 385 | | | | |

## PAD DIAGRAM




* "KS0084-Ma ng : easy to find the PAD"SC3".

## PAD LOCATION

| PAD NUMBER | PAD NAME | COORDINATE | | PAD NUMBER | PAD NAME | COORDINATE | | PAD NUMBER | PAD NAME | COORDINATE | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | X | Y | | | X | Y | | | X | Y |
| 1 | SC80 | -1880 | 2250 | SC46 | | 35 | -2250 | 69 | SC13 | 1880 | 385 |
| 2 | SC79 | -1880 | 2095 | SC45 | -1105 | 36 | -2250 | 70 | SC12 | 1880 | 540 |
| 3 | SC78 | -1880 | 1940 | SC44 | -950 | 37 | -2250 | 71 | SC11 | 1880 | 695 |
| 4 | SC77 | -1880 | 1785 | SC43 | -795 | 38 | -2250 | 72 | SC10 | 1880 | 850 |
| 5 | SC76 | -1880 | 1625 | SC42 | -640 | 39 | -2250 | 73 | SC9 | 1880 | 1005 |
| 6 | SC75 | -1880 | 1470 | SC41 | -485 | 40 | -2250 | 74 | SC8 | 1880 | 1160 |
| 7 | SC74 | -1880 | 1315 | VSS | -330 | 41 | -2250 | 75 | SC7 | 1880 | 1315 |
| 8 | SC73 | -1880 | 1160 | SC40 | -15 | 42 | -2250 | 76 | SC6 | 1880 | 1470 |
| 9 | SC72 | -1880 | 1005 | SC39 | 330 | 43 | -2250 | 77 | SC5 | 1880 | 1625 |
| 10 | SC71 | -1880 | 850 | SC38 | 485 | 44 | -2250 | 78 | SC4 | 1880 | 1785 |
| 11 | SC70 | -1880 | 695 | SC37 | 640 | 45 | -2250 | 79 | SC3 | 1880 | 1940 |
| 12 | SC69 | -1880 | 540 | SC36 | 795 | 46 | -2250 | 80 | SC2 | 1880 | 2095 |
| 13 | SC68 | -1880 | 385 | SC35 | 950 | 47 | -2250 | 81 | SC1 | 1870 | 2250 |
| 14 | SC67 | -1880 | 230 | SC34 | 1105 | 48 | -2250 | 82 | PS | 1655 | 2250 |
| 15 | SC66 | -1880 | 75 | SC33 | 1260 | 49 | -2250 | 83 | V4 | 1474 | 2250 |
| 16 | SC65 | -1880 | -80 | SC32 | 1415 | 50 | -2250 | 84 | VSS | 1319 | 2250 |
| 17 | SC64 | -1880 | -235 | SC31 | 1570 | 51 | -2250 | 85 | CL2 | 1119 | 2250 |
| 18 | SC63 | -1880 | -390 | SC30 | 1725 | 52 | -2250 | 87 | D1 | 929 | 2250 |
| 19 | SC62 | -1880 | -545 | SC29 | 1880 | 53 | -2095 | 88 | D2 | 701 | 2250 |
| 20 | SC61 | -1880 | -700 | SC28 | 1880 | 54 | -1940 | 89 | D3 | 511 | 2250 |
| 21 | SC60 | -1880 | -855 | SC27 | 1880 | 55 | -1785 | 90 | D4 | 283 | 2250 |
| 22 | SC59 | -1880 | -1010 | SC26 | 1880 | 56 | -1630 | 91 | VSS | 111 | 2250 |
| 23 | SC58 | -1880 | -1165 | SC25 | 1880 | 57 | -1475 | 92 | DO | -88 | 2250 |
| 24 | SC57 | -1880 | -1320 | SC24 | 1880 | 58 | -1320 | 93 | EI | -337 | 2250 |
| 25 | SC56 | -1880 | -1475 | SC23 | 1880 | 59 | -1165 | 94 | CL1 | -527 | 2250 |
| 26 | SC55 | -1880 | -1630 | SC22 | 1880 | 60 | -1010 | 95 | VDD | -718 | 2250 |
| 27 | SC54 | -1880 | -1785 | SC21 | 1880 | 61 | -855 | 96 | M | -909 | 2250 |
| 28 | SC53 | -1880 | -1940 | SC20 | 1880 | 62 | -700 | 97 | EO | -1140 | 2250 |
| 29 | SC52 | -1880 | -2095 | SC19 | 1880 | 63 | -545 | 98 | FCS | -1389 | 2250 |
| 30 | SC51 | -1880 | -2250 | SC18 | 1880 | 64 | -390 | 99 | VEE | -1570 | 2250 |
| 31 | SC50 | -1725 | -2250 | SC17 | 1880 | 65 | -235 | 100 | V3 | -1725 | 2250 |
| 32 | SC49 | -1570 | -2250 | SC16 | 1880 | 66 | -80 | | | | |
| 33 | SC48 | -1415 | -2250 | SC15 | 1880 | 67 | 75 | | | | |
| 34 | SC47 | -1260 | -2250 | SC14 | 1880 | 68 | 230 | | | | |
| | | | | SC67 | 1880 | | 385 | | | | |
| | | | | SC68 | 1880 | | | | | | |