INTRODUCTION

The KS0090 is an LCD driver and controller LSI for liquid crystal dot matrix character display systems. It can display 2 or 3 lines of 12 characters with the 5 × 8 dots format. It is capable of interfacing with various microprocessors, supporting the 4-bit and 8-bit parallel modes as well as the clock synchronized serial mode. Voltage converter (2 or 3 times), voltage regulator, divider resistor and voltage follower OP AMP are built-in to the IC, and a low operation current of 50μA is achieved. The slim shape of the chip makes it suitable for the COG module application and TCP. The KS0090 is an ideal solution for display on portable equipment such as hand-held phones.

FEATURES

- **Driver Outputs**
  - — Common output: 26 common
  - — Segment output: 64 segment
  - — Icons: 128 horizontal icons, 24 × 4 vertical icons, 5 static icons
- **Applicable Panel Size**

Display Size	Duty	Output Content
2 line × 12 char	1/18	(12 characters + 4 segments for signal) × 2 + 128 icons + 5 static icons
3 line × 12 char	1/26	(12 characters + 4 segments for signal) × 3 + 128 icons + 5 static icons

- **Internal Memory**
  - — Character generator ROM (CGROM): 10,240 bits (256 characters × 5 × 8 dots)
  - — Character generator RAM (CGRAM): 160 bits (4 characters × 5 × 8 dots)
  - — Display data RAM (DDRAM): 288 bits (12 characters × 3 lines × 8 bits)
  - — Segment icon RAM (ICONRAM): 224 bits (12 × 2 × 5 bits + 2 × 4 bits + 24 × 4 bits)
- **MPU Interface**
  - — No busy MPU interface (No busy check or no execution waiting time)
  - — 8-bit parallel interface mode: 68-series and 80-series are available
  - — 4-bit parallel interface mode: 68-series and 80-series are available
  - — Serial interface mode: 4 pin clock synchronized serial interface
- **Function Set**
  - — Various instruction set: display control, power save, power control, function set... etc.
  - — COM/SEG bidirectional function (4 type LCD application available)
  - — Hardware reset (RES pin)
- **Built-in Analog Circuit**
  - — On-chip oscillator with an Internal resistor or external clock input
  - — Electronic volume for contrast control (32 or 64 steps)
  - — Voltage converter (2 or 3 times) / voltage regulator / voltage follower and bias circuit

- **Low Power Consumption**
  - 80 μA Max.: In normal mode for normal display operation
  - 10 μA Max.: In standby mode for displaying static icon
  - 5 μA Max.: In sleep mode when display is turned off
- **Operating Voltage Range**
  - Power supply voltage (V_{DD}): 2.4 to 5.5 V
  - LCD driving voltage (VLCD = V0 – V_{SS}): 11.0 V (positive process)
- **Package Type**
  - Bumped chip or TCP available

BLOCK DIAGRAM

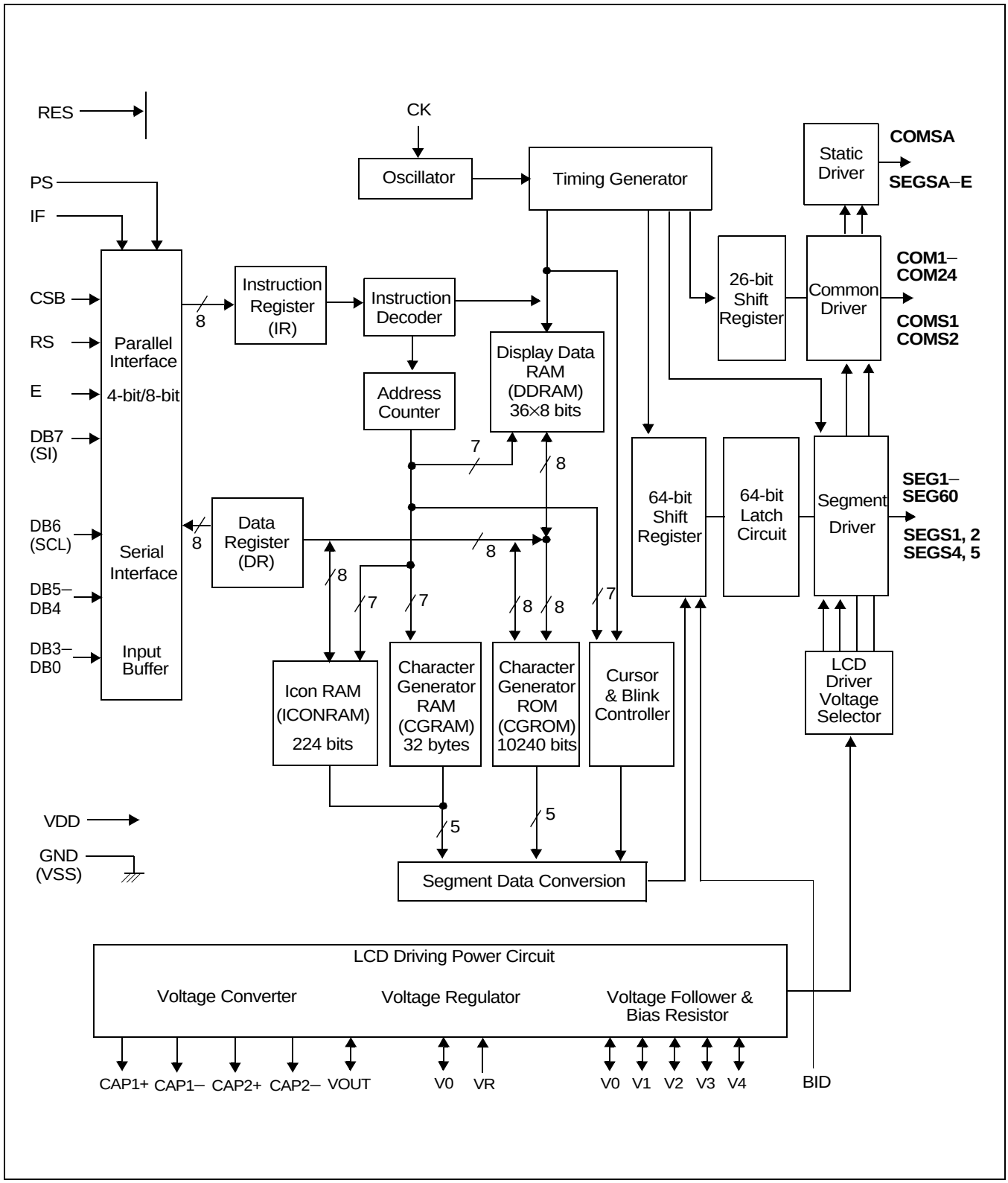
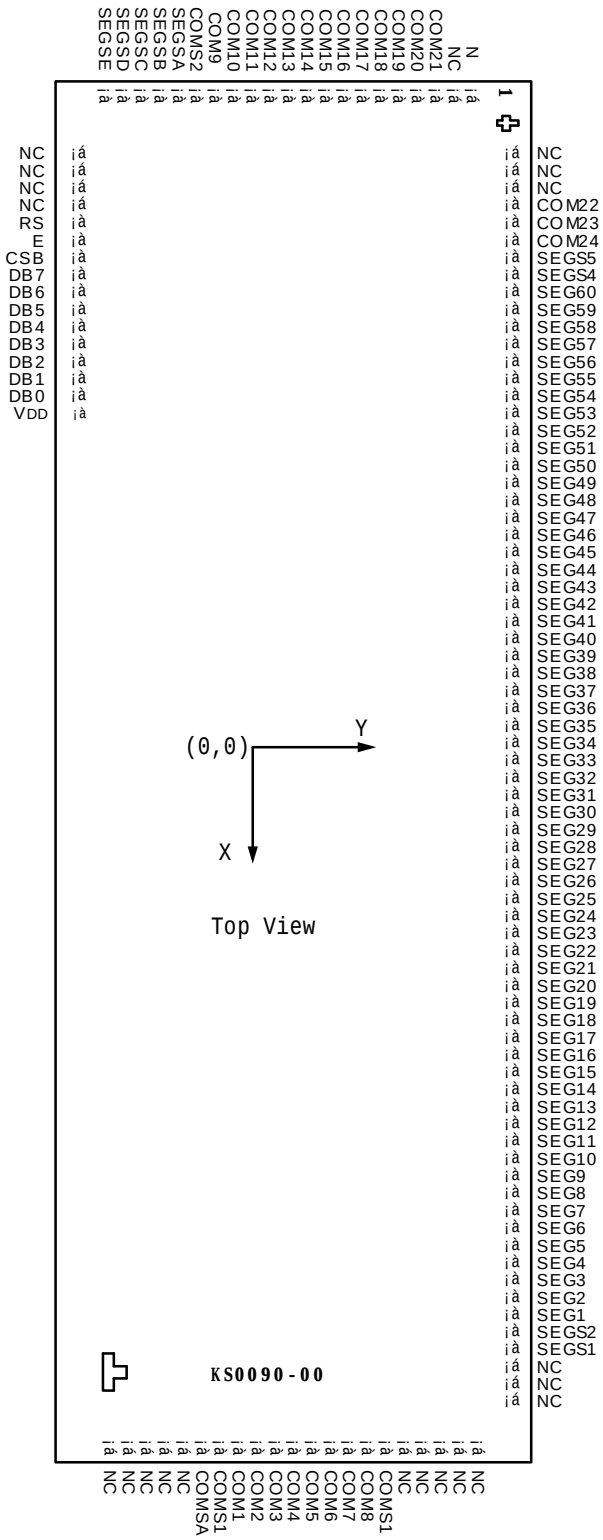


Figure 1. KS0090 Block Diagram

PAD CONFIGURATION



Chip Size: 7410 μm × 2470 μm
Pad Pitch: 90 μm

Al Pad Size: 60 μm × 118 μm

Au Bump Size: 56 μm × 114 μm
Height:17 μm ± 1.5 μm

Align Key Size:

- Left-Top(Cross)
  80 μm × 80μm (Width 40 μm)

- Right-Bottom(T)
  120 μm × 120 μm (Width 40 μm)

PAD LOCATION

[UNIT: ㎜]

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
1	NC1	–3540	880	31	DB5	–2430	–1111	61	CAP2–	270	–1111
2	NC2	–3540	790	32	DB4	–2340	–1111	62	CAP2–	360	–1111
3	COM21	–3540	700	33	DB3	–2250	–1111	63	CAP2–	450	–1111
4	COM20	–3540	610	34	DB2	–2160	–1111	64	CAP2–	540	–1111
5	COM19	–3540	520	35	DB1	–2070	–1111	65	CAP2+	630	–1111
6	COM18	–3540	430	36	DB0	–1980	–1111	66	CAP2+	720	–1111
7	COM17	–3540	340	37	VDD	–1890	–1111	67	CAP2+	810	–1111
8	COM16	–3540	250	38	VDD	–1800	–1111	68	CAP2+	900	–1111
9	COM15	–3540	160	39	VDD	–1710	–1111	69	CAP1–	990	–1111
10	COM14	–3540	70	40	VSS	–1620	–1111	70	CAP1–	1080	–1111
11	COM13	–3540	–20	41	VSS	–1530	–1111	71	CAP1–	1170	–1111
12	COM12	–3540	–110	42	VSS	–1440	–1111	72	CAP1–	1260	–1111
13	COM11	–3540	–200	43	V4	–1350	–1111	73	CAP1+	1350	–1111
14	COM10	–3540	–290	44	V4	–1260	–1111	74	CAP1+	1440	–1111
15	COM9	–3540	–380	45	V3	–1170	–1111	75	CAP1+	1530	–1111
16	COMS2	–3540	–470	46	V3	–1080	–1111	76	CAP1+	1620	–1111
17	SEGSA	–3540	–560	47	V2	–990	–1111	77	VSS	1710	–1111
18	SEGSB	–3540	–650	48	V2	–900	–1111	78	VSS	1800	–1111
19	SEGSC	–3540	–740	49	V1	–810	–1111	79	VSS	1890	–1111
20	SEGSD	–3540	–830	50	V1	–720	–1111	80	BID	1980	–1111
21	SEGSE	–3540	–920	51	V0	–630	–1111	81	VDD	2070	–1111
22	NC3	–3240	–1111	52	V0	–540	–1111	82	VDD	2160	–1111
23	NC4	–3150	–1111	53	V0	–450	–1111	83	VDD	2250	–1111
24	NC5	–3060	–1111	54	V0	–360	–1111	84	CK	2340	–1111
25	NC6	–2970	–1111	55	VR	–270	–1111	85	VDD	2430	–1111
26	RS	–2880	–1111	56	VR	–180	–1111	86	PS	2520	–1111
27	E	–2790	–1111	57	VOUT	–90	–1111	87	IF	2610	–1111
28	CSB	–2700	–1111	58	VOUT	0	–1111	88	RES	2700	–1111
29	DB7	–2610	–1111	59	VOUT	90	–1111	89	VDD	2790	–1111
30	DB6	–2520	–1111	60	VOUT	180	–1111	90	VDD	2880	–1111

[UNIT: ㎜]

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
91	NC7	2970	–1111	124	SEG4	2520	1070	157	SEG37	–450	1070
92	NC8	3060	–1111	125	SEG5	2430	1070	158	SEG38	–540	1070
93	NC9	3150	–1111	126	SEG6	2340	1070	159	SEG39	–630	1070
94	NC10	3240	–1111	127	SEG7	2250	1070	160	SEG40	–720	1070
95	NC11	3540	–920	128	SEG8	2160	1070	161	SEG41	–810	1070
96	NC12	3540	–830	129	SEG9	2070	1070	162	SEG42	–900	1070
97	NC13	3540	–740	130	SEG10	1980	1070	163	SEG43	–990	1070
98	NC14	3540	–650	131	SEG11	1890	1070	164	SEG44	–1080	1070
99	NC15	3540	–560	132	SEG12	1800	1070	165	SEG45	–1170	1070
100	COMSA	3540	–470	133	SEG13	1710	1070	166	SEG46	–1260	1070
101	COMS1	3540	–380	134	SEG14	1620	1070	167	SEG47	–1350	1070
102	COM1	3540	–290	135	SEG15	1530	1070	168	SEG48	–1440	1070
103	COM2	3540	–200	136	SEG16	1440	1070	169	SEG49	–1530	1070
104	COM3	3540	–110	137	SEG17	1350	1070	170	SEG50	–1620	1070
105	COM4	3540	–20	138	SEG18	1260	1070	171	SEG51	–1710	1070
106	COM5	3540	70	139	SEG19	1170	1070	172	SEG52	–1800	1070
107	COM6	3540	160	140	SEG20	1080	1070	173	SEG53	–1890	1070
108	COM7	3540	250	141	SEG21	990	1070	174	SEG54	–1980	1070
109	COM8	3540	340	142	SEG22	900	1070	175	SEG55	–2070	1070
110	COMS1*	3540	430	143	SEG23	810	1070	176	SEG56	–2160	1070
111	NC16	3540	520	144	SEG24	720	1070	177	SEG57	–2250	1070
112	NC17	3540	610	145	SEG25	630	1070	178	SEG58	–2340	1070
113	NC18	3540	700	146	SEG26	540	1070	179	SEG59	–2430	1070
114	NC19	3540	790	147	SEG27	450	1070	180	SEG60	–2520	1070
115	NC20	3540	880	148	SEG28	360	1070	181	SEGS4	–2610	1070
116	NC21	3240	1070	149	SEG29	270	1070	182	SEGS5	–2700	1070
117	NC22	3150	1070	150	SEG30	180	1070	183	COM24	–2790	1070
118	NC23	3060	1070	151	SEG31	90	1070	184	COM23	–2880	1070
119	SEGS1	2970	1070	152	SEG32	0	1070	185	COM22	–2970	1070
120	SEGS2	2880	1070	153	SEG33	–90	1070	186	NC24	–3060	1070
121	SEG1	2790	1070	154	SEG34	–180	1070	187	NC25	–3150	1070
122	SEG2	2700	1070	155	SEG35	–270	1070	188	NC26	–3240	1070
123	SEG3	2610	1070	156	SEG36	–360	1070				

NOTE: The COMS1 has two terminals (#101, #110), and these two COMS1 are the same signal at the same time.

PIN DESCRIPTION

Table 1. Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">Power Supply</td></tr>
<tr><td>VDD</td><td rowspan="2">Power</td><td>Power supply. Connect to MPU power supply pin.</td></tr>
<tr><td>VSS</td><td>0 V (GND)</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>I/O</td><td>Bias voltage level for LCD driving.
Voltages have the following relationship;
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS
When the built-in power circuit is on, the following voltages are given to pin V1 to V4 using internal 1/5 bias resistors.
<table>
<tr><th>LCD Bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>(1/5) Bias</td><td>(4/5) V0</td><td>(3/5) V0</td><td>(2/5) V0</td><td>(1/5) V0</td></tr>
</table>
</td></tr>
<tr><td colspan="3">LCD Driver Supply</td></tr>
<tr><td>CAP1+</td><td rowspan="4">O</td><td>Capacitor1+ connecting pin for the internal voltage converter.
This pin connects the capacitor with CAP1–.</td></tr>
<tr><td>CAP1–</td><td>Capacitor1– connecting pin for the internal voltage converter.
This pin connects the capacitor with CAP+.</td></tr>
<tr><td>CAP2+</td><td>Capacitor2+ connecting pin for the internal voltage converter.
When VOUT is 2 times boosting, this pin connects the capacitor with V_{DD}.
When 3 times boosting, this pin connects the capacitor with CAP2–.</td></tr>
<tr><td>CAP2–</td><td>Capacitor2– connecting pin for the internal voltage converter.
When VOUT is 2 times boosting, this pin is not used.
When 3 times boosting, this pin connects the capacitor with CAP2+.</td></tr>
<tr><td>VOUT</td><td>I/O</td><td>2 or 3 times DC/DC voltage converter output.
This pin connects a capacitor with V_{DD} pin.</td></tr>
<tr><td>VR</td><td>I</td><td>Voltage adjust pin. This pin gives a voltage between V0 and Vss by resistance-division of voltage.</td></tr>
</table>

Table 1. Pin Description (Continued)

Name	I/O	Description
System Control		
CK	I	External clock input pin. It must be fixed to “High” when the internal oscillation circuit is used. In the external clock mode, it is used as an external clock input pin.
PS	I	Parallel/Serial selection pin When PS = “Low”: serial mode When PS = “High”: 4-bit/8-bit bus mode
IF	I	Interface data length selection pin for parallel data input. When PS = “Low” IF = “Low” or “High”: serial interface mode When PS = “High” IF = “Low”: 4-bit bus mode IF = “High”: 8-bit bus mode
BID	I	SEG direction selection pin When BID = “Low”, SEGS1 → SEGS2 → SEG1 → …… → SEG60 → SEGS4 → SEGS5 When BID = “High”, SEGS5 → SEGS4 → SEG60 → …… → SEG1 → SEGS2 → SEGS1
MPU Interface		
RES	I	Initialization is performed by edge sensing of the RES signal. An interface type for the 60 / 80 series MPU is selected by input level after initialization. When RES = “Low”: 68 series MPU. When RES = “High”: 80 series MPU.
CSB	I	Chip selection pin. When CSB = “Low”: Selected. When CSB = “High”: Not selected.
RS	I	Register selection pin. When RS = “Low”: Instruction register. When RS = “High”: Data register.
E	I	In 80 series MPU interface mode, active “Low”. This pin connects the $\overline{WR}$ pin of the 80 series MPU. The signal on the data bus is fetched at the rise of the $\overline{WR}$ signal. In 68-series MPU interface mode, active “high”. This pin becomes as enable clock input of the 68-series MPU.
DB0 – DB3 DB4 – DB5 DB6 (SCL) DB7 (SI)	I	When in 8-bit interface mode, DB0 to DB7 are used as input data bus pin. In the 4-bit bus mode, only DB4 to DB7 are used as data input pin and DB0 to DB3 are not used. In the serial mode, DB6 (SCL) is used as a serial clock input pin, DB7(SI) is used as a serial data input pin and the others are not used.

Table 1. Pin Description (Continued)

Name	I/O	Description
LCD Driver Outputs (Dynamic)		
COM1 to COM24	O	Common signal output for character display.
COMS1, COMS2	O	Common signal output for icon display. The COMS1 has two terminals, and these two COMS1 are the same signal at the same time.
SEG1 to SEG60	O	Segment signal output for character display.
SEGS1, SEGS2 SEGS4, SEGS5	O	Segment signal output for vertical icon display
LCD Driver Outputs (Static)		
COMSA	O	Static common signal output for static icon display.
SEGSA, B, C, D, E	O	Static segment signal output for static icon display.

FUNCTION DESCRIPTION

SYSTEM INTERFACE

KS0090 has two kinds of interface type with MPU: bus mode and serial mode. Bus mode or serial mode is selected by the PS pin. In bus mode, 4-bit bus or 8-bit bus is selected by the IF pin, and 68 series MPU or 80 series MPU is selected by the RES pin.

Table 2. Various Kinds of MPU Interface According to PS, RES and IF

PS	RES	IF	CSB	RS	E	DB0–3	DB4–5	DB6	DB7
Bus Mode (H)	80 series (H)	8-bit (H)	CSB	RS	$\overline{WR}$	DB0 to 3	DB4 to 5	DB6	DB7
		4-bit (L)	CSB	RS	$\overline{WR}$	–	DB4 to 5	DB6	DB7
	68 series (L)	8-bit (H)	CSB	RS	E	DB0 to 3	DB4 to 5	DB6	DB7
		4-bit (L)	CSB	RS	E	–	DB4 to 5	DB6	DB7
Serial Mode (L)	(H)/(L)	(H)/(L)	CSB	RS	(H)/(L)	–	–	SCL	SI

NOTES:

1. "–": Don't care ("High", "Low" or "Open"),
2. (H)/(L): Fixed "High" (V_{DD}) or "Low" (V_{SS})

PS: "High" = Bus mode, "Low" = Serial mode
RES: "High" = 80 Series MPU, "Low" = 68 Series MPU
IF: "High" = 8-bit mode, "Low" = 4-bit mode (PS: "High")
CSB: "High" = Chip is not selected, "Low" = Chip is selected
RS: "High" = Data register, "Low" = Instruction register
E: 80 series active "Low", 68 series active "High"
SCL (DB6): Serial clock input
SI (DB7): Serial data input

Interface with MPU in Parallel Mode (PS = “High”)

During writing operation, two 8-bit registers, data register (DR) and instruction register (IR), are used. The data register (DR) is used as temporary data storage place to be written into DDRAM/CGRAM/ICONRAM, and one of these RAMs is selected by the RAM address setting instruction. The Instruction register (IR) is used only to store instruction code transferred from MPU. To select DR or IR register, RS input pin is used in bus mode or serial mode. In 4-bit bus mode, the RS input pin is needed to transfer 4-bit data (DB4 to DB7) two times. The high order bits (for 8-bit mode DB4 to DB7) are transferred before the low order bits (for 8-bit mode DB0 to DB3). The DB0 to DB3 pins are floated in this 4-bit bus mode. After RES resets, KS0090 considers first 4-bit data from MPU as the high order bits.

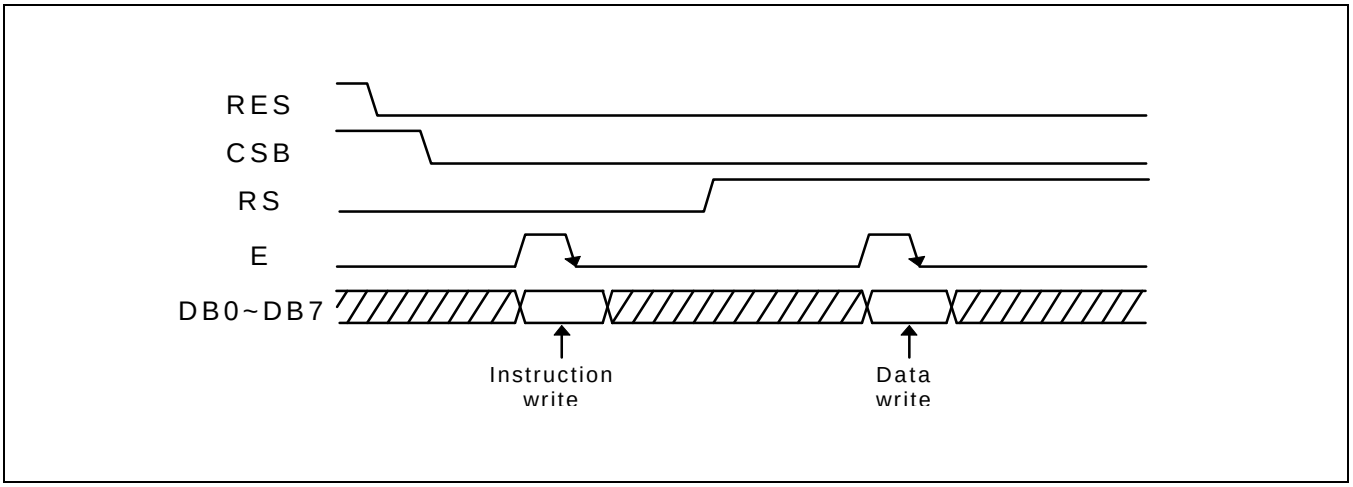


Figure 2. 8-bit Parallel Bus Mode (68 series MPU Mode)

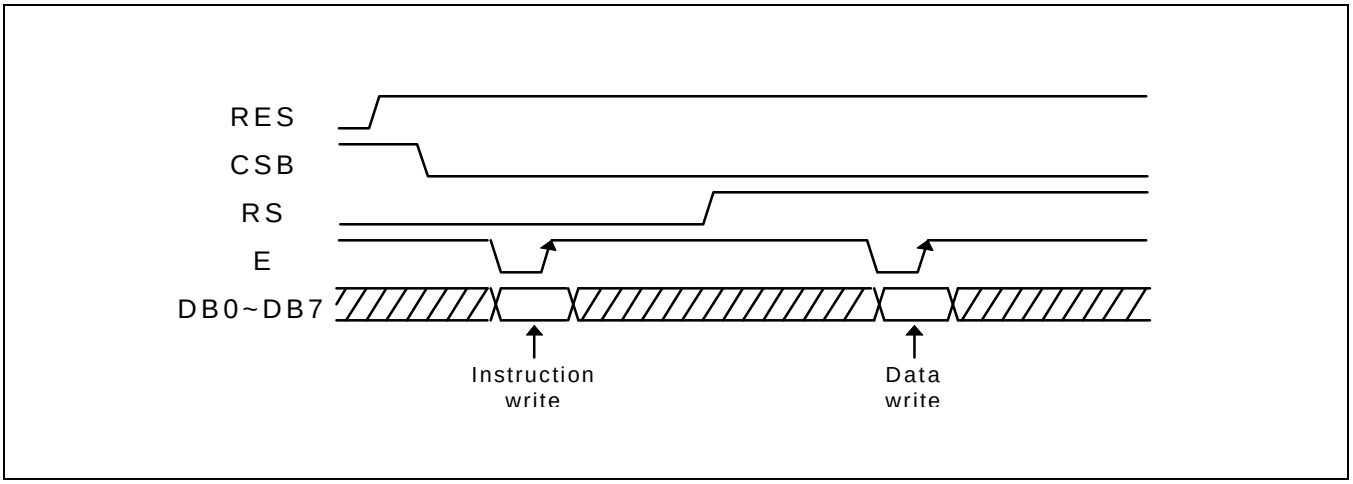


Figure 3. 8-bit Parallel Bus Mode (80 series MPU Mode)

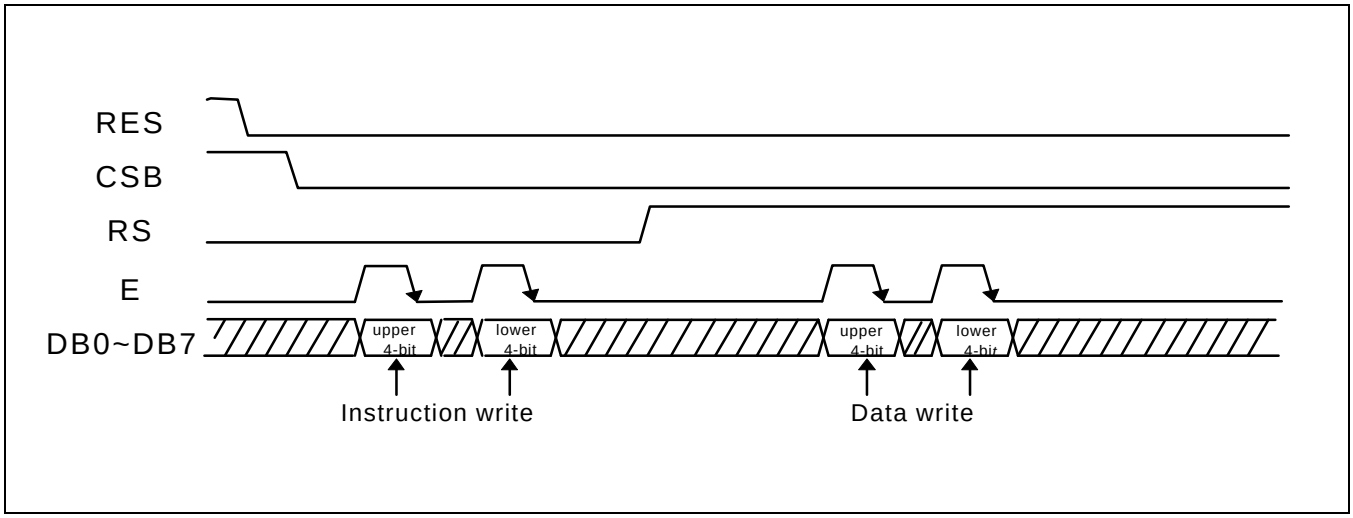


Figure 4. 4-bit Parallel Bus Mode (68 series MPU Mode)

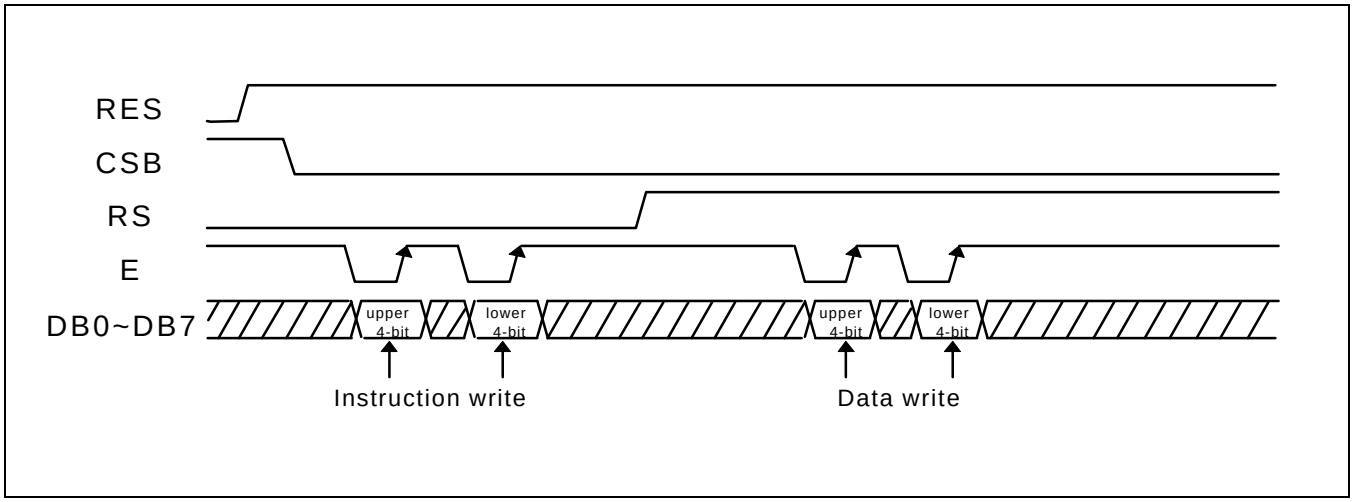


Figure 5. 4-bit Parallel Bus Mode (80 series MPU Mode)

Interface with MPU in Serial Mode (PS = “Low”)

When PS input pin is “Low”, clock synchronized serial interface mode is selected. At this time, four ports, SCL (DB6, synchronizing transfer clock), SI (DB7, serial input data), RS (register selection input) and CSB (chip selection input) are used.
By setting CSB to “Low”, KS0090 can receive SCL input. If CSB is set to “High”, KS0090 resets the internal 8-bit shift register and 3-bit counter.
Serial data is input in the order of “D7, D6, D5, D4, D3, D2, D1, D0” from the serial data input pin (SI = DB7) at the rising edge of serial clock (SCL = DB6). At the rising edge of the 8th serial clock, the serial data (D7–D0) is converted into 8-bit bus mode data. The RS input of the DR/IR selection is latched at the rising edge of the 8th serial clock (SCL).

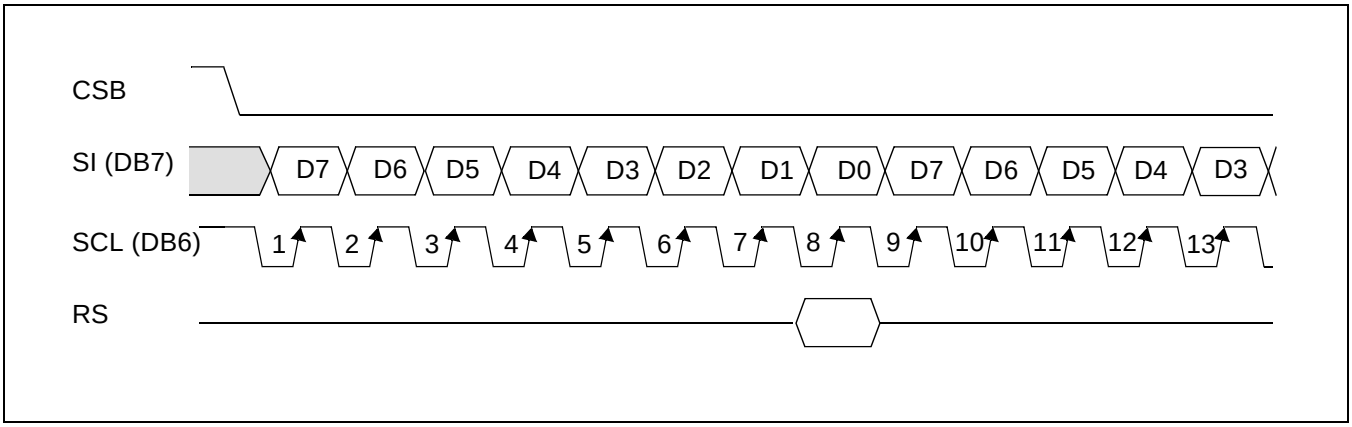


Figure 6. Serial Data Transfer

ADDRESS COUNTER (AC)

The address counter (AC) in KS0090 stores the CGRAM/DDRAM/ICONRAM address, which is transferred from IR. After writing into CGRAM/DDRAM/ICONRAM, AC is automatically increased by 1.

DISPLAY DATA RAM (DDRAM)

DDRAM stores display data of maximum 36 × 8 bits (Max. 36 characters).
DDRAM address is set in the address counter (AC) as a hexadecimal number.

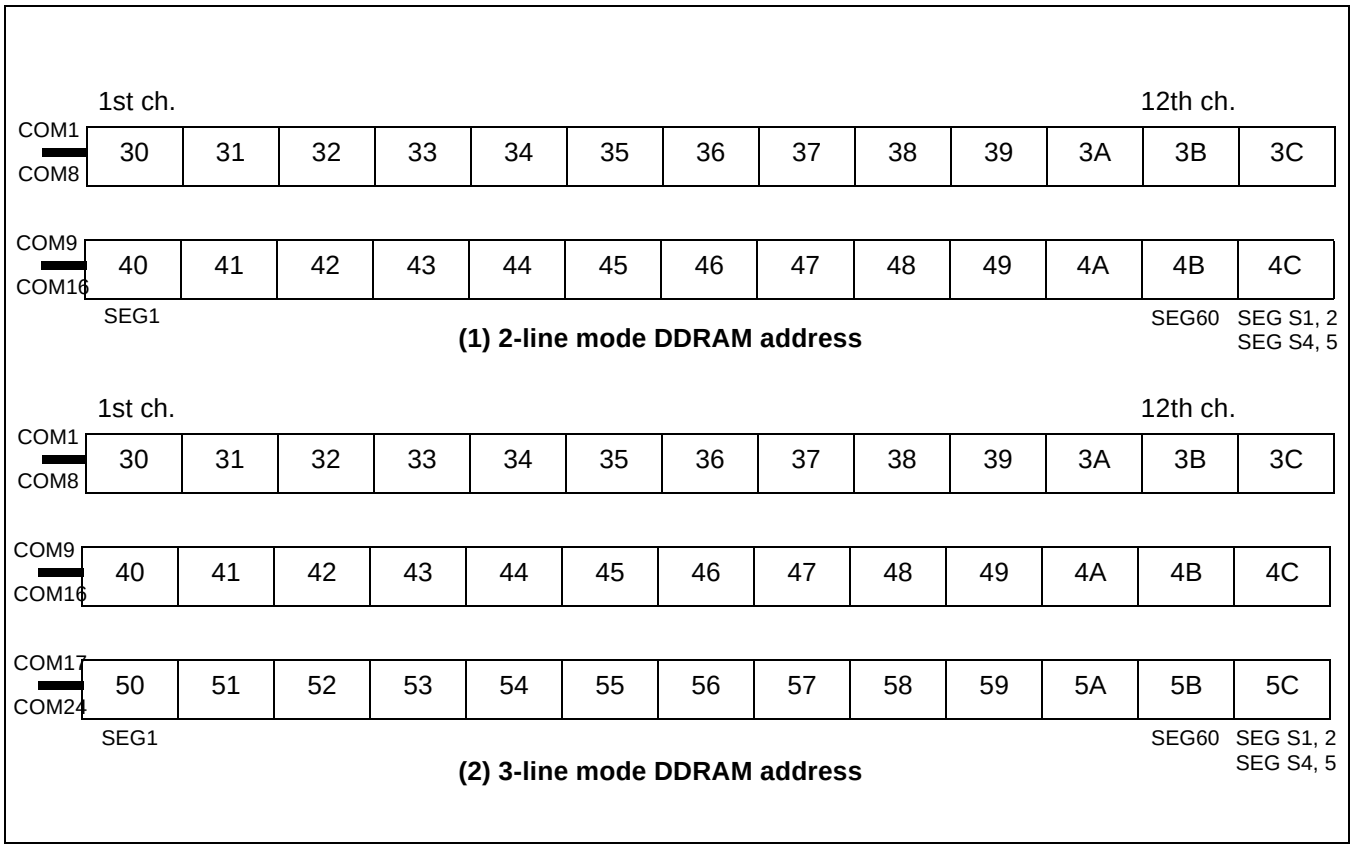


Figure 7. DDRAM Address

CHARACTER GENERATOR ROM (CGROM)

KS0090 has the character generator ROM (CGROM) consisting of up to 256 types of characters. Character size is 5 × 8 dots. The CG bit of the instruction table selects the 4 characters (00h to 03h) of CGROM or CGRAM. KS0090 CGROM is contact mask option ROM and compatible with customized ROM font.

Figure 8. CGROM Character Code Table (F00)

CHARACTER GENERATOR RAM (CGRAM)

CGRAM contained in KS0090 enables the user to program the character pattern to display signals.
When using CGRAM, the CG bit should be selected to “High”. CGRAM has up to four 5 x 8-dot characters.
By writing font data to CGRAM, the user defined character can be used.

Table 3. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

Character Code (DDRAM data)								CGRAM Address								CGRAM Data (Character pattern)								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–	–	–	0	1	0	1	0	Pattern 1
			(00h)					0	0	0	0	0	0	0	1	–	–	–	1	0	1	0	1	
								0	0	0	0	0	0	1	0	–	–	–	0	1	0	1	0	
								0	0	0	0	0	0	1	1	–	–	–	1	0	1	0	1	
								0	0	0	0	0	1	0	0	–	–	–	0	1	0	1	0	
								0	0	0	0	0	1	0	1	–	–	–	1	0	1	0	1	
								0	0	0	0	0	1	1	0	–	–	–	0	1	0	1	0	
								0	0	0	0	0	1	1	1	–	–	–	1	0	1	0	1	
0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	–	–	–	0	0	0	0	0	Pattern 2
			(01h)					0	0	0	0	1	0	0	1	–	–	–	1	1	1	1	1	
								0	0	0	0	1	0	1	0	–	–	–	0	0	0	0	0	
								0	0	0	0	1	0	1	1	–	–	–	1	1	1	1	1	
								0	0	0	0	1	1	0	0	–	–	–	0	0	0	0	0	
								0	0	0	0	1	1	0	1	–	–	–	1	1	1	1	1	
								0	0	0	0	1	1	1	0	–	–	–	0	0	0	0	0	
								0	0	0	0	1	1	1	1	–	–	–	1	1	1	1	1	
0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	–	–	–	0	1	0	1	0	Pattern 3
			(02h)					0	0	0	1	0	0	0	1	–	–	–	0	1	0	1	0	
								0	0	0	1	0	0	1	0	–	–	–	0	1	0	1	0	
								0	0	0	1	0	0	1	1	–	–	–	0	1	0	1	0	
								0	0	0	1	0	1	0	0	–	–	–	0	1	0	1	0	
								0	0	0	1	0	1	0	1	–	–	–	0	1	0	1	0	
								0	0	0	1	0	1	1	0	–	–	–	0	1	0	1	0	
								0	0	0	1	0	1	1	1	–	–	–	0	1	0	1	0	
0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	–	–	–	0	1	0	1	0	Pattern 4
			(03h)					0	0	0	1	1	0	0	1	–	–	–	0	1	0	1	0	
								0	0	0	1	1	0	1	0	–	–	–	1	0	1	0	1	
								0	0	0	1	1	0	1	1	–	–	–	1	0	1	0	1	
								0	0	0	1	1	1	0	0	–	–	–	0	1	0	1	0	
								0	0	0	1	1	1	0	1	–	–	–	0	1	0	1	0	
								0	0	0	1	1	1	1	0	–	–	–	1	0	1	0	1	
								0	0	0	1	1	1	1	1	–	–	–	1	0	1	0	1	

(“–”: Don’t care)

SEGMENT ICON RAM (ICONRAM)

ICONRAM has segment control data and segment pattern data.

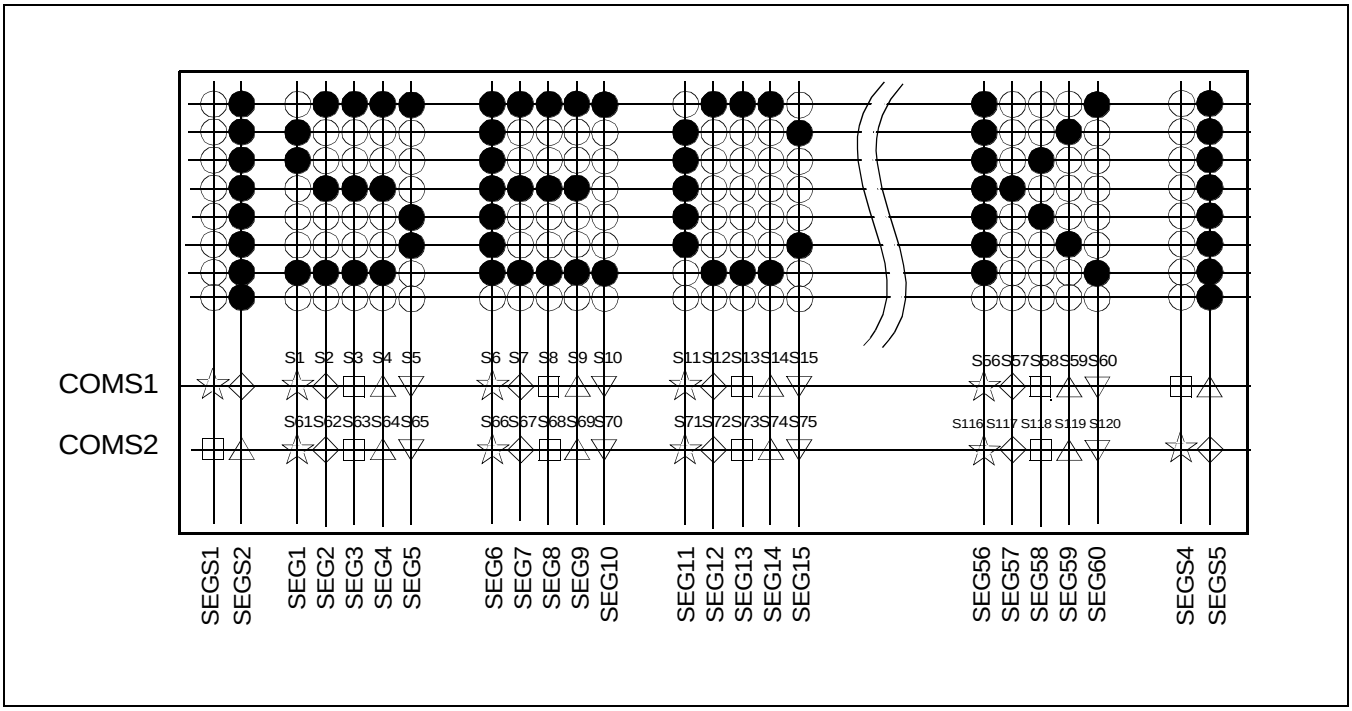


Figure 9. Relationship between ICONRAM and Icon Display

Table 4. Relationship between ICONRAM Address and Display Pattern

ICONRAM Address		ICONRAM Bits							
High Order	Low Order	D7	D6	D5	D4	D3	D2	D1	D0
6	0	–	–	–	S1	S2	S3	S4	S5
	1	–	–	–	S6	S7	S8	S9	S10
	:	:	:	:	:	:	:	:	:
	A	–	–	–	S51	S52	S53	S54	S55
	B	–	–	–	S56	S57	S58	S59	S60
	C	–	–	–	SEGS1	SEGS2	–	SEGS4	SEGS5
7	0	–	–	–	S61	S62	S63	S64	S65
	1	–	–	–	S66	S67	S68	S69	S70
	:	:	:	:	:	:	:	:	:
	A	–	–	–	S111	S112	S113	S114	S115
	B	–	–	–	S116	S117	S118	S119	S120
	C	–	–	–	SEGS1	SEGS2	–	SEGS4	SEGS5

("–": Don't care)

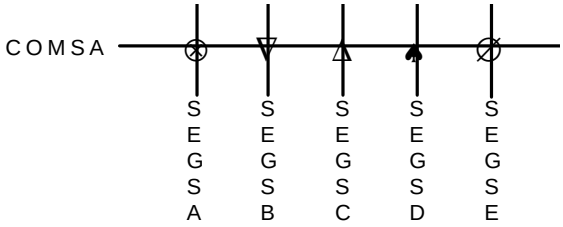
STATIC ICON RAM (SI)

KS0090 contains the static icon RAM to display the static icons in addition to the dynamic icons. Capacity of static icon RAM is 10-bits and is capable of displaying up to 5 icons.
The following table shows the relationship between the static icon functions, static icon RAM address and written data (Blink frequency: 1 to 2 Hz).

Table 5. Relationship between static icon RAM address and display pattern

Function	RAM Address	Static Icon Data								Static Icon				
		D7	D6	D5	D4 (A)	D3 (B)	D2 (C)	D1 (D)	D0 (E)	SEGS -A	B	C	D	E
Display On/Off	20h	–	–	–	0	1	0	1	0	□	■	□	■	□
Blink On/Off	21h	–	–	–	1	1	1	0	0	■	□	■	■	□

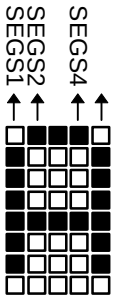
20h = “0”: Static icon off
“1”: Static icon on
21h = “0”: Blink off
“1”: Blink on (20h data are inverted)



SEGMENTS FOR SIGNAL DISPLAY (FS)

When DDRAM address is 3Ch: COM1 to COM8, 1 line
4Ch: COM9 to COM16, 2 line
5Ch: COM17 to COM24, 3 line

SEGS1: Font 1st bit display
SEGS2: Font 2nd bit display
SEGS4: Font 4th bit display
SEGS5: Font 5th bit display
(Font 3rd bit is not displayed.)



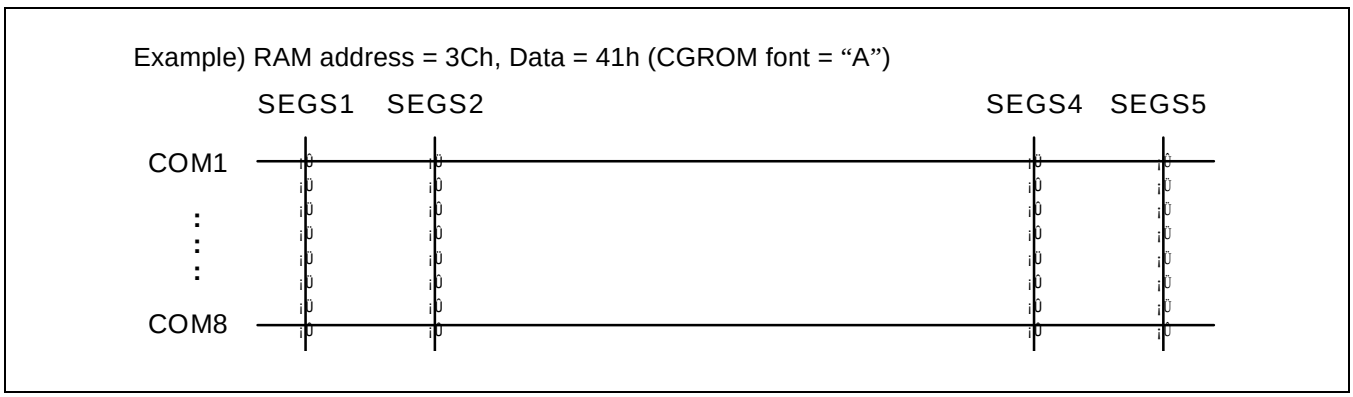


Figure 10. Segment for Signal Display

LOW POWER CONSUMPTION MODE

KS0090 provides a “standby mode” and “sleep mode” to reduce power consumption during the standby period.

Standby Mode (Power save bit on, Oscillation bit on)

The standby mode can be switched on and off by the power save command.
In the standby mode, only the static icon is displayed.

1. Liquid crystal display output
   COM1 to COM24, COMS1, COMS2: Vss level
   SEG1 to SEG60, SEGS1, 2, 4, 5: Vss level
   SEGSA, B, C, D, E, COMSA: V_{DD} or V_{SS} level (Can be turned on/off by static drivers)
   Use the static icon RAM for controlling the static icon display done with SEGSA, B, C, D, E, COMSA.
2. Written data in DDRAM, CGRAM, ICONRAM and registers remain at its previous value.
3. Operation mode is retained the same as it was prior to execution of the standby mode.
   The internal circuit for the dynamic display output is stopped.
4. The oscillation circuit for the static display must remain “on”.

Sleep Mode (Power save on, Oscillation off)

To enter the sleep mode, the power circuit and oscillation circuit should be turned off by the power save command and power control command. This mode helps reduce power consumption by reducing current to reset level.

1. Liquid crystal display output
   COM1 to COM24, COMS1, COMS2: V_{SS} level
   SEG1 to SEG60, SEGS1, 2, 4, 5: V_{SS} level
   SEGSA, B, C, D, E, COMSA: V_{SS} level
2. Written data in DDRAM, CGRAM, ICONRAM and registers remain at its previous value.
3. Operation mode is retained as it was prior to execution of the sleep mode.
   All internal circuits are stopped.
4. Power circuit and oscillation circuit
   The built-in power supply circuit and oscillation circuit are turned off by the power save command and power control command.

LCD DRIVER CIRCUIT

LCD driver circuit has 26 common and 64 segment signals for driving LCD. Data from ICONRAM/CGRAM/ CGROM are transferred to 64-bit segment register serially, and then they are stored to 64-bit latch. For 2-line display mode, COM1 to COM16, COMS1, and COMS2 have 1/18 duty, and in 3-line mode, COM1 to COM 24, COMS1, and COMS2 have 1/26 duty ratio.
SEG bidirectional function is selected by the BID input pin, and COM shift direction is selected by the function set instruction “S” bit.

Table 6. SEG Data Shift Direction

BID pin	SEG Data Shift Direction
Low	SEGS1 → SEGS2 → SEG1→ ..... → SEG60 → SEGS4 → SEGS5
High	SEGS5 → SEGS4 → SEG60 → ..... → SEG1 → SEGS2 → SEGS1

INSTRUCTION DESCRIPTION

Table 7. Instruction Table

Instruction	Instruction Code									Description
	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Return Home	0	0	0	0	1	–	–	–	–	DDRAM address is set to “30h” from AC and cursor returns to “30h” position if shifted. The contents of DDRAM are not changed.
Display Control	0	0	0	1	1	C	B	–	D	Cursor/blink /display on/off C = 0: cursor off (default), C = 1: cursor on B = 0: blink off (default), B = 1: blink on D = 0: display off (default), D = 1: display on
Power Save	0	0	1	0	0	–	–	OS	PS	Power save/oscillation circuit. OS = 0: oscillator off (default), OS = 1: oscillator on PS = 0: power save off (default), PS = 1: power save on
Power Control	0	0	1	0	1	0	VR	VF	VC	LCD power control VR = 0: voltage regulator off (default), 1: voltage regulator on VF = 0: voltage follower off (default), 1: voltage follower on VC = 0: voltage converter off (default), 1: voltage converter on
Function Set	0	0	1	1	0	N2	N1	S	CG	Display line mode. N2, N1 = 0, 0: 2 line display mode (default), 0, 1: 3 line display mode Set shifting direction of COM S = 0: COM left shift (COM1→ COM24) (default), 1: COM right shift (COM24 → COM1) Select CGRAM or CGROM CG = 0: use CGROM (default), 1: use CGRAM
RAM Address Set	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	DDRAM/CGRAM/ICONRAM or register address.
Write Data	1	D7	D6	D5	D4	D3	D2	D1	D0	Write DDRAM/CGRAM/ICONRAM or register data.
EV Mode	0	0	0	0	0	0	0	0	EV	Electronic volume step EV = 0: 32 contrast-step (default), 1: 64 contrast-step
Test Mode	0	0	0	0	0	*	*	*	*	Instruction for IC chip test. Don’t use this instruction.

(“–”: Don’t care, “*”: Don’t use)

NOTES:

1. For the NOP instruction,
   when EV mode is “0” (32 contrast-step), the NOP instruction set is (000000000), and
   when EV mode is “1” (64 contrast-step), the NOP instruction set is (000000001).
2. Instruction execution time depends on the internal process time of KS0090, therefore it is necessary to provide a time larger than one MPU interface cycle time (tc) between execution of two successive instructions.

RETURN HOME

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**1**	**-**	**-**	**-**	**-**

("–": Don't care)

Retrun home instruction field makes the cursor return home.
DDRAM address is set to "30h" into the address counter. Return cursor to first digit of the first line. The contents of DDRAM are not changed.

DISPLAY CONTROL

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**1**	**1**	**C**	**B**	**-**	**D**

("–": Don't care)

Display control instruction field controls cursor / blink / display on / off.

C **Cursor on / off control bit**

H	Cursor is turned on.
L	Cursor is disappeared in current display and can't blink (default).

B **Cursor blink on / off control bit**

H	When C = "H", KS0090 makes LCD alternate between inverting display character and normal display character at the cursor position with about a half second. On the contrary, if C = "Low", only a normal character is displayed regardless of the B flag.
L	Blink is off (default).

D **Display on / off control bit**

H	Display is turned on
L	Display is turned off, but display data remain in DDRAM (default).

NOTE: Static icons driven by COMSA and SEGSA/B/C/D/E must be controlled by the static icon RAM.

POWER SAVE

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**0**	**-**	**-**	**OS**	**PS**

("–": Don't care)

Power save instruction field is used to control the oscillator and power save mode.

OS **Oscillator on / off control bit**

H	Oscillator is turned on.
L	Oscillator is turned off (default).

PS **Power save on / off control bit**

H	Power save mode is turned on.
L	Power save mode is turned off (default).

POWER CONTROL

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**VR**	**VF**	**VC**

Power control instruction filed sets voltage regulator / follower / converter on / off.

VR **Voltage regulator circuit control bit**

H	Voltage regulator is turned on.
L	Voltage regulator is turned off (default).

VF **Voltage follower circuit control bit**

H	Voltage follower is turned on.
L	Voltage follower is turned off (default).

VC **Voltage converter circuit control bit**

H	Voltage converter is turned on.
L	Voltage converter is turned off (default).

NOTE: The oscillator circuit must be turned on for the voltage converter circuit to be active.

FUNCTION SET

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**0**	**N2**	**N1**	**S**	**CG**

N2, N1 **Display line mode instruction field selects 2-line or 3-line display mode**

L	L	2-Line display mode (default)
L	H	3-Line display mode

S **Data shift direction of common**

H	COM right shift (default)
L	COM left shift

Table 8. COM Data Shift Direction

Line Mode	S	COM Data Shift Direction
2 Line Mode	0 (Left)	COM1 → ..... → COM15 → COM16 → COMS1 →COMS2 → COM1
	1 (Right)	COM16 → COM15 →..... → COM1 → COMS1 → COMS2 → COM16
3 Line Mode	0 (Left)	COM1 → ..... → COM23 → COM24 → COMS1 → COMS2 → COM1
	1 (Right)	COM24 → COM23 → ..... → COM1 → COMS1 → COMS2 → COM24

CG **CGRAM enable bit**

H	CGRAM can be accessed and you can use this RAM as a four special character area. (00h – 03h = CGRAM font display)
L	CGRAM is disabled. CGROM (00h to 03h) can be accessed and the additional current consumption is saved by using this mode (default). (00h – 03h = CGROM font display)

RAM ADDRESS SET

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**1**	**AC6**	**AC5**	**AC4**	**AC3**	**AC2**	**AC1**	**AC0**

RAM address set instruction field sets CGRAM / DDRAM / ICONRAM or register address. Each RAM is distinguished by a RAM address.
Before writing data into the RAM, set the address by RAM address set instruction. Next, when data are written in succession, the address is automatically increased by 1.

Table 9. RAM Address Mapping

Address	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**
00h	CGRAM (00h)								CGRAM (01h)							
10h	CGRAM (02h)								CGRAM (03h)							
20h	SI		Unused						EV	TE	Unused					
30h	DDRAM line 1 (30h to 3Bh)												FS	Unused		
40h	DDRAM line 2 (40h to 4Bh)												FS			
50h	DDRAM line 3 (50h to 5Bh)												FS			
60h	ICONRAM COMS1 Icon (60h – 6Ch)													Unused		
70h	ICONRAM COMS2 Icon (70h – 7Ch)															

NOTE:
SI: Static icon register (20h, 21h). It is used for SEGS/B/C/D/E
EV: Electronic volume register (28h)
TE: Test register (29h) (Do not use.)
FS: For signals: 1 line (3Ch), 2 line (4Ch), 3 line (5Ch). It is used for SEGS1/2/4/5.

WRITE DATA

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

This instruction field makes KS0090 write binary 8-bit data to DDRAM / CGRAM / ICONRAM or register. The RAM address to be written into is determined by the previous RAM Address Set instruction. After writing operation, the address is automatically increased by 1.

EV MODE

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**EV**

This instruction field selects between 2 electronic volume steps: 32 and 64 contrast-step.

When the EV = “Low”, KS0090 selects 32 contrast-step (default), and when

Electronic volume register (28h)=

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
–	–	–	**C4**	**C3**	**C2**	**C1**	**C0**

(“–”: Don’t care)

When the EV = “High”, KS0090 selects 64 contrast-step.

Electronic volume register (28h)=

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
–	–	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**

(“–”: Don’t care)

INITIALIZING & POWER SAVE MODE SETUP

HARDWARE RESET

After reset by RES pin, KS0090 can be initialized the following state.

1. Control Display on/off instruction

C=0: Cursor off
B=0: Blink off
D=0: Display off

2. Power Save Set instruction

OS=0: Oscillator off
PS=0: Power save off

3. Power Control Set instruction

VR=0: Voltage regulator off
VF=0: Voltage follower off
VC=0: Voltage converter off

4. Function Set instruction

N2=0, N1=0: 2 line display mode
S=0: COM left shift
CG=0: CGRAM is not used

5. Return Home

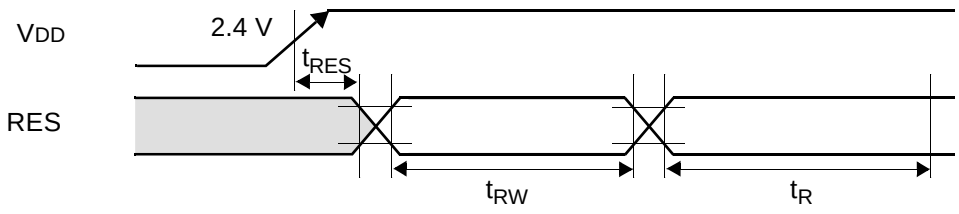
Address counter = 30h

6. Static icon RAM & electronic contrast control register

Static icon RAM: 20h = (0, 0, 0, 0, 0), static icon off
21h = (0, 0, 0, 0, 0), blink off
EV = 0: 32 contrast-step
Electronic contrast control register: 28h = ((0),0, 0, 0, 0, 0), contrast high

7. In case of 4-bit interface mode selection KS0090 considers the first 4-bit data from MPU as the high order bits.

NOTE: If initialization is not done by the RES pin at application, an unknown condition may result, in which case you can initialize by instruction.

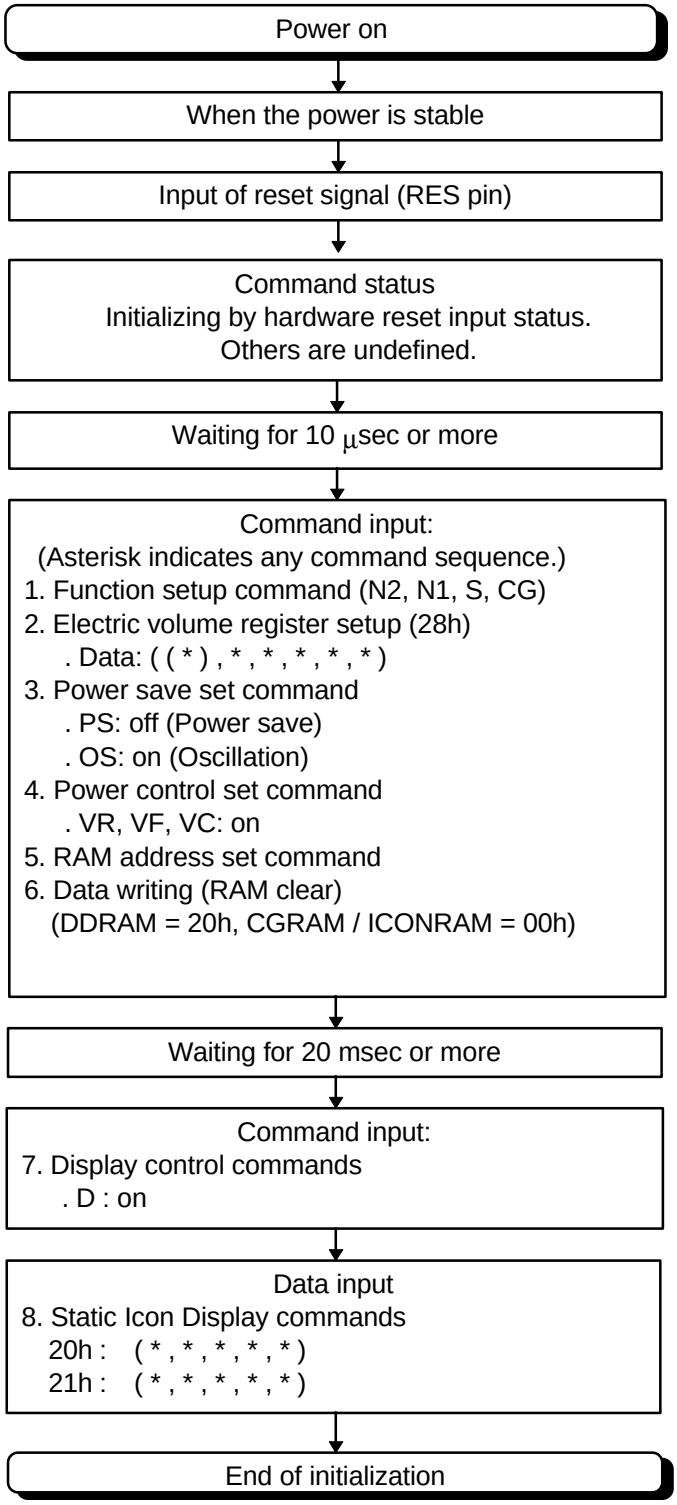


Reset time	t_R	1 µs
Reset pulse width	t_{RW}	10 µs
Reset start time	t_{RES}	50 ns

Figure 11. RESET Timing

INITIALIZING AND POWER SAVE MODE SETUP

Initializing by Instruction



NOTES:
At command (5) and (6), the internal RAM should be cleared.

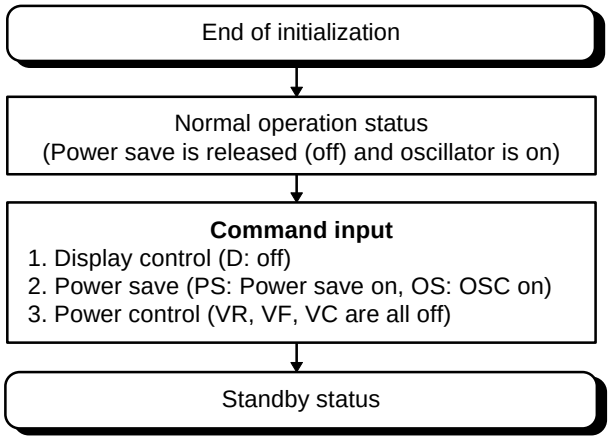
To clear DDRAM and FS (segment for signal)
–Set address at 30h (first DDRAM) and then write 20h (space character code) 13 times
–Set address at 40h and write 20h for 13 times
–Set address at 50h and write 20h for 13 times

To clear CGRAM,
–Set address at 00h (first CGRAM) and then write 00h (null data) 32 times

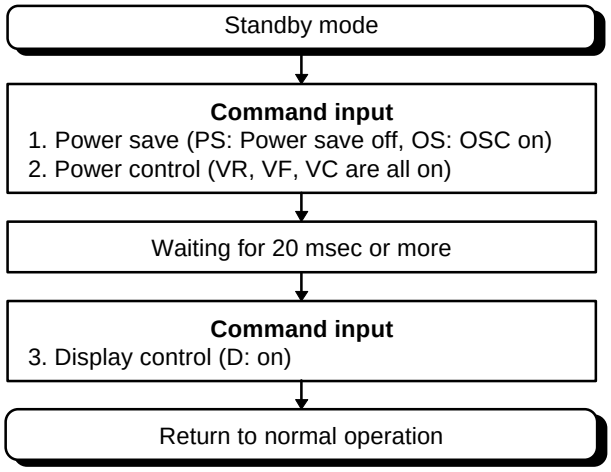
To clear ICONRAM,
–Set address at 60h (first ICONRAM) and then write 00h (null data) 13 times
–Set address at 70h and write 00h for 13 times

Standby Mode Set or Release by Instruction

(a) Standby mode set

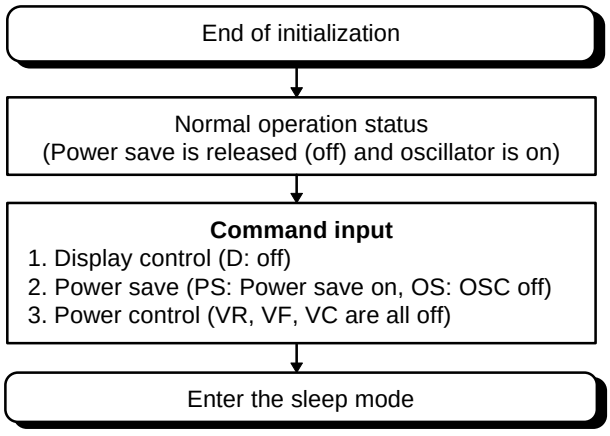


(b) Standby mode release

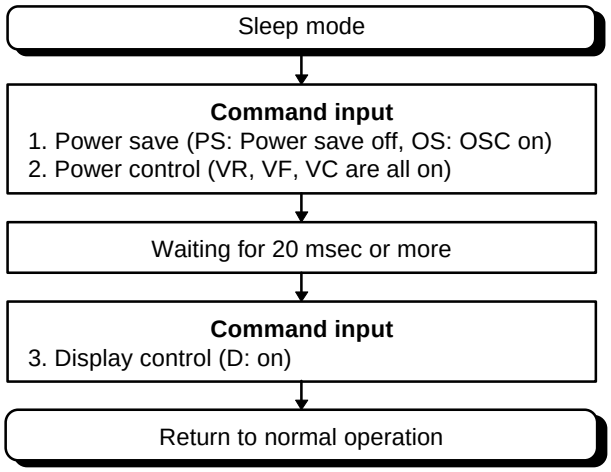


Sleep Mode Set or Release by Instruction

(a) Sleep mode set



(b) Sleep mode release



LCD DRIVING POWER SUPPLY CIRCUIT

The power supply circuit produces LCD panel driving voltage at low power consumption. The LCD driving power supply circuit consists of voltage converter (2 times or 3 times), voltage regulator, and voltage follower. It is controlled by power control instruction. Table 10. shows how the LCD driving power supply circuit works by power control instruction sets.

Table 10. Power Supply Control Mode Set

VR	VF	VC	Voltage Regulator	Voltage Follower	Voltage Converter	VOUT Pin	VR Pin	V0, V1, V2, V3, V4 Pin
1	1	1	Enable	Enable	Enable	Internal voltage output	Used for voltage adjustment	Internal voltage output
1	1	0	Enable	Enable	Disable	External voltage input	Used for voltage adjustment	Internal voltage output
0	1	0	Disable	Enable	Disable	Open	Open	V1 – V4: Internal voltage output V0: External voltage input
0	0	0	Disable	Disable	Disable	Open	Open	V0 – V4: External voltage input

NOTE: Any other case which is not written in this table is prohibited.

VOLTAGE CONVERTER

If capacitors are connected between CAP1+ and CAP1-, CAP2+ and CAP2-, VDD and VOUT, VDD- VSS voltage is positively tripled and generated at VOUT terminal. When the voltage is doubled, open CAP2- and connect CAP2+ to VOUT terminal.
This boosted voltage is used in the built-in voltage regulator circuit.

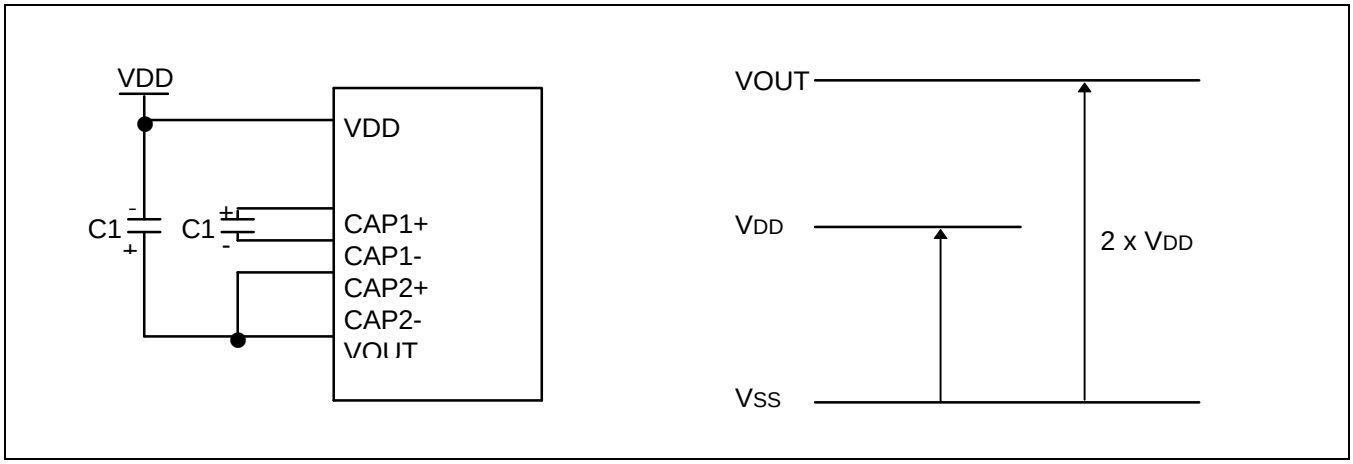


Figure 12. Two Times Boosting

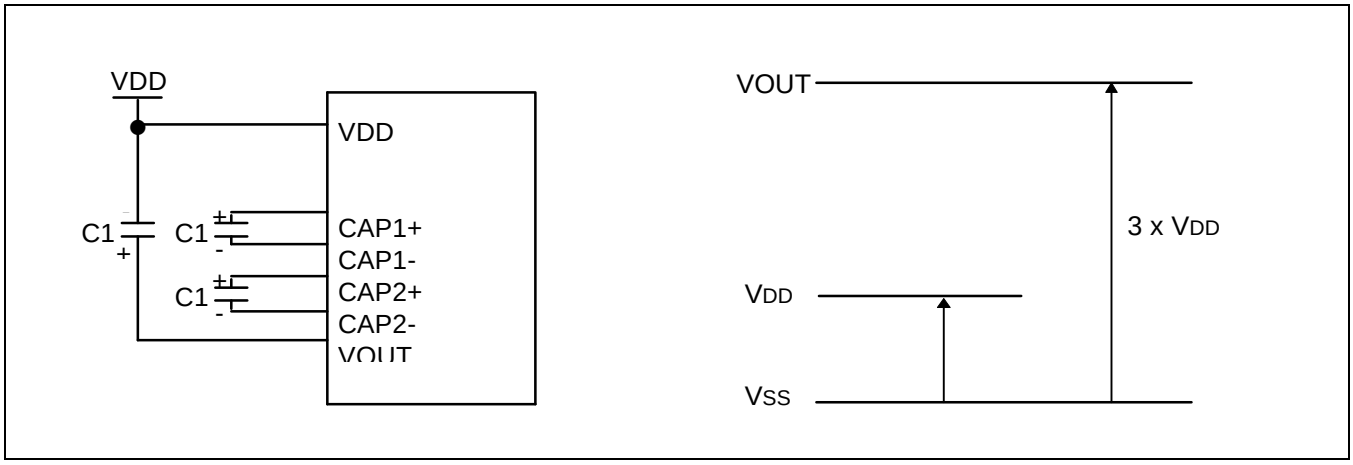


Figure 13. Three Times Boosting

VOLTAGE REGULATOR

The voltage regulator circuit is used to obtain an appropriate LCD panel driving voltage. This voltage is obtained by adjusting resistors Ra and Rb as shown in equation (1), and by setting electronic contrast control data bits. See equation (2) or (3).
The potential of V0 pin can be adjusted within V_{REF} to VOUT. V_{REF} is the internal constant voltage source of the chip and this value is 2.0V in the condition $V_{DD} \geq 2.4V$.

Voltage regulation by adjusting resistors Ra, Rb

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{REF} \quad \text{..... (1)}$$

The internal V_{REF} of voltage regulator has the temperature compensation function, and the temperature coefficient is approximately –0.05%/°C at range –20°C to +50°C.

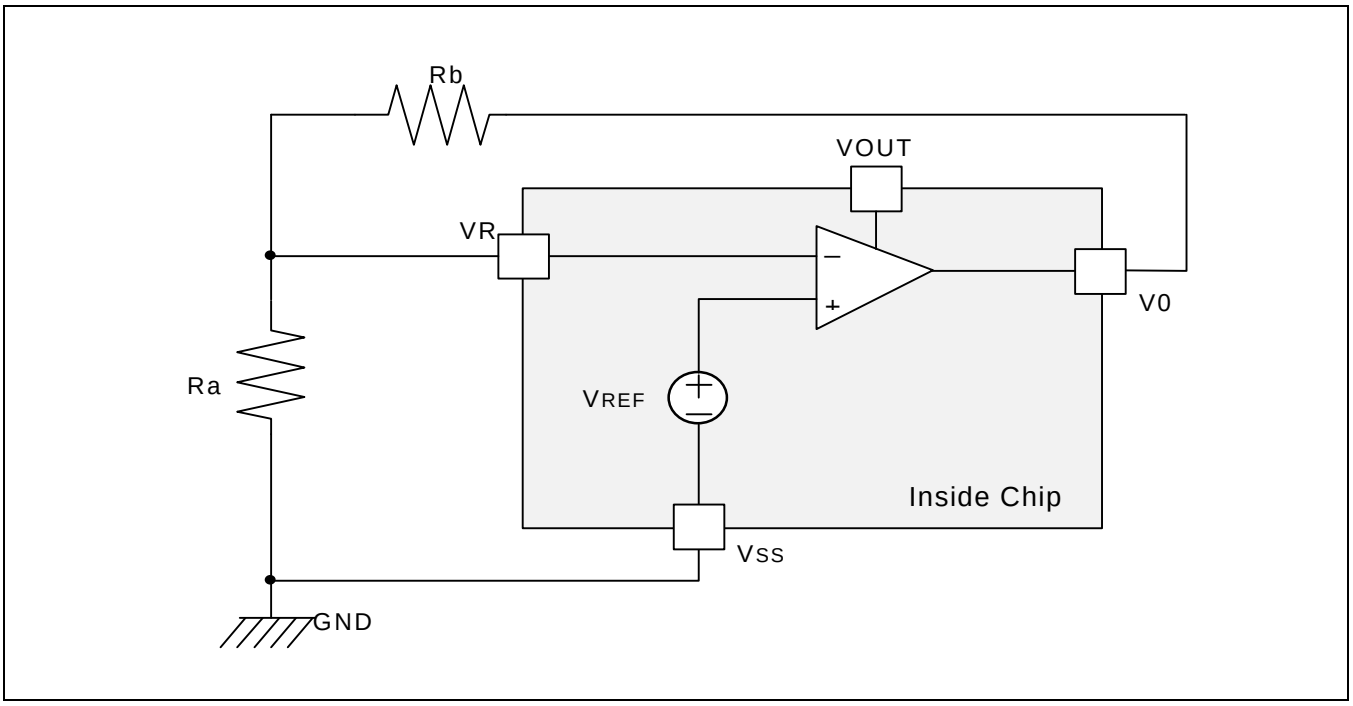


Figure 14. Voltage Regulator Circuit

ELECTRONIC CONTRAST CONTROL (EV=0, 32 STEPS)

For 32 contrast-step, EV flag of EV set mode instruction field should be set to “Low”. Then, electronic contrast control data bits 28h = (C4,C3,C2,C1,C0) can be valid. Voltage regulation is adjusted as 32-contrast step according to the value of Electronic Contrast Control data bits. LCD drive voltage V0 has one of 32 voltage values if 5-bit data is set to the electronic contrast control register (RAM address 28h). When using the electronic contrast control function, you need to turn on the voltage regulator using power control instruction.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad \text{..... (2)}$$

$$V_{EV} = V_{REF} - n\alpha \qquad (n = 0, 1, 2, \text{..... } 30, 31)$$

$$\alpha = V_{REF} / 150$$

For example Ra = 1 MΩ, Rb = 2 MΩ, n = 0 then V0 = 6 V

Table 11. Electronic Contrast Control Register (32 Steps)

No.	C7	C6	C5	C4	C3	C2	C1	C0	nα	V0	Contrast
0	–	–	–	0	0	0	0	0	0 (default)	Maximum	High
1	–	–	–	0	0	0	0	1	1 α	:	:
2	–	–	–	0	0	0	1	0	2 α	:	:
3	–	–	–	0	0	0	1	1	3 α	:	:
:	:	:	:	:	:	:	:	:	:	:	:
30	–	–	–	1	1	1	1	0	(n-1) α	:	:
31	–	–	–	1	1	1	1	1	n α	Minimum	Low

(“–”: Don’t care)

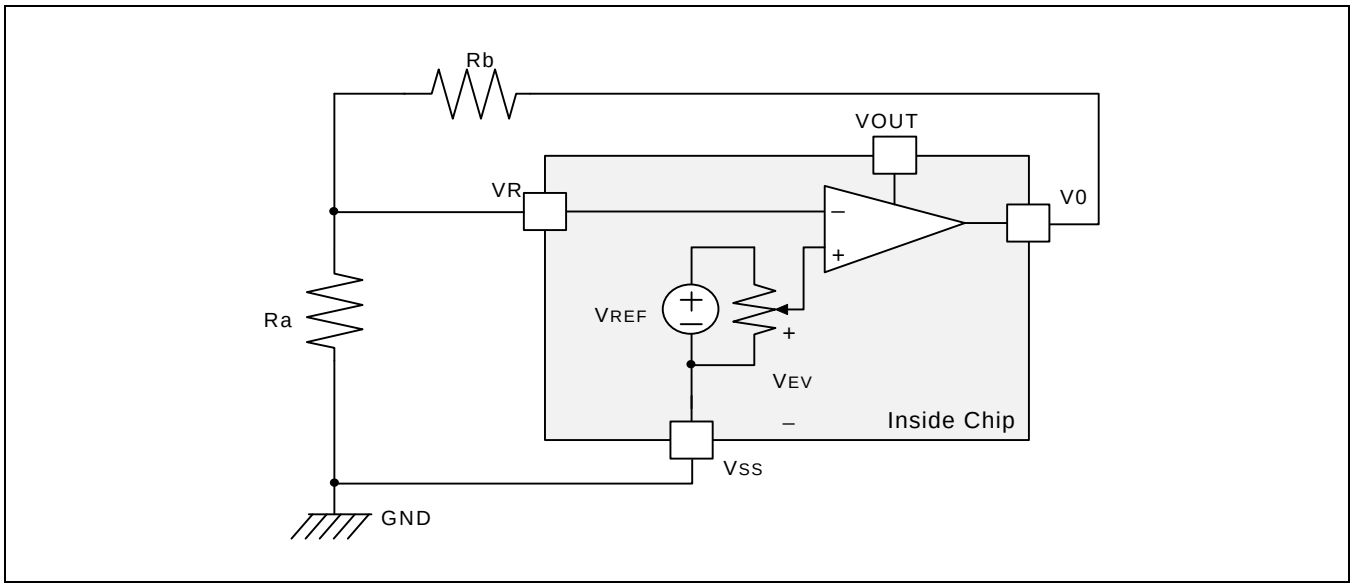


Figure 15. Electronic Contrast Control Circuit

ELECTRONIC CONTRAST CONTROL (EV=1, 64 STEPS)

For 64 contrast-step, EV flag of EV set mode instruction field should be set to “High”. After this, electronic contrast control data bits 28h = (C5, C4,C3,C2,C1,C0) can be valid. Voltage regulation is adjusted as 64-contrast step according to the value of Electronic Contrast Control data bits. LCD drive voltage V0 has one of 64 voltage values if 6-bit data is set to the electronic contrast control register (RAM address 28h). When using the electronic contrast control function, you must turn on the voltage regulator using power control instruction.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad \text{..... (3)}$$

$$V_{EV} = V_{REF} - n\alpha \qquad (n = 0, 1, 2, \text{..... } 62, 63)$$

$$\alpha = V_{REF} / 300$$

Table 12. Electronic Contrast Control Register (64 Steps)

No.	C7	C6	C5	C4	C3	C2	C1	C0	nα	V0	Contrast
0	–	–	0	0	0	0	0	0	0 (default)	Maximum	High
1	–	–	0	0	0	0	0	1	1 α	:	:
2	–	–	0	0	0	0	1	0	2 α	:	:
3	–	–	0	0	0	0	1	1	3 α	:	:
:	:	:	:	:	:	:	:	:	:	:	:
62	–	–	1	1	1	1	1	0	(n-1) α	:	:
63	–	–	1	1	1	1	1	1	n α	Minimum	Low

(“–”: Don’t care)

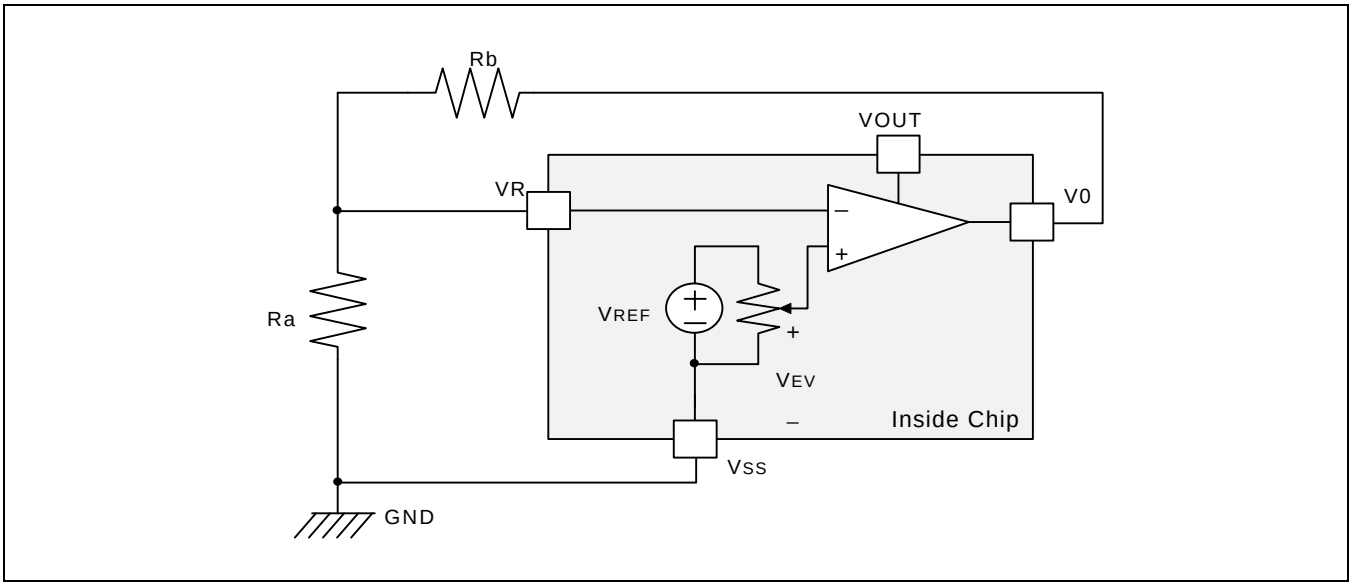
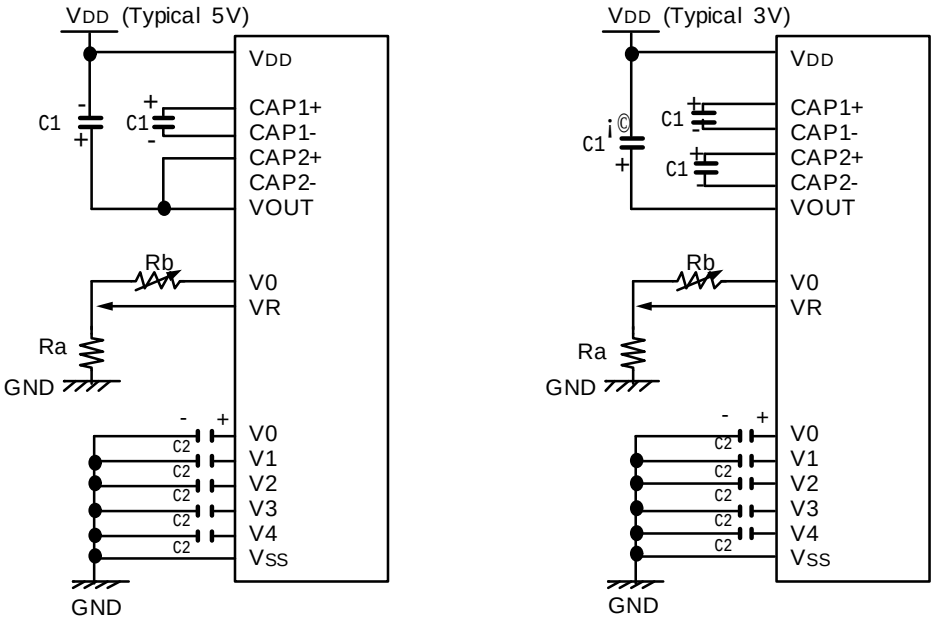


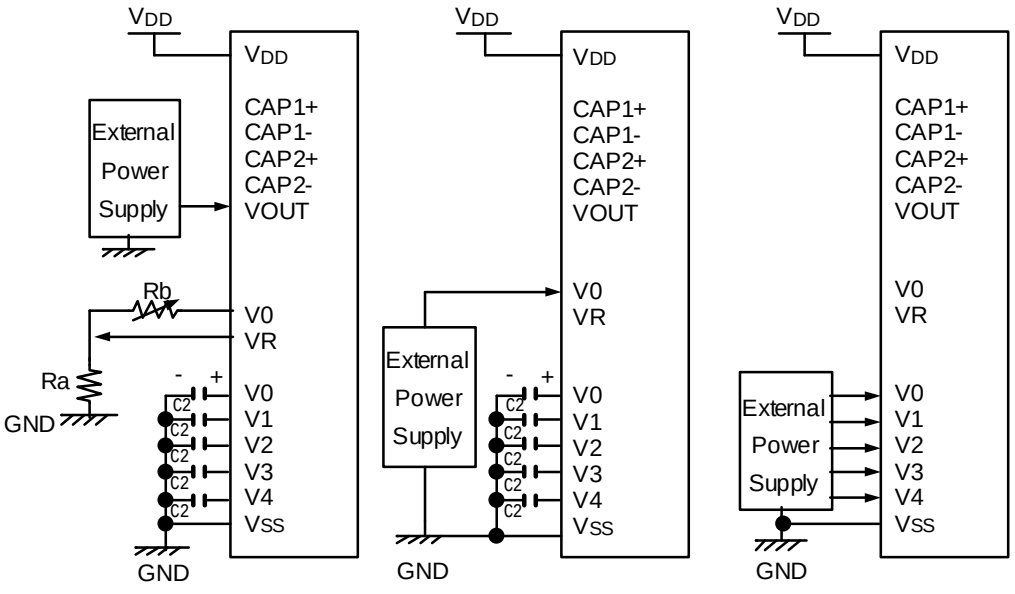
Figure 16. Electronic Contrast Control Circuit

VOLTAGE GENERATOR CIRCUIT



* Reference setting values : C1 = 0.1 ~ 4.7uF, C2 = 0.1uF

Figure 17. When Built-in Power Supply is Used (VR, VF, VC = 1, 1, 1)



* Reference setting values : C2 = 0.1 ~ 4.7uF

Figure 18. When External Power Supply is Used

MPU INTERFACE

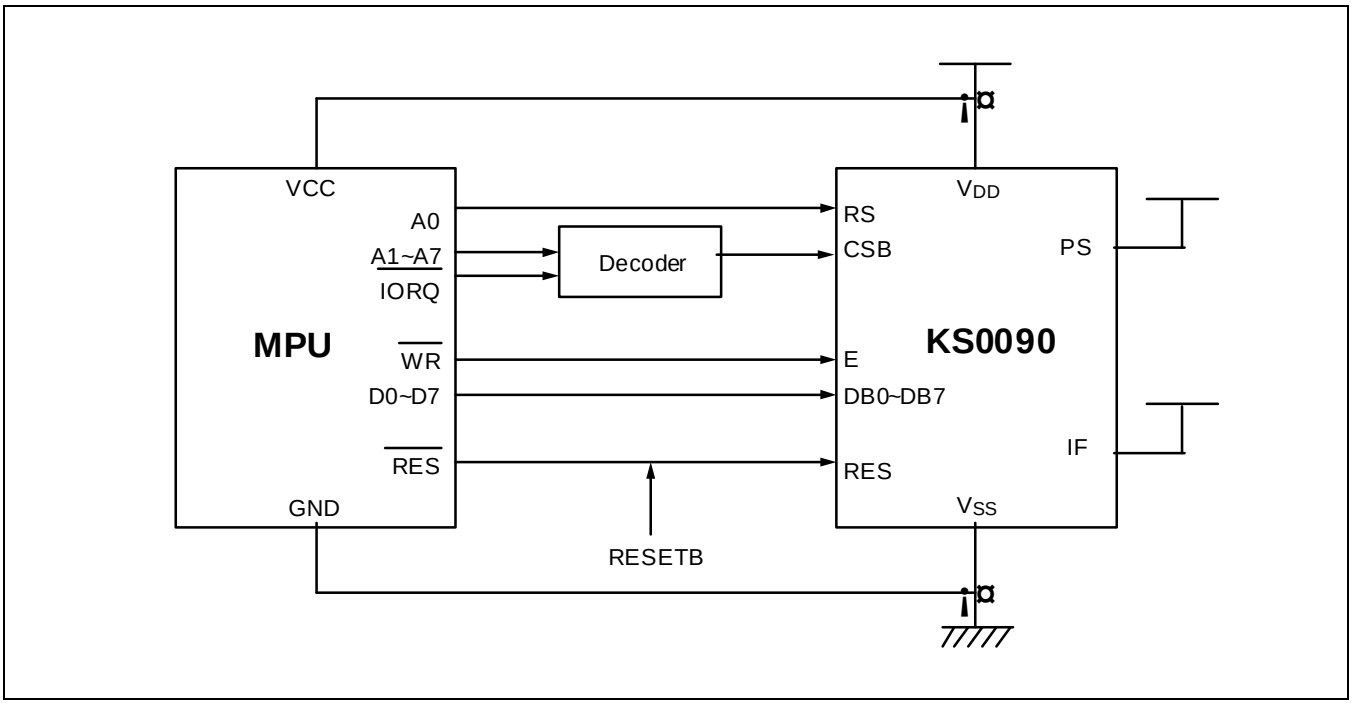


Figure 19. Parallel Interfacing with 8080-series Microprocessors.

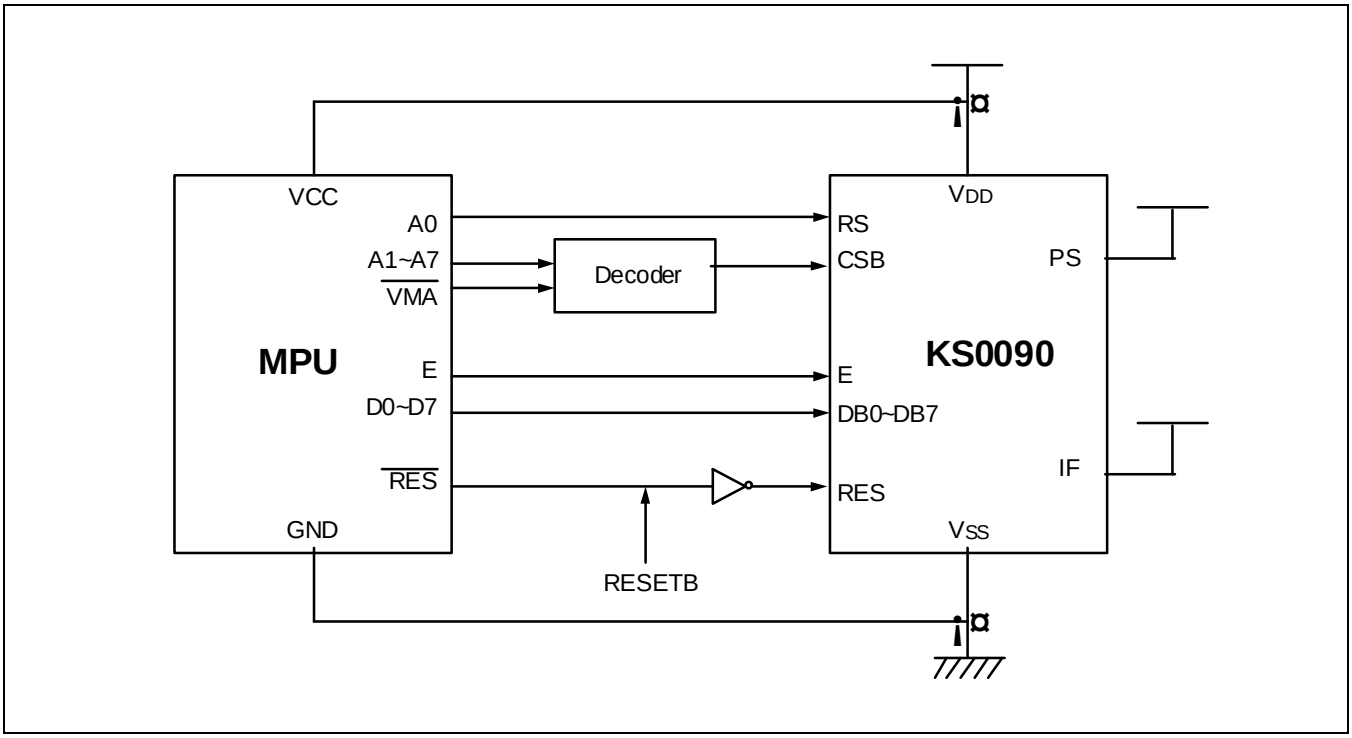


Figure 20. Parallel Interfacing with 6800-series Microprocessors.

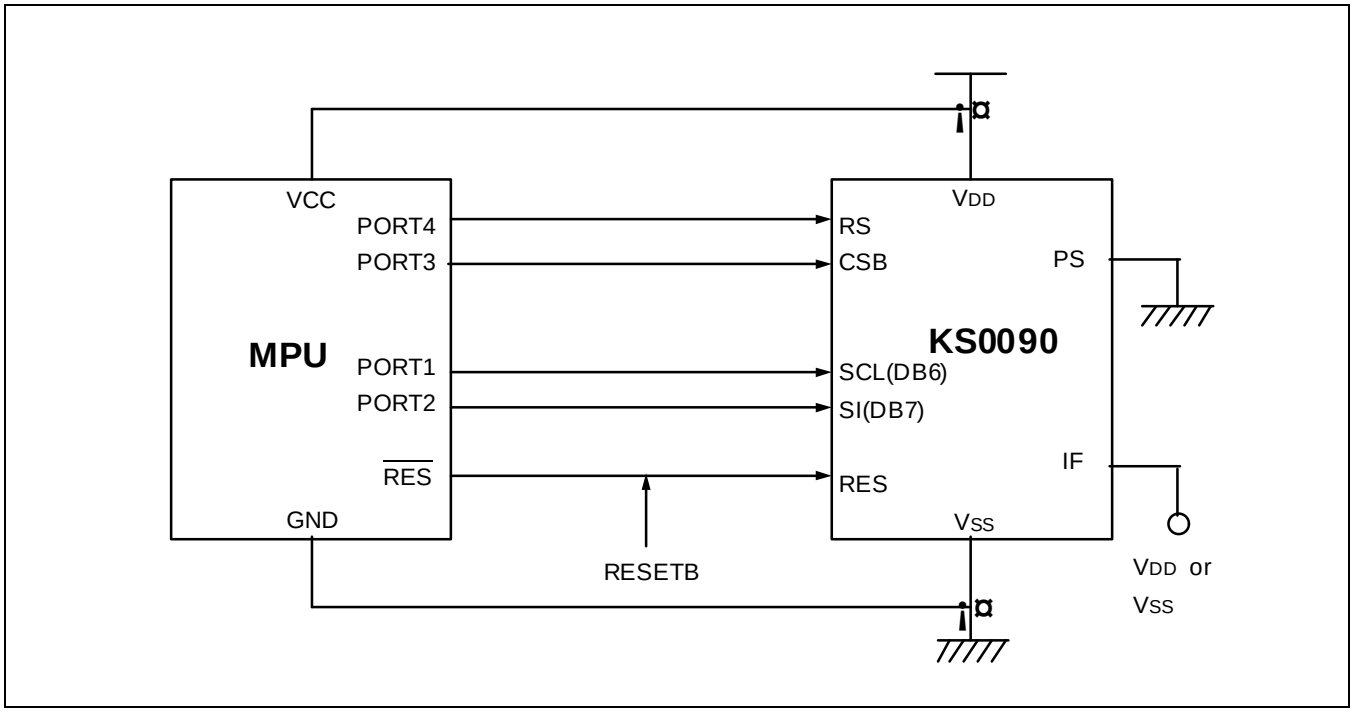


Figure 21. Clock Synchronized Serial Interfacing with Any Microprocessors.

APPLICATION INFORMATION FOR LCD PANEL

CHIP BOTTOM AND LOWER VIEW (S (COM) = “0”, BID (SEG) = “0”)

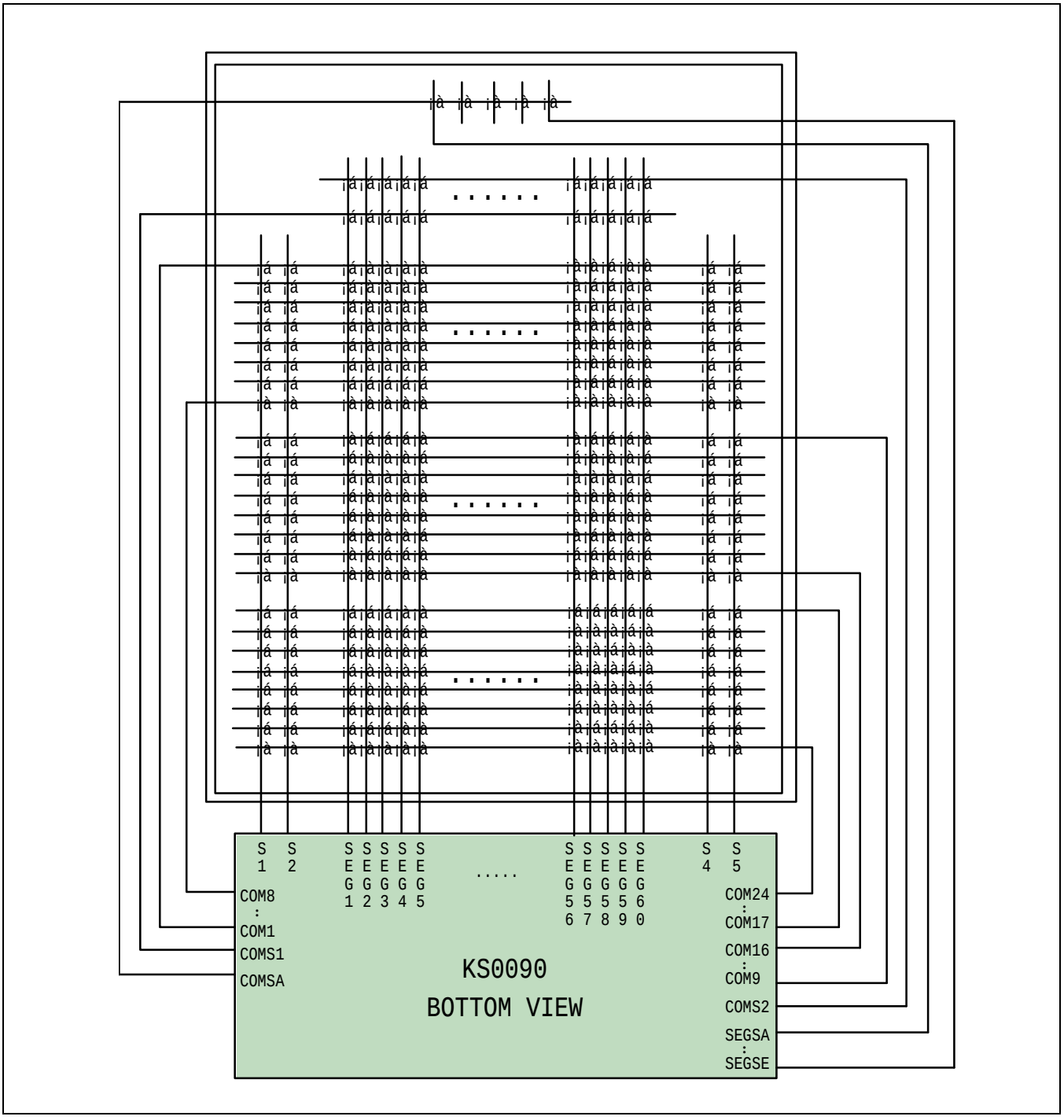


Figure 22.

CHIP BOTTOM & UPPER VIEW (S (COM) = “1”, BID (SEG) = “1”)

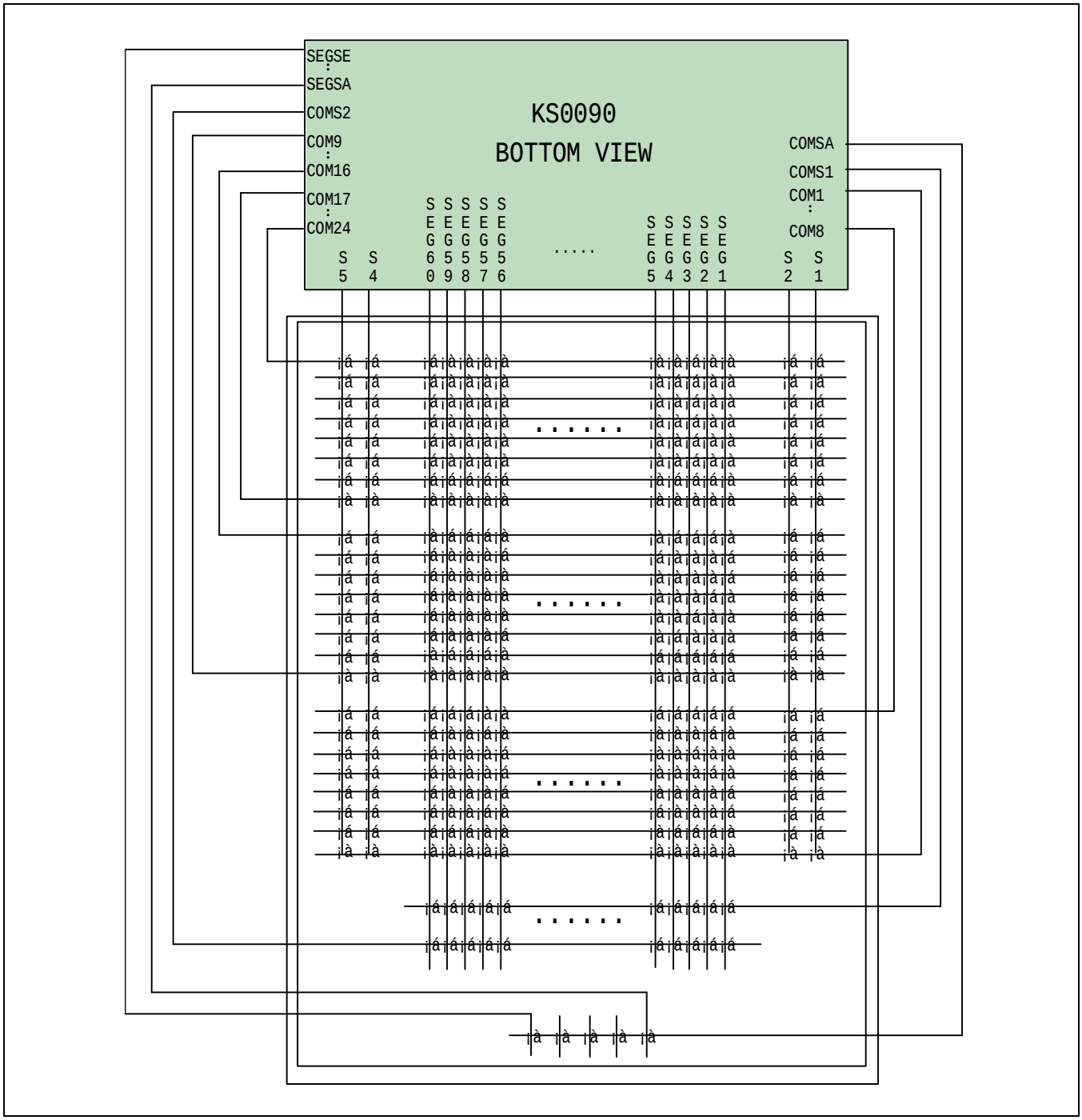


Figure 23.

CHIP TOP & LOWER VIEW (S (COM) = “0”, BID (SEG) = “1”)

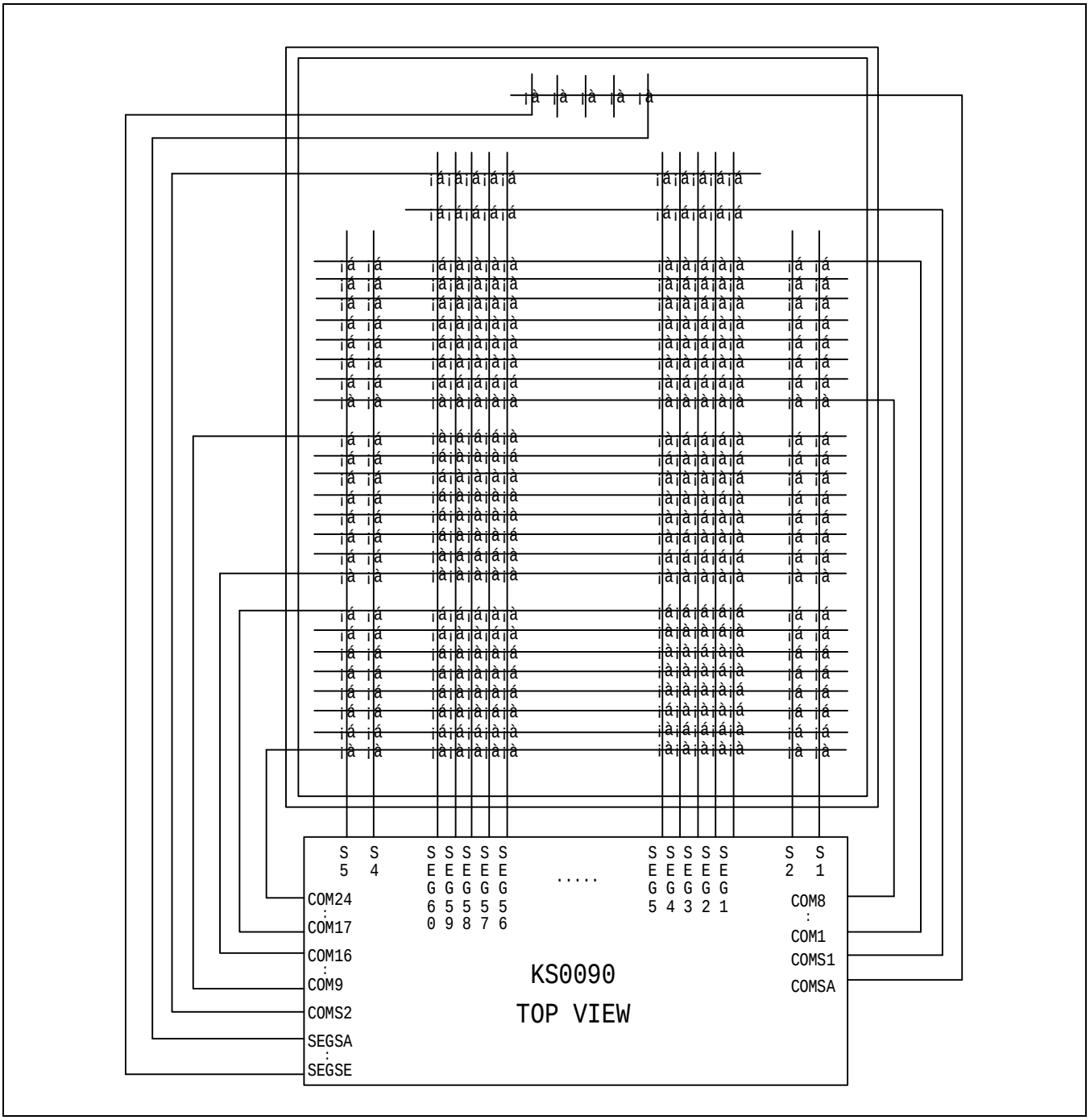


Figure 24.

CHIP TOP & UPPER VIEW (S (COM) = “1”, BID (SEG) = “0”)

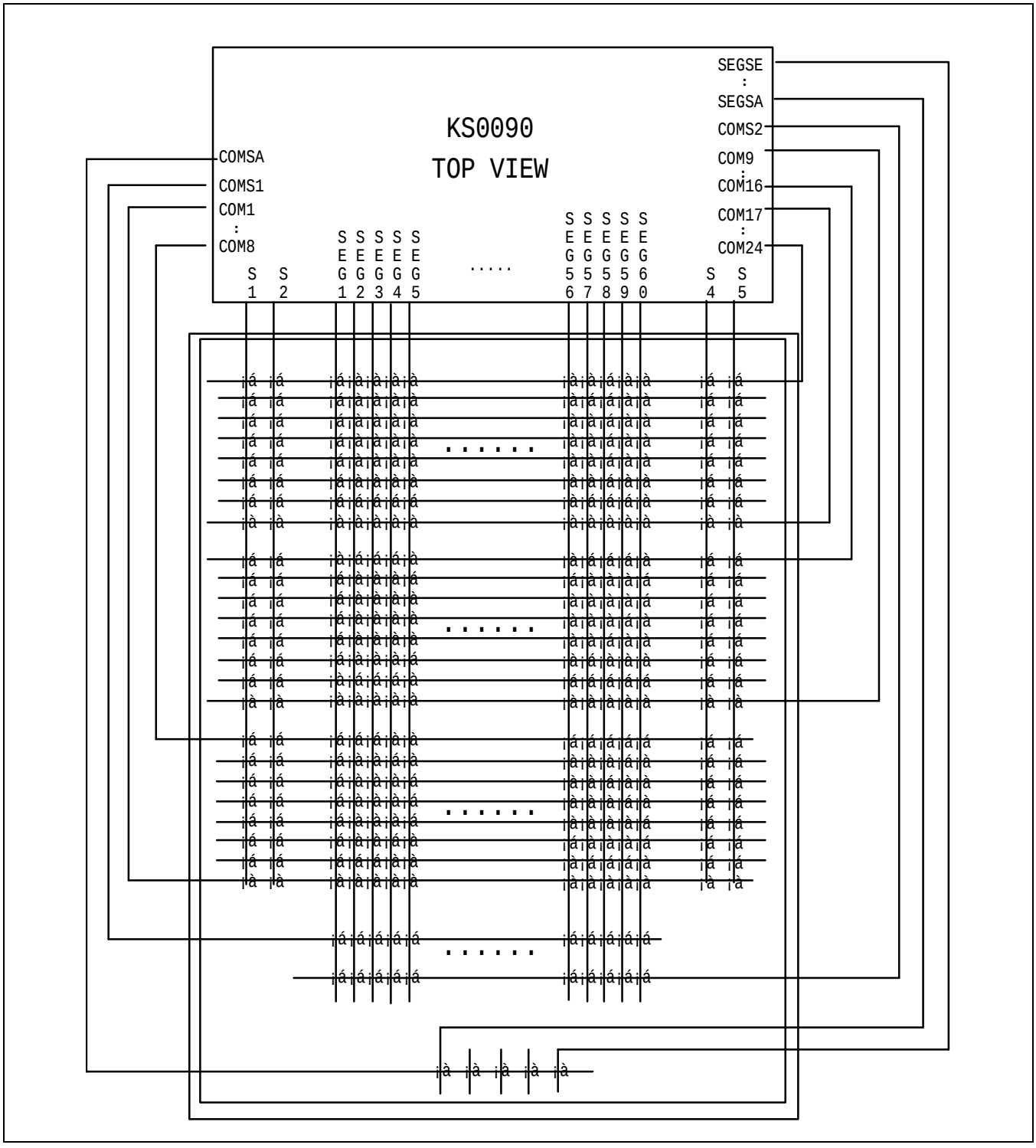
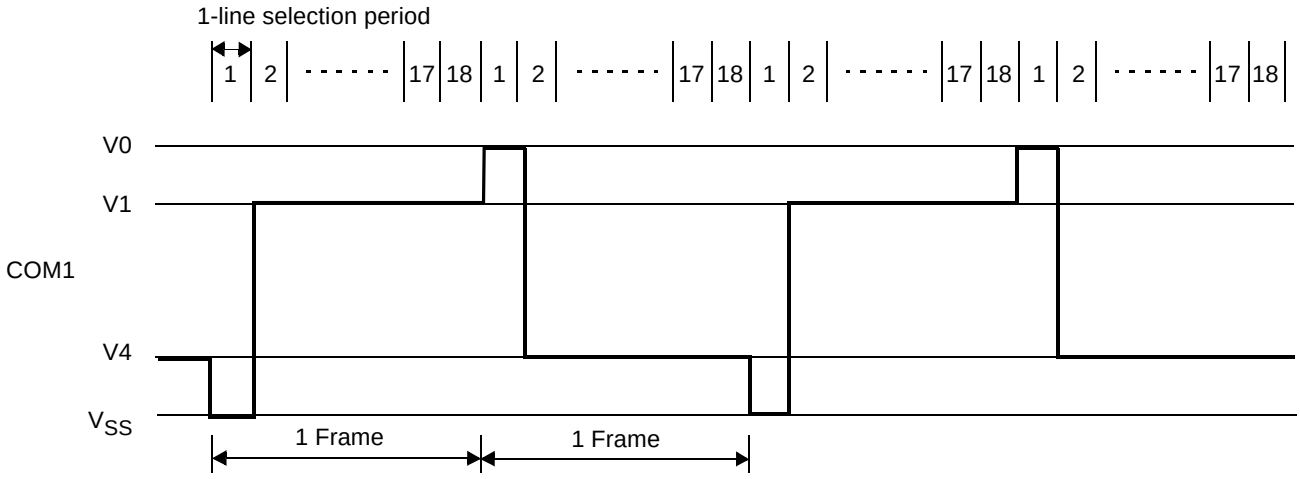


Figure 25.

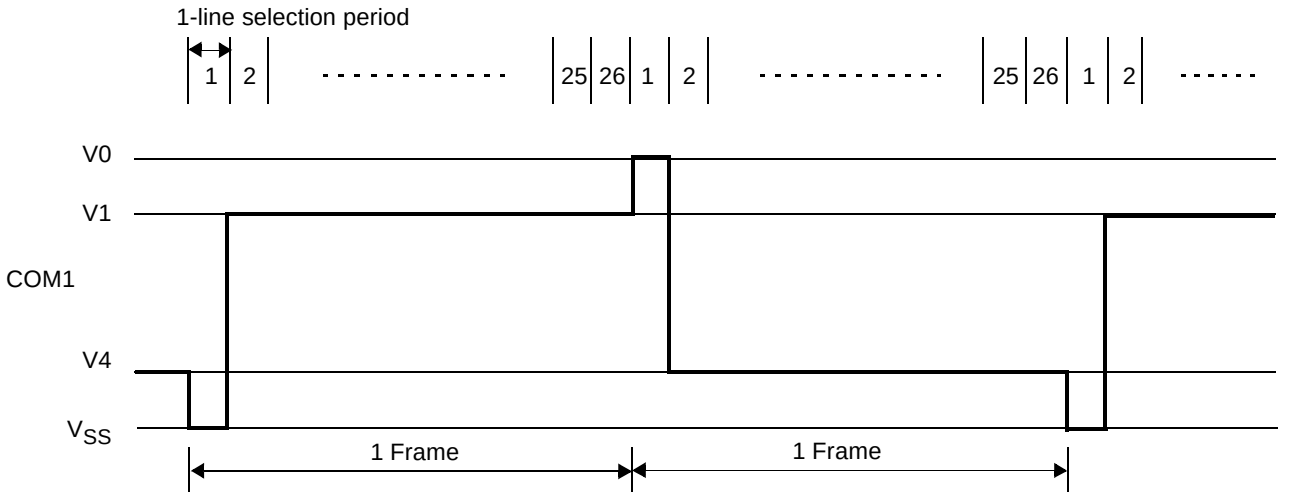
FRAME FREQUENCY

1/18 DUTY (2-LINE MODE)



1-line selection period = 13 clocks
One Frame = 13 × 18 × 43.2 μs = 10.0 ms (1 clock = 43.2 μs at fosc = 23.4 kHz)
Frame frequency = 1/10.0 ms = 100 Hz

1/26 DUTY (3-LINE MODE)



1-line selection period = 13 clocks
One Frame = 13 × 26 × 29.5 μs = 10.0 ms (1 clock = 29.5 μs at fosc = 33.8 kHz)
Frame frequency = 1/10.0 ms = 100 Hz

ABSOLUTE MAXIMUM RATINGS

Table 13. Absolute Maximum Ratings

Characteristics	Symbol	Value	Unit
Power supply voltage (1)	V_{DD}	– 0.3 to + 7.0	V
Power supply voltage (2)	V0, VOUT	– 0.3 to + 13.0	V
Power supply voltage (3)	V1, V2, V3, V4	– 0.3 to V0	V
Operating temperature	T_{OPR}	– 30 to + 85	°C
Storage temperature	T_{STG}	– 55 to + 125	°C

NOTES:

1. Voltage greater than above may damage the circuit
2. All the voltage levels are based on V_{SS} = 0V
3. Voltage level: VOUT ≥ V0 ≥ V_{DD} ≥ V_{SS}
   V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V_{SS}

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

Table 14. DC Characteristics

(V_{DD} = 2.4V to 3.6V, Ta = – 30 to + 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	–	2.4	–	3.6	V
Supply current (V_{DD} = 3V, Ta = 25°C)	I_{DD1}	Display operation, V_{LCD} = 6 V without load No access from MPU	–	–	80	µA
	I_{DD2}	Standby operation without load, Oscillation on, Power off	–	–	10	
	I_{DD3}	Sleep operation without load Oscillation off, Power off	–	–	5	
	I_{DD4}	Access operation from MPU Fcyc=200 kHz	–	–	500	
Input voltage	V_{IH}	–	$0.8V_{DD}$	–	V_{DD}	V
	V_{IL}	–	V_{SS}	–	$0.2V_{DD}$	
Input leakage current	I_{IL}	V_{IN} = 0V to V_{DD}	–1	–	1	µA
R_{ON} resistance	R_{COM}	I_O = ± 50 µA	–	–	5	kΩ
	R_{SEG}	I_O = ± 50 µA	–	–	10	
Frame frequency	f_{FR}	V_{DD} = 3 V, Ta = 25°C	70	100	130	Hz
External clock frequency	f_{CK}	Display of 2-line mode	–	23.4	–	kHz
		Display of 3-line mode	–	33.8	–	
Voltage converter V_{DD} 2 or 3 times	$V_{OUT2/3}$	Ta = 25°C, C1 = 1 µF Without load	95	99	–	%
Voltage regulator reference voltage	V_{REF}	Ta = 25°C	1.94	2.0	2.06	V
LCD driving voltage	V_{LCD}	V_{LCD} = V0 – V_{SS}	4.0	–	11.0	

Table 15. DC Characteristics

(V_{DD} = 3.6V to 5.5V, Ta = – 30 to + 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	–	3.6	–	5.5	V
Supply current (V_{DD} = 5V, Ta = 25°C)	I_{DD1}	Display operation, V_{LCD} = 6 V without load No access from MPU	–	–	100	µA
	I_{DD2}	Standby operation without load, Oscillation on, Power off	–	–	20	
	I_{DD3}	Sleep operation without load Oscillation off, Power off	–	–	10	
	I_{DD4}	Access operation from MPU Fcyc=200 kHz	–	–	1000	
Input voltage	V_{IH}	–	$0.8V_{DD}$	–	V_{DD}	V
	V_{IL}	–	V_{SS}	–	$0.2V_{DD}$	
Input leakage current	I_{IL}	V_{IN} = 0V to V_{DD}	–1	–	1	µA
R_{ON} resistance	R_{COM}	I_O = ± 50 µA	–	–	5	kΩ
	R_{SEG}	I_O = ± 50 µA	–	–	10	
Frame frequency	f_{FR}	V_{DD} = 5V, Ta = 25°C	70	100	130	Hz
External clock frequency	f_{CK}	Display of 2-line mode	–	23.4	–	kHz
		Display of 3-line mode	–	33.8	–	
Voltage converter V_{DD} 2 times	V_{OUT2}	Ta = 25°C, C1 = 1 µF Without load	95	99	–	%
Voltage regulator reference voltage	V_{REF}	Ta = 25°C	1.94	2.0	2.06	V
LCD driving voltage	V_{LCD}	V_{LCD} = V0 – V_{SS}	4.0	–	11.0	

NOTE: When power supply (V_{DD}) range is 3.6 V to 5.5 V, the boosting of the voltage converter is only available 2 times.

AC CHARACTERISTICS

Write Bus Mode (68 Mode)

(V_{DD} = 2.4V to 3.6V, Ta = – 30 to + 85°C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write bus mode	E cycle time	t_C	650	–	-	ns
	Pulse rise / fall time	t_R, t_F	-	–	25	
	E pulse width high	t_{WH}	450	–	–	
	E pulse width low	t_{WL}	150	–	–	
	RS and CSB setup time	t_{SU1}	60	–	–	
	RS and CSB hold time	t_{H1}	30	–	–	
	DB setup time	t_{SU2}	100	–	–	
	DB hold time	t_{H2}	50	–	–	

(V_{DD} = 2.7V to 3.3V, Ta = – 30 to + 85°C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write bus mode	E cycle time	t_C	500	–	–	ns
	Pulse rise / fall time	t_R, t_F	–	–	25	
	E pulse width high	t_{WH}	350	–	–	
	E pulse width low	t_{WL}	100	–	–	
	RS and CSB setup time	t_{SU1}	60	–	–	
	RS and CSB hold time	t_{H1}	10	–	–	
	DB setup time	t_{SU2}	100	–	–	
	DB hold time	t_{H2}	20	–	–	

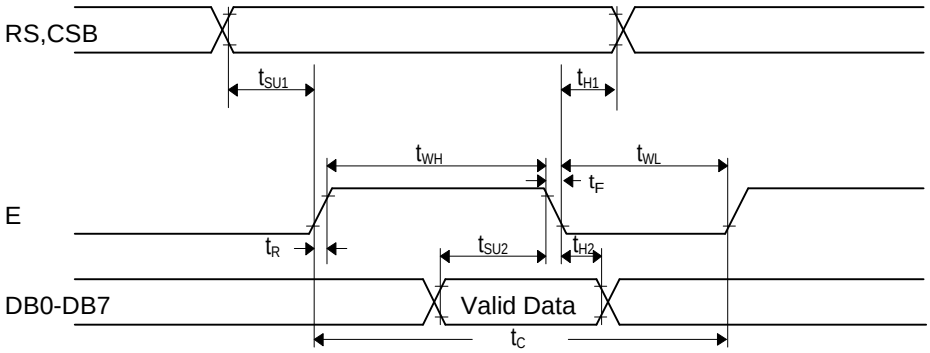


Figure 26. Write Bus Mode Timing Diagram (68 Mode)

Write Bus Mode (80 Mode)

(V_{DD} = 2.4 to 3.6V, Ta = – 30 to + 85°C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write bus mode	E cycle time	t_C	650	–	–	ns
	Pulse rise / fall time	t_R, t_F	–	–	25	
	E pulse width high	t_{WH}	150	–	–	
	E pulse width low	t_{WL}	450	–	–	
	RS and CSB setup time	t_{SU1}	60	–	–	
	RS and CSB hold time	t_{H1}	30	–	–	
	DB setup time	t_{SU2}	100	–	–	
	DB hold time	t_{H2}	50	–	–	

(V_{DD} = 3.6V to 5.5V, Ta = – 30 to + 85°C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write bus mode	E cycle time	t_C	500	–	–	ns
	Pulse rise / fall time	t_R, t_F	–	–	25	
	E pulse width high	t_{WH}	100	–	–	
	E pulse width low	t_{WL}	350	–	–	
	RS and CSB setup time	t_{SU1}	60	–	–	
	RS and CSB hold time	t_{H1}	10	–	–	
	DB setup time	t_{SU2}	100	–	–	
	DB hold time	t_{H2}	20	–	–	

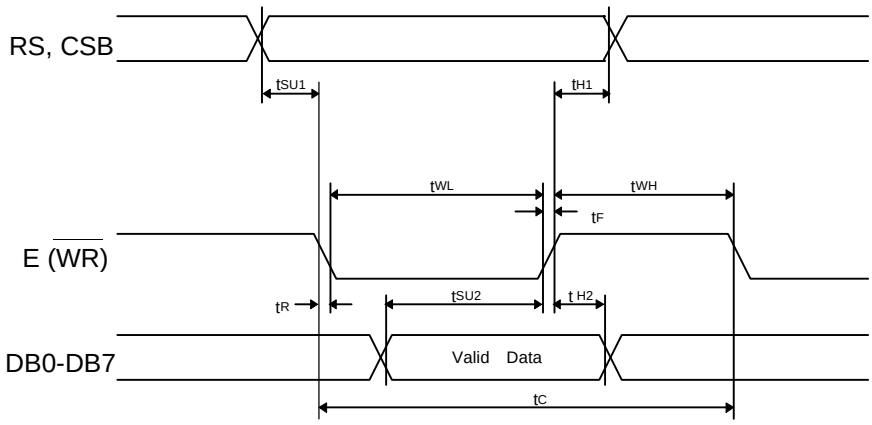


Figure 27. Write Bus Mode Timing Diagram (80 Mode)

Clock Synchronized Serial Mode

(V_{DD} = 2.4V to 3.6V, Ta = – 30 to + 85°C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Clock Synchronized Serial Interface Mode	SCL clock cycle time	t_C	1000	–	–	ns
	Pulse rise / fall time	t_R, t_F	–	–	25	
	SCL clock width (High, Low)	t_W	300	–	–	
	CSB setup time	t_{SU1}	150	–	–	
	CSB hold time	t_{H1}	700	–	–	
	RS data setup time	t_{SU2}	50	–	–	
	RS data hold time	t_{H2}	300	–	–	
	SI data setup time	t_{SU3}	50	–	–	
	SI data hold time	t_{H3}	50	–	–	

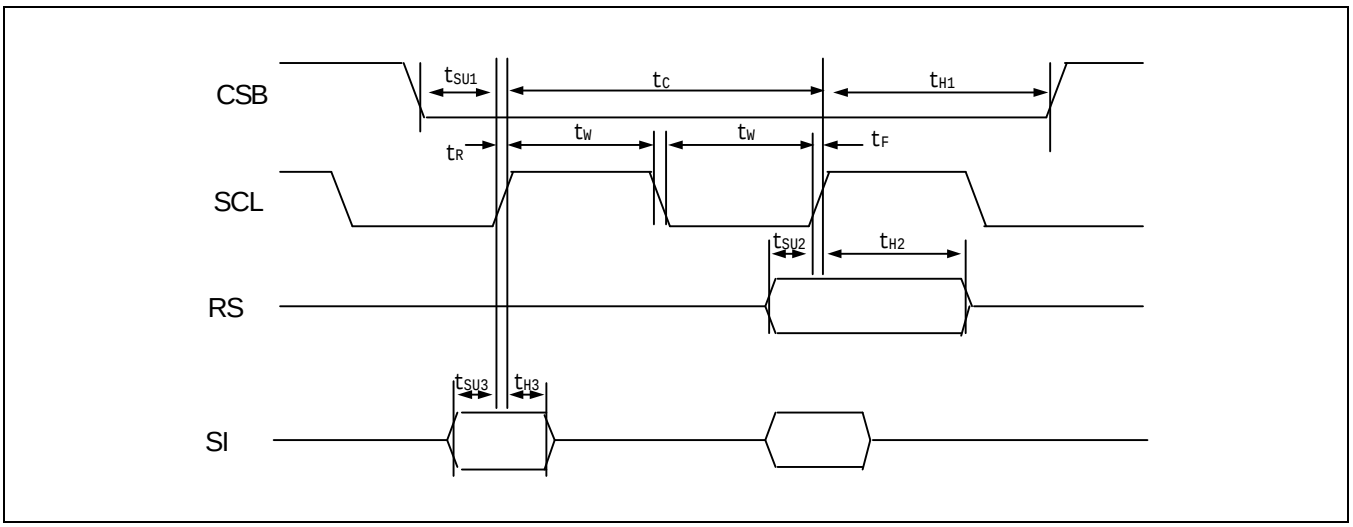


Figure 28. Clock Synchronized Serial Interface Mode Timing Diagram

Write Bus And Serial Mode (typical 5V)

68 Bus Mode

(V_{DD} = 3.6 to 5.5V, Ta = – 30 to + 85°C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write bus mode	E cycle time	t_C	350	–	–	ns
	Pulse rise / fall time	t_R, t_F	–	–	25	
	E pulse width high	t_{WH}	250	–	–	
	E pulse width low	t_{WL}	100	–	–	
	RS and CSB setup time	t_{SU1}	40	–	–	
	RS and CSB hold time	t_{H1}	10	–	–	
	DB setup time	t_{SU2}	40	–	–	
	DB hold time	t_{H2}	10	–	–	

80 Bus Mode

(V_{DD} = 3.6V to 5.5V, Ta = – 30 to + 85°C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write bus mode	E cycle time	t_C	350	–	-	ns
	Pulse rise / fall time	t_R, t_F	-	–	25	
	E pulse width high	t_{WH}	100	–	–	
	E pulse width low	t_{WL}	250	–	–	
	RS and CSB setup time	t_{SU1}	40	–	–	
	RS and CSB hold time	t_{H1}	10	–	–	
	DB setup time	t_{SU2}	40	–	–	
	DB hold time	t_{H2}	10	–	–	

Serial Mode

(V_{DD} = 3.6V to 5.5V, Ta = – 30 to + 85°C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Clock Synchronized Serial Interface Mode	SCL clock cycle time	t_C	600	–	–	ns
	Pulse rise / fall time	t_R, t_F	–	–	25	
	SCL clock width (High, Low)	t_W	200	–	–	
	CSB setup time	t_{SU1}	100	–	–	
	CSB hold time	t_{H1}	400	–	–	
	RS data setup time	t_{SU2}	40	–	–	
	RS data hold time	t_{H2}	200	–	–	
	SI data setup time	t_{SU3}	40	–	–	
	SI data hold time	t_{H3}	40	–	–	