DIGITAL VIDEO ENCODER

The KS0123 multi-standard video encoder converts CCIR 656 8-bit multiplexed digital component video into analog baseband signals. It outputs composite video (CVBS) and S-Video simultaneously at three analog output pins.

The encoder implements Macrovision revision 6.0 anti-taping scheme. Additionally, it contains a color subcarrier genlock to support analog/digital video splicing.

The video outputs conform to either SMPTE 170M (NTSC) or CCIR 624 (PAL) standards.

44 PLCC

ORDERING INFORMATION

Device	Package	Temperature Range
KS0123	44 PLCC	0°~+70°C

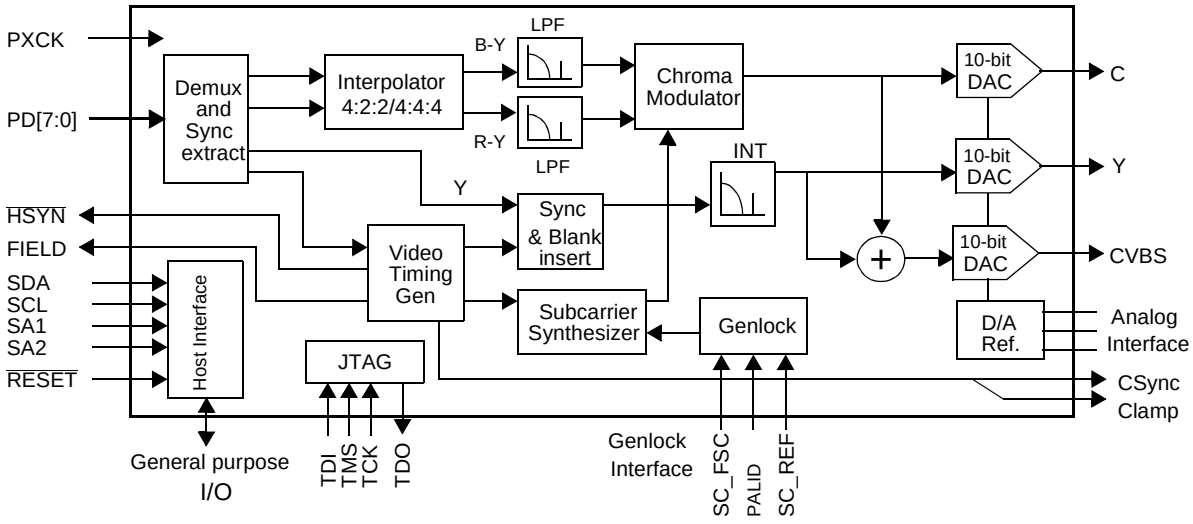
FEATURES

- **Macrovision revision 6.0 anti-taping support**
- **8-bit parallel CCIR 656 CbYCr input format**
- **Synchronizes to CCIR 656 AVE time reference codes for horizontal and vertical timing generation in *slave mode* operation**
- **Generates HSYN and FIELD signals in *master mode* operation**
- **Programmable subcarrier frequency, SCH phase, and synchronous field display to support MPEG II picture-coding-extension**
- **Optional subcarrier genlock to analog f_{sc_ref} reference**
- **650 kHz or 1.3 MHz chrominance bandwidth selection**
- **Support NTSC, PAL, PAL-M and PAL-N**
- **Switchable pedestal with gain compensation**
- **Selectable 37 nsec YC delay pre-compensation**
- **Video outputs meet SMPTE 170M or CCIR 624 spec**
- **27 MHz DAC conversion rate**
- **Triple 10-bit DAC's for simultaneous S-video and composite output**
- **2 -wire serial host interface**
- **8 general purpose I/O pins**
- **JTAG test interface**
- **Single 5 V supply with power down mode**
- **44-pin PLCC package**

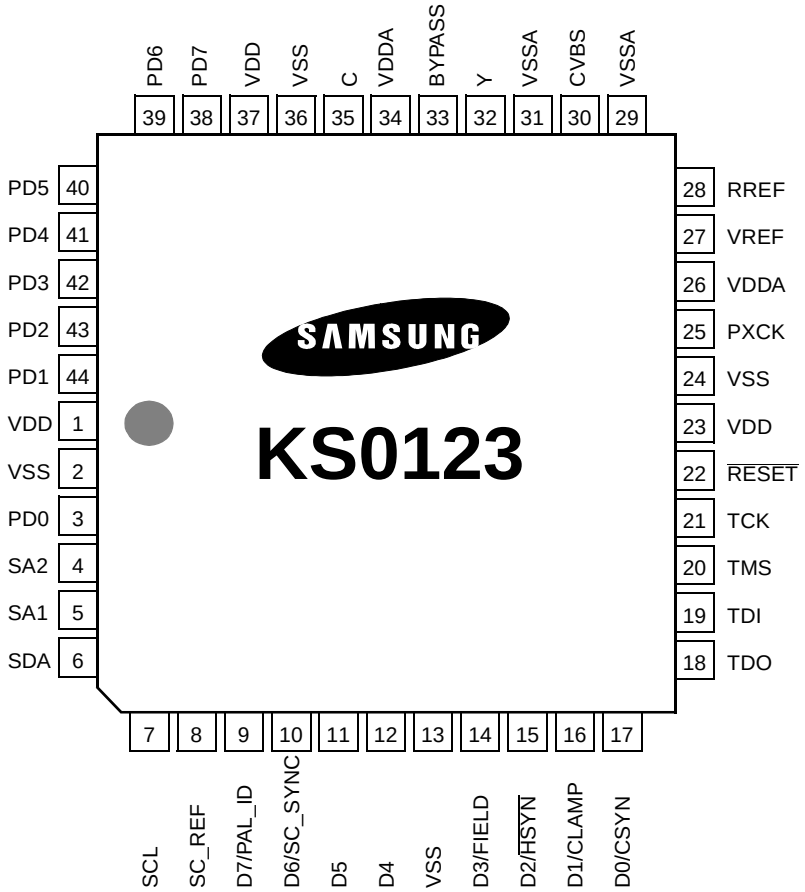
Application

- **Settop Box Video Encoding**
- **MPEG Playback**
- **Multimedia**

BLOCK DIAGRAM



PIN ASSIGNMENT - 44 PLCC



TYPICAL APPLICATION

The Encoder is shown in a typical settop box application.

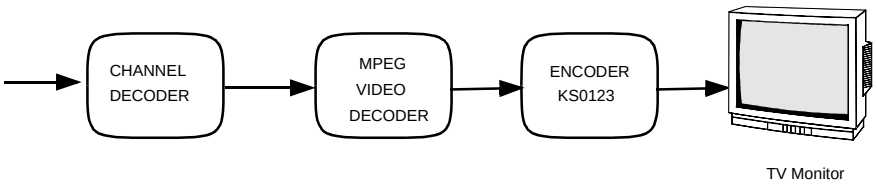


Figure 1. Typical Application

PIN DESCRIPTION

Pin Name	Pin #	Type	Description
CLOCK INPUT			
PXCK	25	I	27 MHz clock input. TTL/CMOS.
PIXEL DATA PORT			
PD7 - PD0	38-44, 3	I	Pixel data inputs. TTL/CMOS.
GENERAL PURPOSE PORT AND OTHER SIGNALS			
SC_REF	8	I	Subcarrier reference input. TTL.
D7/PAL_ID	9	I/O	General Purpose I/O Port 7 or PAL_ID input. TTL/CMOS.
D6/SC_SYNC	10	I/O	General Purpose I/O Port 6 or SC_SYNC input. TTL/CMOS.
D5	11	I/O	General Purpose I/O Port 5. TTL/CMOS.
D4	12	I/O	General Purpose I/O Port 4. TTL/CMOS.
D3/FIELD	14	I/O	General Purpose I/O Port 3 or FIELD output. TTL/CMOS.
D2/$\overline{\text{HSYN}}$	15	I/O	General Purpose I/O Port 2 or $\overline{\text{HSYN}}$ output. TTL/CMOS.
D1/CLAMP	16	I/O	General Purpose I/O Port 1 or CLAMP output. TTL/CMOS.
D0/CSYN	17	I/O	General Purpose I/O Port 0 or CSYN output. TTL/CMOS.
SERIAL MICROPROCESSOR PORT			
SDA	6	I/O	Serial data I/O. Open drain.
SCL	7	I	Serial clock input.
SA1	5	I	Slave address select. TTL.
SA2	4	I	Slave address select. TTL.
RESET			
$\overline{\text{RESET}}$	22	I	Master reset input. TTL.
VIDEO OUTPUTS			
CVBS	30	O	Composite video output.
Y	32	O	Luminance output.
C	35	O	Chrominance output.
DAC REFERENCE AND COMPENSATION			
VREF	27	I/O	Voltage reference I/O. Connect a 0.1 µF capacitor to VSSA.
BYPASS	33	I/O	Compensation capacitor. Connect a 0.1 µF capacitor to VDDA.
RREF	28	I/O	Current setting resistor.

PIN DESCRIPTION (Continued)

Pin Name	Pin #	Type	Description
JTAG PORT			
TDI	19	I	Data input port. TTL.
TMS	20	I	Scan select input. TTL.
TCK	21	I	Scan clock input. TTL.
TDO	18	O	Data output port. CMOS.
POWER			
VDD	1,23,37	+5V	Digital power supply.
VDDA	26,34	+5V	Analog power supply.
GROUND			
VSS	2,13,24,36	0V	Digital ground.
VSSA	29,31	0V	Analog ground.

PIN CROSS REFERENCE

Numerical Order by Pin Number

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	VDD	12	D4	23	VDD	34	VDDA
2	VSS	13	VSS	24	VSS	35	C
3	PD0	14	D3/FIELD	25	PXCK	36	VSS
4	SA2	15	D2/$\overline{\text{HSYN}}$	26	VDDA	37	VDD
5	SA1	16	D1	27	VREF	38	PD7
6	SDA	17	D0	28	RREF	39	PD6
7	SCL	18	TD0	29	VSSA	40	PD5
8	SC_REF	19	TD1	30	CVBS	41	PD4
9	D7/PAL_ID	20	TMS	31	VSSA	42	PD3
10	D6/SC_SYNC	21	TCK	32	Y	43	PD2
11	D5	22	$\overline{\text{RESET}}$	33	BYPASS	44	PD1

Alphabetical Order by Pin Name

Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #
BYPASS	33	PD0	3	SA1	5	VDD	37
C	35	PD1	44	SA2	6	VDDA	26
CVBS	30	PD2	43	SCL	7	VDDA	34
D0	17	PD3	42	SC_REF	8	VREF	27
D1	16	PD4	41	SDA	6	VSS	2
D2/$\overline{\text{HSYN}}$	15	PD5	40	TCK	21	VSS	13
D3/FIELD	14	PD6	39	TDI	19	VSS	24
D4	12	PD7	38	TDO	18	VSS	36
D5	11	PXCK	25	TMS	20	VSSA	29
D6/SC_SYNC	10	$\overline{\text{RESET}}$	22	VDD	1	VSSA	31
D7/PAL_ID	9	RREF	28	VDD	23	Y	32

GENERAL DESCRIPTION

The encoder accepts 27 MHz 8-bit multiplexed digital component video in CCIR 656 CbYCr format at the Pixel Data (PD) port. The pixel data are demultiplexed into luminance and chrominance components for interpolation and low pass filtering to reduce cross luma/chroma interference. The filtered chrominance signals are modulated onto a color subcarrier and added to the processed luminance components to form the composite video (CVBS). The digital CVBS and S-Video signals are interpolated to 27 MHz rate and then converted to analog forms by 3 10-bit D/A converters.

Anti-taping pulses, synch signals and color burst are generated internally. The rise and fall times of those pulses are controlled to reduce ringing. The shaped signals are inserted into the video stream controlled by the timing generator.

The encoder also contains a color subcarrier PLL, which when enabled will frequency and phase lock the color subcarrier to an external analog fsc or 4 x fsc reference. The SCH phase can be adjusted to compensate for additional external phase delay.

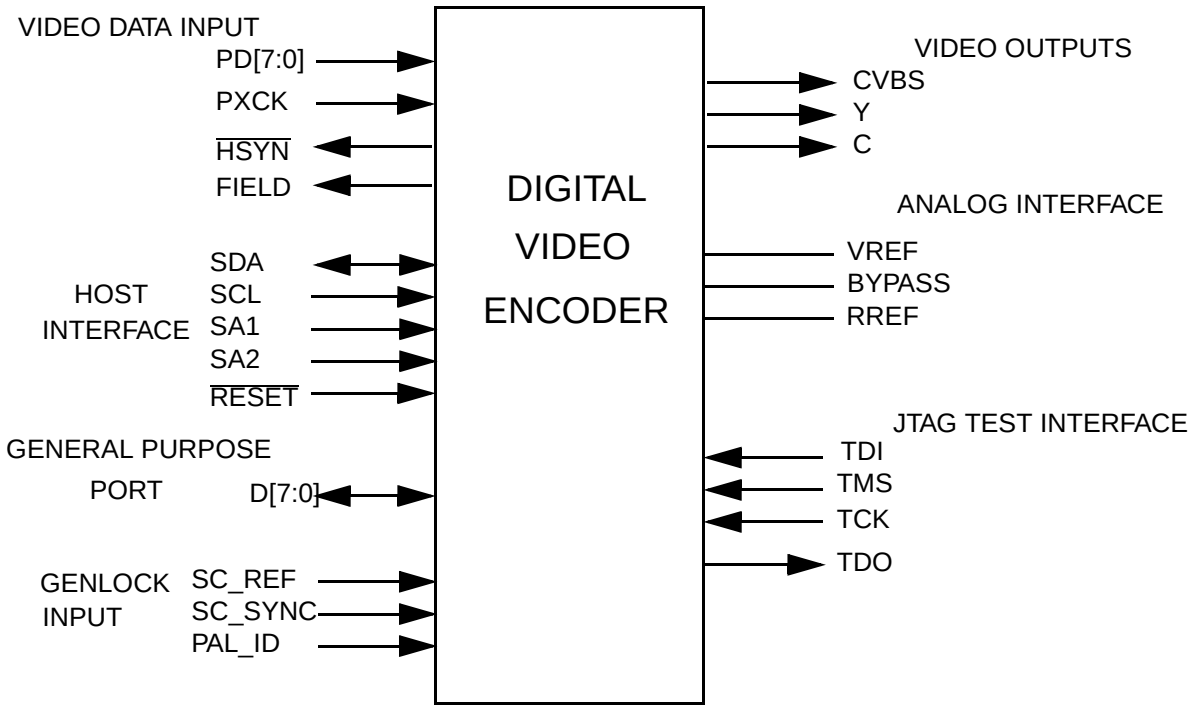


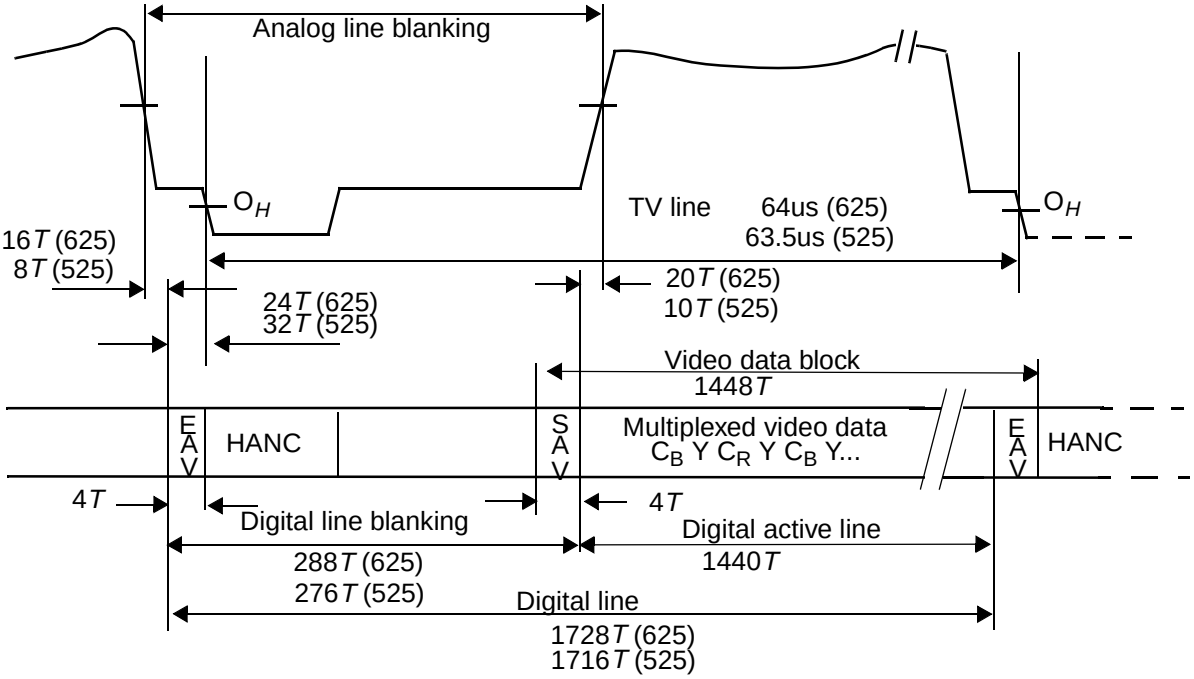
Figure 2. Logic Diagram

DIGITAL VIDEO INPUT FORMAT

Video data enters the encoder on pins PD[7:0]. The encoder accepts and processes digital video data in accordance with **CCIR 656** and **CCIR 601** standards. The input data are 8 bit multiplexed CbYCr component video, encoded in the 4:2:2 format. The input bit stream may contain End of Active Video (EAV) and Horizontal Ancillary Control (HANC) codes. The relationships of the digital video with analog timing are show in Figure 3.

CCIR 656 Timing Relationship Between Video Data and The Analog Sync Waveform

The digital active line begins at 244 words (in the 525-line standard) or at 264 words (in the 625-line standard) after the leading edge of the analog line synchronization pulse, this time being specified between half-amplitude points.



T: clock period 37ns nom.
SAV: start of active video timing ref. code
EAV: end of active video timing ref. code
HANC: horizontal ancillary data

Figure 3. 656 Data Format and Timing Relationship

Timing Reference Codes

Each video line can have two timing reference codes, one at the beginning of the data block (start of active video **SAV**) and one at the end (end of active video **EAV**) as shown in Figure 3. Each timing reference code consists of a four byte sequence in the form FF, 00, 00 and XX as shown in Table 1. The first three words are fixed, the fourth byte contains field and line blanking information.

Table 1: Video Timing Reference Codes

Bit #	7(MSB)	6	5	4	3	2	1	0(LSB)	HEX
First	1	1	1	1	1	1	1	1	FF
Second	0	0	0	0	0	0	0	0	00
Third	0	0	0	0	0	0	0	0	00
Fourth	1	F	V	H	P_3	P_2	P_1	P_0	XX

Notes:
F = 0 during field 1
1 during field 2

V = 0 elsewhere
1 during field blanking

H = 0 in SAV
1 in EAV

P_3 - - P_0: Protection bits (not used by the encoder)

The encoder decodes the video timing reference code that indicates the end of active video (EAV). The EAV code shall contain the **F** (field) and **V** (blanking) bits as specified in CCIR 656. This information applies to the following video line. The encoder *ignores* the start of active video (SAV) timing code.

The encoder uses the F bit for synchronization purposes. The transition of F bit is used to indicate the start of a new field. The polarity is also used to indicate odd and even. Additional field information is supplied by the ancillary data.

The V bit is not used for synchronization. A V of ‘1’ indicates line blanking. Certain lines and half lines are blanked regardless of the state of the V bit. In general if the V bit is high, then the encoder blanks the line (Figure 10 and Figure 11).

Horizontal Ancillary Data Sequence (HANC)

The ancillary data contains additional timing information about the following video line. Table 2 shows the sequence of the ancillary data. The HANC data, if present, should immediately follow the EAV code. The encoder decodes the ancillary data if the ancillary data type code (TT) matches the data ID code stored in the internal ANCDID register (index 07h).

The LSB of the ancillary data is a parity bit. The video encoder assumes that the data is error free and *always ignores* this bit.

Table 2: Ancillary Data Sequence

Word ID	Description	B7	B6	B5	B4	B3	B2	B1	B0
ANC(2)	Ancillary Data Header	0	0	0	0	0	0	0	0
ANC(1)		1	1	1	1	1	1	1	1
ANC(0)		1	1	1	1	1	1	1	1
TT	Data Type	TT6	TT5	TT4	TT3	TT2	TT1	TT0	P
	Reserved	(R)	(R)	(R)	(R)	(R)	(R)	(R)	P
		(R)	(R)	(R)	(R)	(R)	(R)	(R)	P
FIELD	Field number and synchronous video flag	(R)	(R)	(R)	SVF/	F2	F1	F0	P
PH(1)	Subcarrier Instantaneous Phase	PHV	PH12	PH11	PH10	PH9	PH8	PH7	P
PH(0)		PH6	PH5	PH4	PH3	PH2	PH1	PH0	P
FR(4)	Subcarrier Frequency	FRV	(R)	(R)	FR31	FR30	FR29	FR28	P
FR(3)		FR27	FR26	FR25	FR24	FR23	FR22	FR21	P
FR(2)		FR20	FR19	FR18	FR17	FR16	FR15	FR14	P
FR(1)		FR13	FR12	FR11	FR10	FR9	FR8	FR7	P
FR(0)		FR6	FR5	FR4	FR3	FR2	FR1	FR0	P

Note: 1. P = odd parity bit
2. R = reserved bit; ignored by video encoder

The **ancillary data header** (ANC) consists of three bytes which indicate the start of the ancillary data. This is in accordance with CCIR 656.

The **data type** code is used to specify the ancillary data type. The encoder compares this value with the value programmed into the ANCDID register. If the two match, the encoder will process the ancillary data, otherwise the encoder will ignore the ancillary data.

The **field number** bits are used by the encoder to program the field counter. The field number will be loaded to the counter if SVF/ is low and the ancillary timing reference enable (ATMEN) bit is ‘1’.

The **subcarrier instantaneous phase** is a 13-bit integer which defines the phase of the reference subcarrier at the synch tip. The subcarrier frequency synthesizer *phase* will be reset to this number at the synch tip when both HANC datum PHV and control register APHEN are '1's.

Table 3: Definition of Subcarrier Instantaneous Phase

subcarrier phase #	phase value
0	([360^0 / 8192]) * 0
1	([360^0 / 8192]) * 1
...	...
8191	([360^0 / 8192]) * 8191

The MPEG II system allows the 27 MHz clock frequency to vary to prevent the input buffer from overflow or underflow. When this happens the color subcarrier frequency will shift if the addend of numerical oscillator is not adjusted accordingly. If control register bit AFREN is '1' the subcarrier synthersizer will select the latched HANC's **subcarrier frequency** data (**FR**) as the addend instead of the programmable register (0x8-0xb) (Figure 6). The FR is latched if HANC datum **FRV** = '1'. and the HANC control register's AFREN bit is set. The FR's value should be calculated using the equation

$$FR = NINT\left(2^{32} \bullet \frac{Fsc}{Ck}\right)$$

where Fsc is the desired color subcarrier frequency,
Ck is the clock frequency,
and NINT is the nearest integer.

VIDEO ENCODING

The incoming digital video are gain and offset adjusted according to the output format, NTSC or PAL, controlled by the format register. Both the luminance and chrominance are band limited and interpolated to 27 MHz sampling rate for digital to analog conversion. The NTSC output can be selected to include a 7.5 IRE **pedestal**. The user can also select either 650 kHz or 1.35 MHz **chrominance bandwidth**. The U and V components have equal bandwidth.

Luminance Filter

The luminance signal is band-limited to 6 MHz. The filter is implemented with a 15 tap linear phase FIR filter. Figure 4 shows the frequency responses.

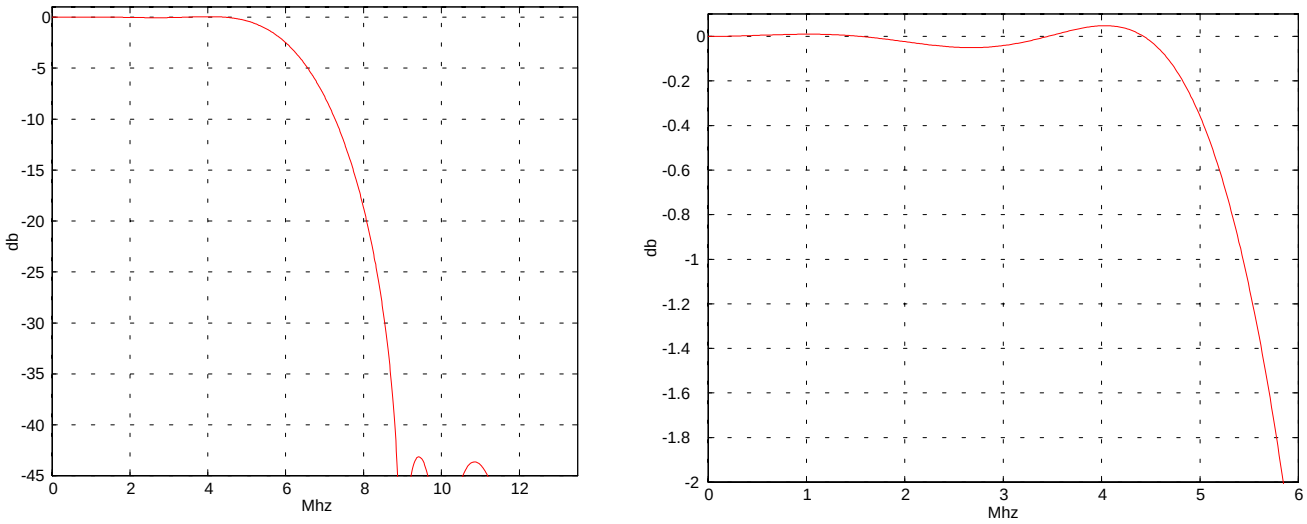
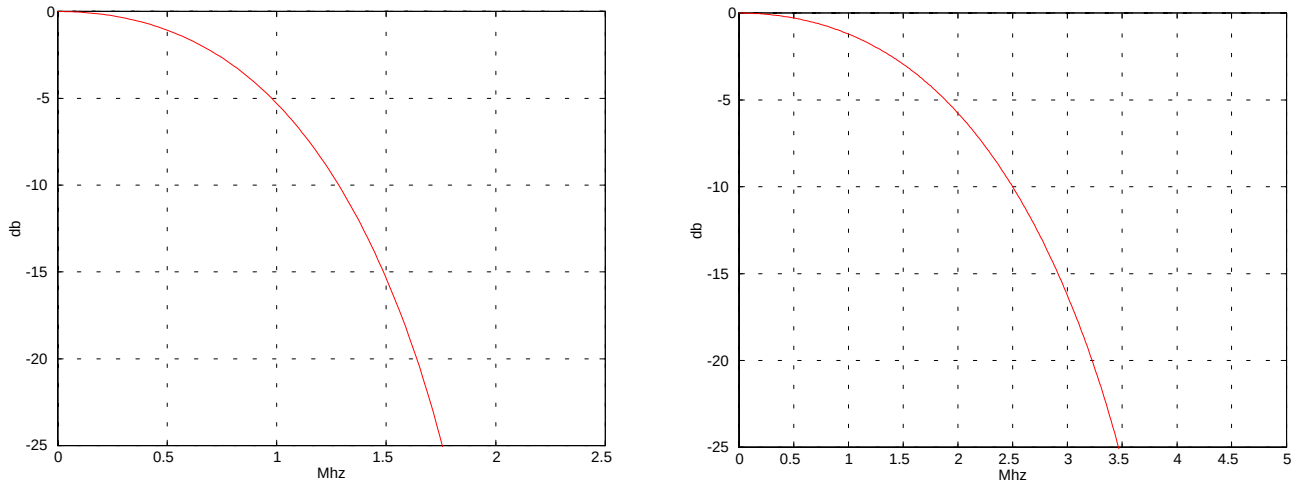


Figure 4. Luminance Filter Frequency Response

Chrominance Filter

Figure 6 shows the chrominance frequency response for different bandwidth selections.



CHRBW = ‘0’ CHRBW = ‘1’

Figure 5. Chrominance Filter Frequency Response

COLOR SUBCARRIER GENERATION

The chrominance signals are modulated onto a subcarrier. The nominal subcarrier frequency is determined by 4 registers (08h - 0Bh). The subcarrier generation also contains Subcarrier Horizontal Synch Phase, SCH, offset control (Reg 0Ch - 0Dh), and genlock functions to support digital/analog video multiplexing.

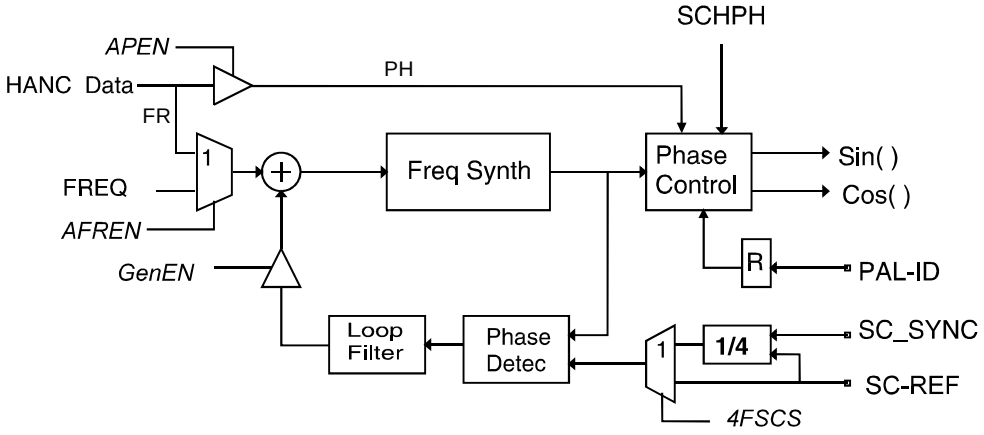


Figure 6. Fsc Synthersizer

The color subcarrier synthesizer can operate in 3 modes: (a) free running mode, (b) HANC genlock mode, and (c) analog genlock mode.

(a). In the **free running mode** the color subcarrier frequency is programmed via the host interface. The 4 field or 8 field SCH phase are maintained. The nominal frequency register values for different video standards are listed in Table 4.

Table 4: Register Values for Subcarrier Frequencies

Standard	Subcarrier Frequency(MHz)	Frequency Register			
		FREQD	FREQC	FREQB	FREQA
NTSC	3.57954545	43	E0	F8	3E
PAL-B,G,H,I	4.43361875	54	13	15	96
PAL-M	3.57561189	43	CD	DF	C7
PAL-N	3.58205625	43	ED	28	8D

(b). In the **HANC genlock mode** the subcarrier frequency, FR, and instantaneous phase, PH, information are sent to the encoder via the HANC data. The frequency and phase values are updated during the synch tip.

(c). If **analog genlock mode** is selected the subcarrier synthesizer is locked to an external reference signal, fsc or 4 fsc. An external PAL_ID signal is required to control the PAL phase alternation. The PLL has 2 kHz pull in range.

Analog Genlock Circuit

The analog genlock circuit will lock the frequency and phase of the subcarrier synthesizer to an external reference signal. To activate the genlock circuit, first program the nominal FREQD-A value then set GENEN = 1.The external

reference signal is applied to the SC_REF input pin. The frequency of this squarewave is either Fsc or 4*Fsc (program the 4FSCS bit accordingly). When using a 4*Fsc input, the SC_SYNC resets the internal divider's phase to the 0 count state as shown in Figure 7. The **SCHM** and **SCHL** registers can be programmed to compensate for the propagation delay from the phase detector input to the DAC output.

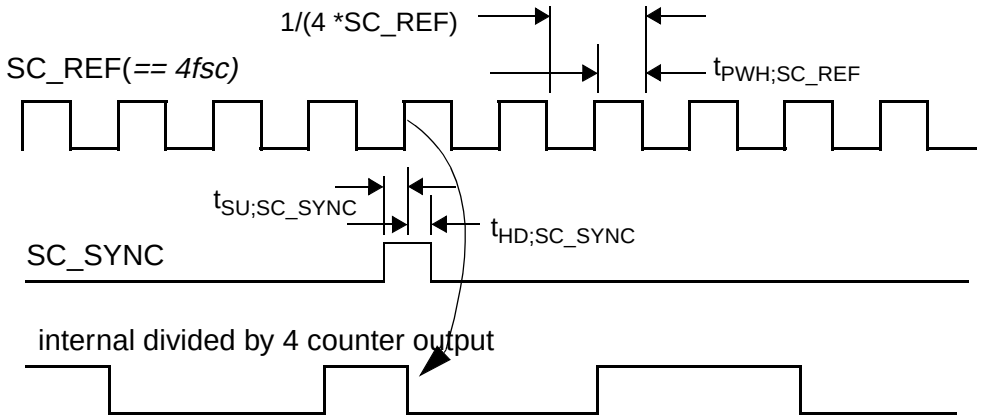


Figure 7. SC_REF and SC_SYNC Input Timing

PAL_ID Input

The PAL_ID input is used by the analog genlock circuit to control the PAL chroma **V-axis** inversion. PAL_ID is only recognized when GENEN = 1 and the video format is PAL. PAL_ID is low for lines where the color burst phase is 135^{o}, and high for lines where the color burst phase is -135^{o}. PAL_ID is sampled and its value is used on the following line. The PAL_ID should be valid during the time interval corresponding to video samples 1440 to 1449. See Figure 8 for the PAL_ID timing requirement.

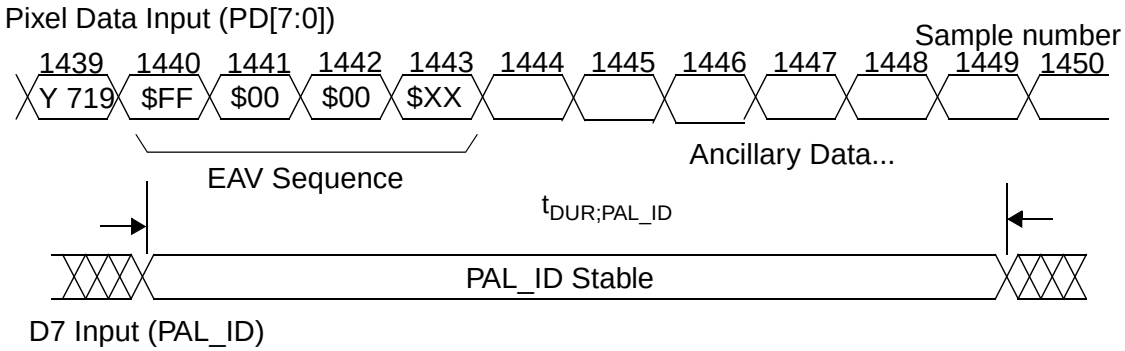


Figure 8. PAL_ID Input Timing

SC_SYNC and PAL_ID Pins

The SC_SYNC and PAL_ID inputs are shared with the D6 and D7 general purpose I/O pins respectively. To configure D6 as the SC_SYNC input, the register value of [DDR6, GENEN, 4FSCS] must be set to [0, 1, 1]. To activate the PAL_ID input, the register value of [DDR7, GENEN, FORMAT] must be set to [0, 1, 01] or [0, 1, 10].

SCH Phase Control

The video encoder maintains a constant 4-field (NTSC) or 8-field (PAL) sub-carrier/horizontal synch phase relationship in the free running mode by resetting the subcarrier synthesizer every 8 fields. In all mode of operations the SCH phase can be adjusted via **SCHM** and **SCHB** registers to compensate external phase delay.

VIDEO TIMING GENERATION

The decoder can operate either in master mode or slave mode. In the **salve mode**, the encoder extracts the horizontal and vertical sync timing, blanking, and field count information from the timing reference codes (EAV) in the pixel data stream. Additional timing data may be extracted from horizontal ancillary (HANC) data. The ancillary data definition is shown in Table 2.

In the **master mode**, the encoder generates horizontal synch ($\overline{\text{HSYN}}$) and field (FIELD) signals. The FIELD signal is high for the even field period. To enable the master mode the direction register DDR3 and DDR2 must be set to '1's and the reserved register 0x83 must be set to 0x18.

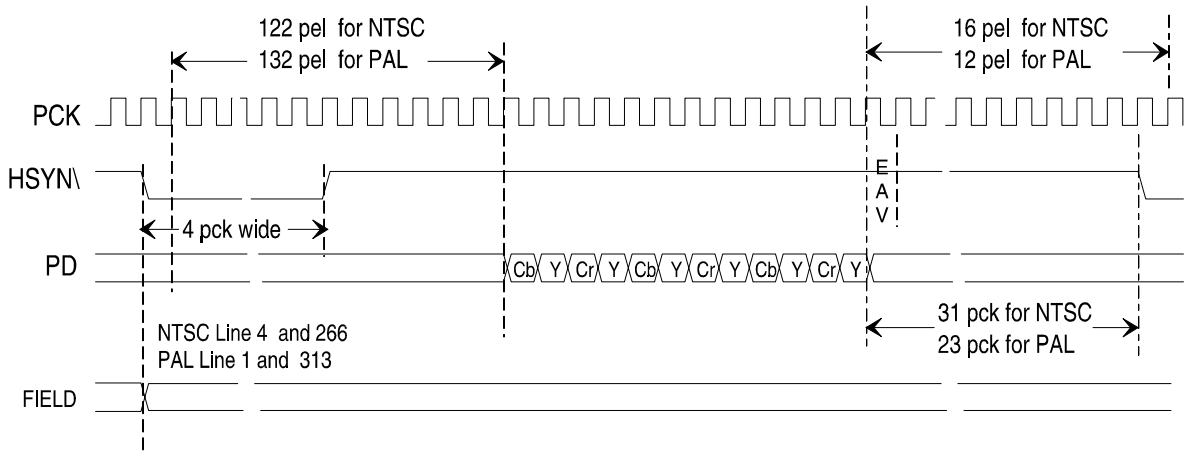


Figure 9. Master Mode Video Interface Timing

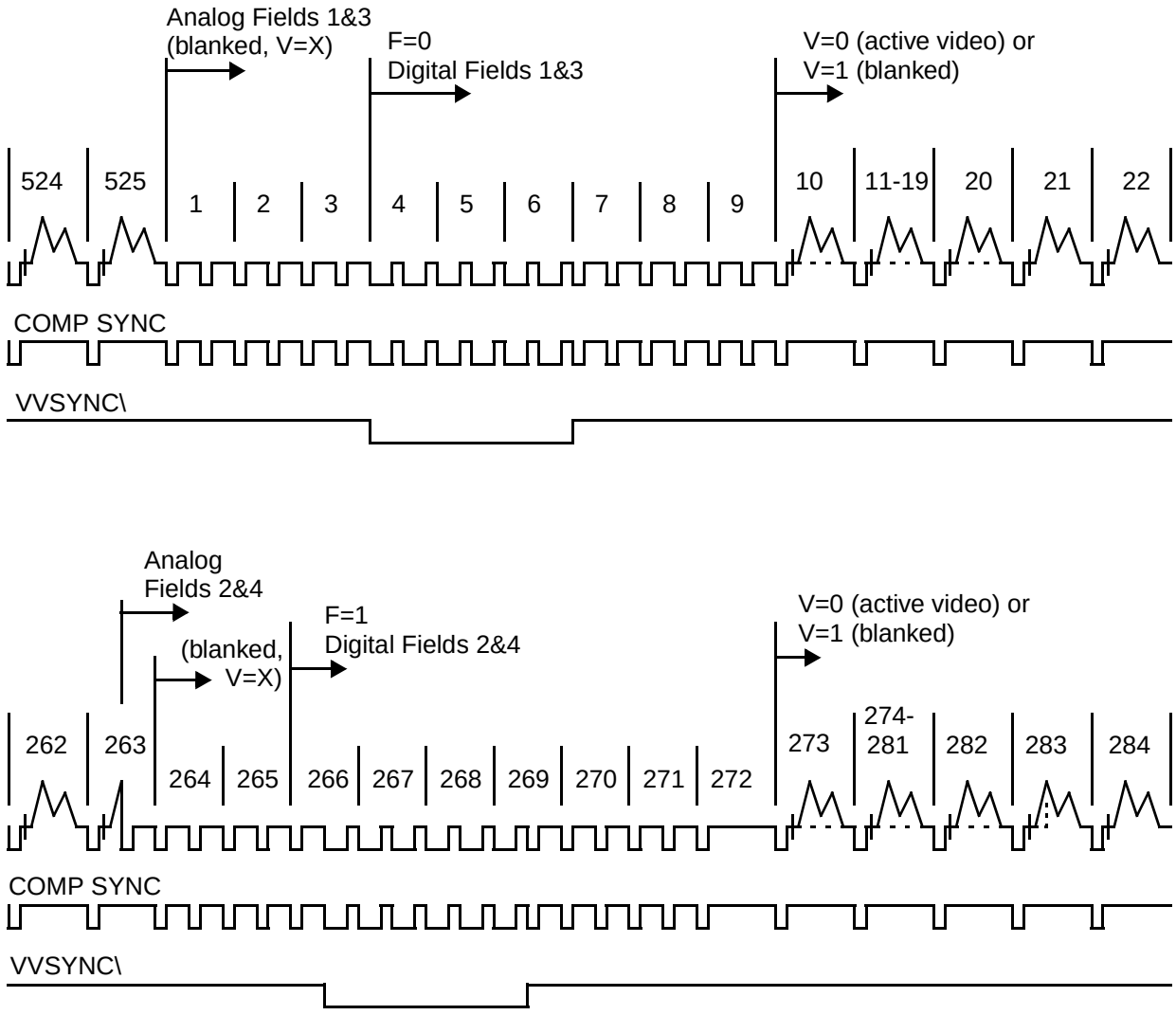


Figure 10. NTSC Vertical Interval

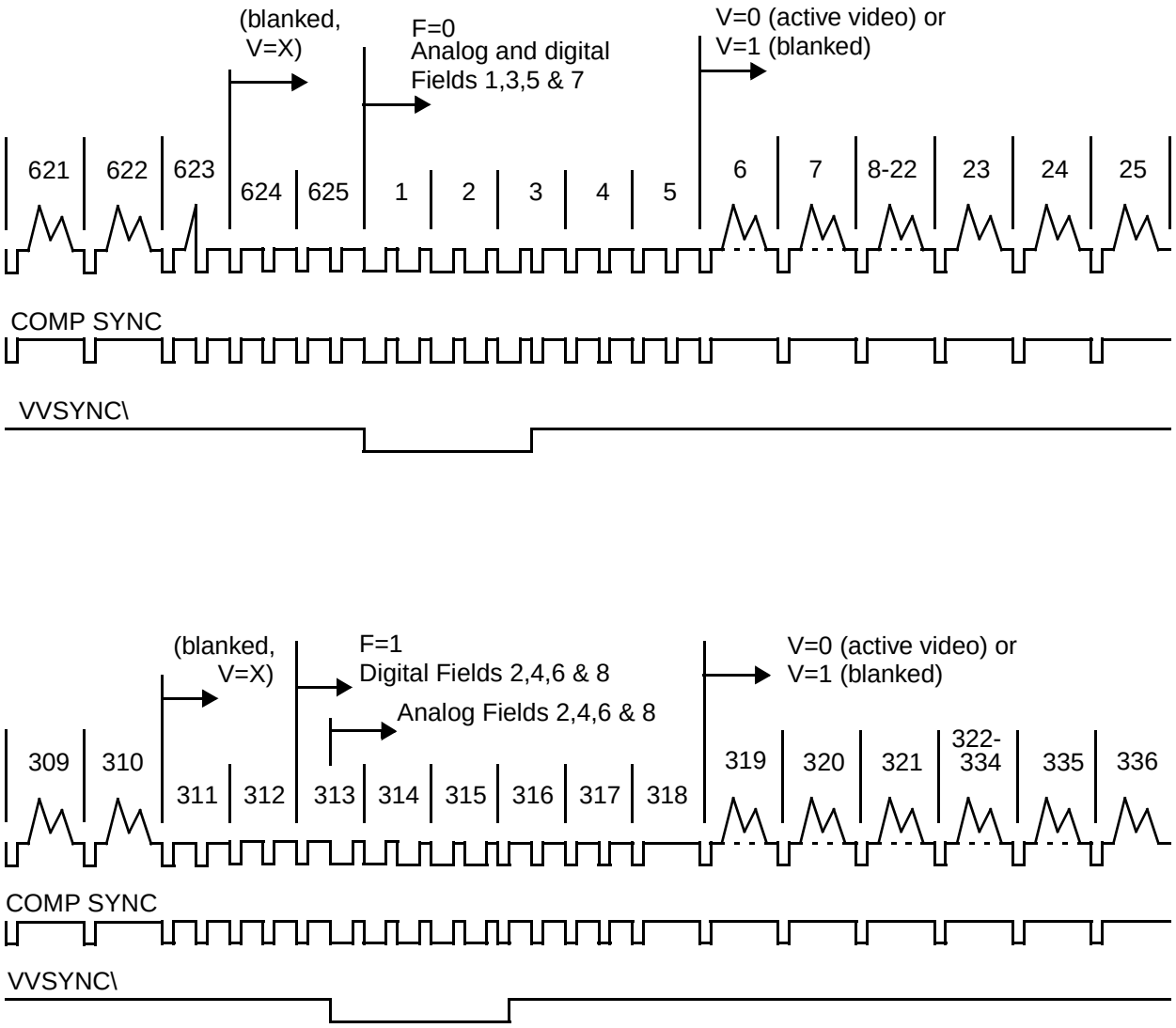


Figure 11. PAL-B, G, H, I, N Vertical Interval

Internal Test Ramp Signal Generation

The modulated ramp test signal is enabled through the host interface by setting the **RAMPEN** bit high. Additionally the **PDEN** must be set to zero to disable the pedestal and reserved registers 0x10 and 0x11 be set to '0's as well. The ramp signal can be used for differential gain and phase measurements. The luminance component ramps from blanking level (0 IRE) to maximum white (100 IRE). The chroma has 40 IRE constant amplitude.

Macrovision Anti-taping

The Macrovision anti-taping revision 6 for PPV application is implemented. For more information please contact Samsung LA Design Center.

Power on Reset

The reset line is an active low signal that is used to initialize the device. Setting $\overline{\text{RESET}}$ low sets all internal state machines and control registers to their initial conditions, disables all digital and analog outputs (high impedance), and places the encoder in a power-down mode.

The reserved register (0x10 - 0x1f) must be set to zero manually for proper operation.

General Purpose I/O Port and Other Signals

Pins D7 through D0 form a general purpose I/O port where some pins have a dual function. The list below indicates the pin functionality. The directions of the I/Os are controlled by the DDR register.

Table 5: General Purpose I/O Functions

Pin	Function
D7 / PAL_ID	General purpose I/O port; also used as the PAL_ID (PAL phase identification) signal input in the analog genlock mode. (see page 15)
D6 / SC_SYNC	General purpose I/O port; also used as the SC_SYNC (subcarrier sync) signal input.(see page 15)
D5 - D4	General purpose I/O ports only.
D3/FIELD	General purpose I/O port in slave mode. FIELD output in Master mode.(see page 15)
D2/$\overline{\text{HSYN}}$	General purpose I/O port in slave mode. $\overline{\text{HSYN}}$ output in Master mode.(see page 15)
D1/CLAMP	General purpose I/O port; also used as the CLAMP (clamp gate) output signal.
D0/CSYN	General purpose I/O port; also used as the CSYN (composite sync) output signal.

The CSYN (composite sync) output is shared with D0 pin, and is programmed with the DDR0 and CSDIS control bits as shown below.

Table 6: Control of Pin D0/CSYN

DDR0 reg.	CSDIS reg.	GPP0 read value	Effect of a GPP0 write on D0/CSYN	Configuration
0	X	Logic state applied to D0	no effect	general purpose input
1	1	not defined	outputs GPP0 logic state	general purpose output
1	0	not defined	no effect	CSYN output

The CLAMP output is shared with D1 pin, and is programmed with the DDR1 and CLMDIS control bits as shown below.

Table 7: Control of Pin D1/CLAMP

DDR1 reg	CLMDIS reg	GPP1 read value	Effect of a GPP1 write on D1/CLAMP	Configuration
0	X	Logic state applied to D1	no effect	general purpose input
1	1	not defined	outputs GPP1 logic state	general purpose output
1	0	not defined	no effect	CLAMP output

D/A Converters

The analog outputs of the encoder come from the three 10-bit D/A converters, operating at a 27 MHz clock rate. The outputs can drive standard video levels into a 75 or 37.5 ohm load. An internal voltage reference can be used to provide reference current for the three D/A converters. For accurate video levels, an external fixed or variable voltage reference source can be used. The video signal levels from the encoder may be adjusted to overcome the insertion loss of analog low-pass output filters by varying R_{REF} or V_{REF}.

There are three analog video outputs, one composite, one luminance, and one chrominance. The composite and S-video DACs can be disabled independently to save power.

The components required for the DAC voltage and current reference is shown below. The 787 ohm resistor should be used for single end 75 ohm termination while the 394 ohm resistor for double end 75 ohm termination.

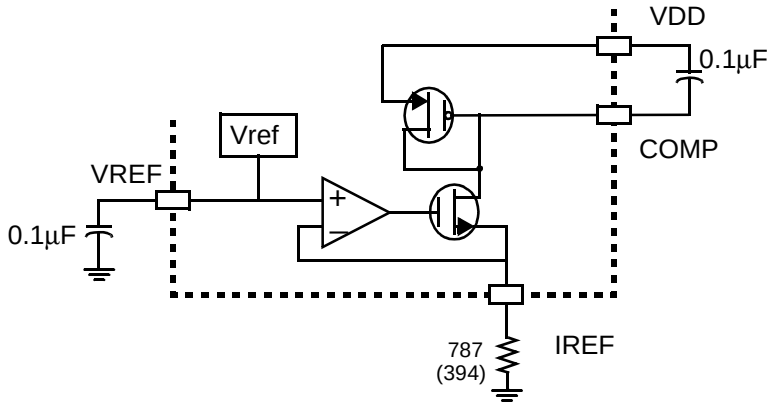


Figure 12. Voltage and Current Reference Components

Two reconstruction filters are suggested for the output of the D/A converters. The one shown in Figure 13 is designed to be a single 75 ohm load to the D/A output; while the one shown in Figure 14 is for the double ended termination.

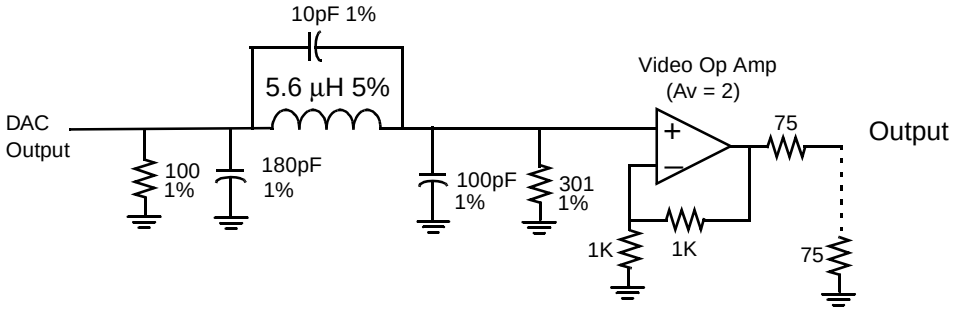


Figure 13. Reconstruction Filter for Single Ended Termination

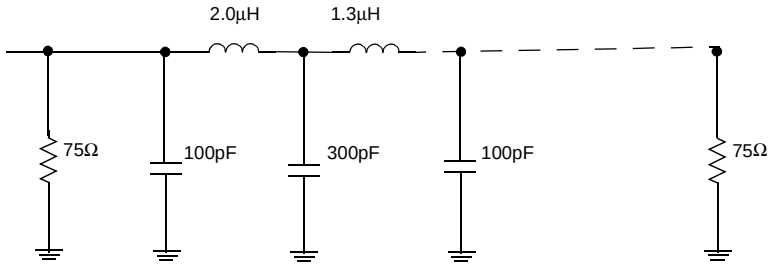
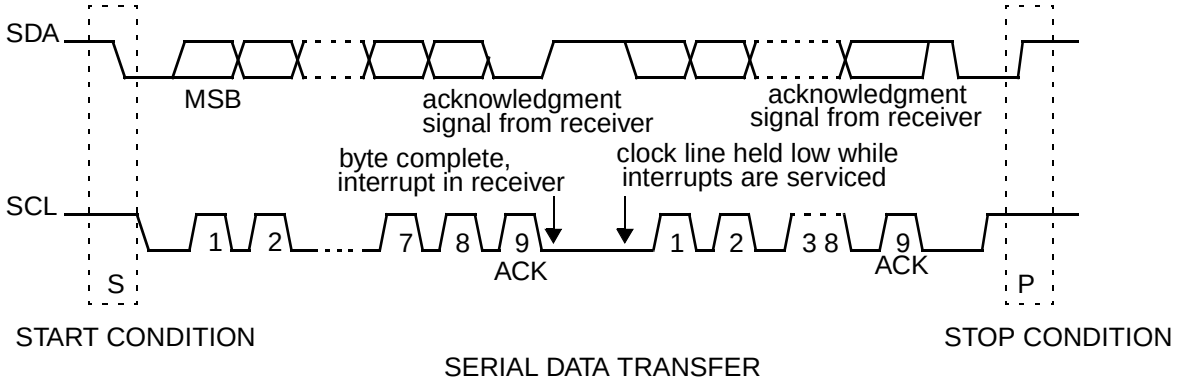


Figure 14. Reconstruction Filter for Double Ended Termination

Serial Host Interface

The internal control registers of the encoder are read and written via a two wire serial port. The two wire port consists of a serial I/O data line (SDA) and a clock (SCL) input. Each of the SDA and SCL line is connected to +VDD with a pull-up resistor. The data on the SDA line must be stable when the clock (SCL) is high. Data can only change while SCL is low. Transitions on SDA while SCL is high indicate start (high to low transition) and stop (low to high) conditions. When both lines are high, the bus is considered to be free.

Communication consists of five parts: the START signal, slave address transmission, (register address transmission), data transfer, and the STOP signal. When the bus is free, a master initiates communication by sending a start signal (high to low of SDA while SCL is high). The first byte transferred after the start signal is a seven bit long slave address followed by the eighth R/W bit. The R/W bit indicates the direction of data transfer (high = read). If the slave address matches that of the encoder (set with pins SA1 and SA2), the encoder will acknowledge by pulling SDA low during the 9th clock. The bytes following the slave address are the data to or from the encoder. Each byte is 8 bits long with the MSB transferred first. Each byte is followed by an acknowledge by the receiving device by pulling the SDA line low during the 9th clock. A stop signal is created when the master sends a low to high on the SDA line with SCL high. Figure 15 shows the data transfer and acknowledge on the serial bus.



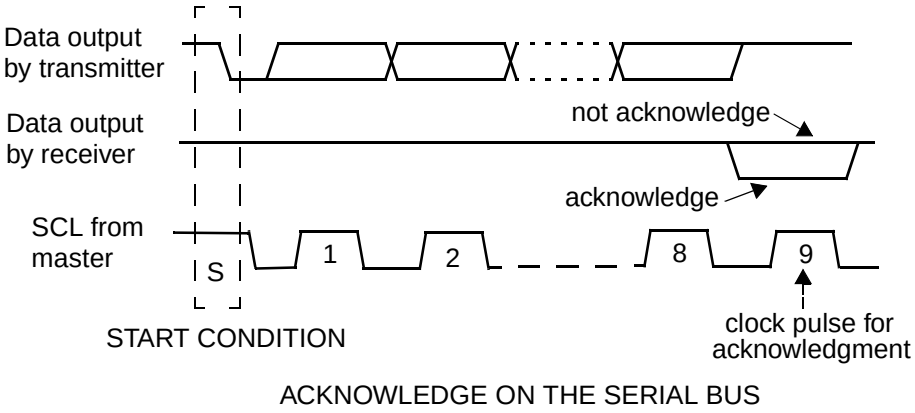


Figure 15. Serial Bus Timing

The master must specify a base address (BAR) when it accesses the encoders registers. The base address is written to the encoder following the slave address when the R/W bit is low. For encoder register writes, data bytes are sent to the control registers starting with the register selected by the BAR and incremented by one address for each additional data byte transferred (auto increment). To read data from the encoder control registers, two data transfer operations are required. The first one writes the BAR (R/W = 0) and the second one is to read the data (R/W = 1). Figure 16 explains the data transfer operations.

Write to Control Registers

START signal
Slave address (R/W = 0)
Base address (BAR)
Data transfer (master to encoder, one or more bytes)
STOP signal

Read from Control Registers

START signal
Slave address (R/W = 0)
Base address (BAR)
STOP signal
START signal
Slave address (R/W = 1)
Data transfer (encoder to master, one or more bytes)
STOP signal

Figure 16. Typical Write and Read Operations

Two address select pins are used to select one of four slave addresses, the slave address is seven bits long. Refer to Table 8 for the possible slave addresses.

Table 8: Serial Port Slave Addresses

A6	A5	A4	A3	A2	A1 (SA2)	A0 (SA1)
0	0	0	1	1	0	0
0	0	0	1	1	0	1
0	0	0	1	1	1	0
0	0	0	1	1	1	1

The serial port timing parameters are shown below, refer to the timing tables at the end of this data sheet for the values.

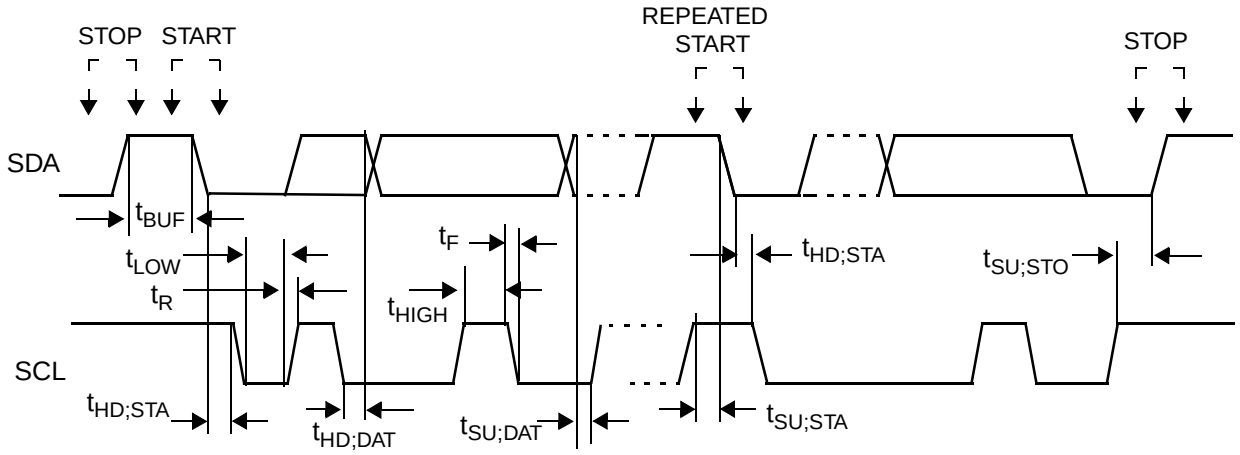


Figure 17. Serial Port Timing Parameters

JTAG Test Interface

The encoder includes a 4-line JTAG test interface port (as modified herein), providing access to all digital input/output data pins except the JTAG test port pins, analog pins, power and ground. This is provided to facilitate component and board-level testing. Table 9 shows the sequence of the test registers. The register number indicates the order in which the register data is loaded and read. The scan is 23 registers long.

The test data input (TDI) and test mode select (TMS) inputs are referred to the rising edge of the test clock (TCK) input. The test data output (TDO) is referred to the falling edge of TCK.

Table 9: JTAG Sequence List

JTAG Reg	Pin	JTAG Reg	Pin	JTAG Reg	Pin
1	$\overline{\text{RESET}}$	9	PD1	17	D6
2	PXCK	10	PD0	18	D5
3	PD7	11	SA2	19	D4
4	PD6	12	SA1	20	D3
5	PD5	13	SDA	21	D2
6	PD4	14	SCL	22	D1
7	PD3	15	SC_REF	23	D0
8	PD2	16	D7		

The JTAG test port timing is shown below, refer to the timing tables at the end of this data sheet for the values.

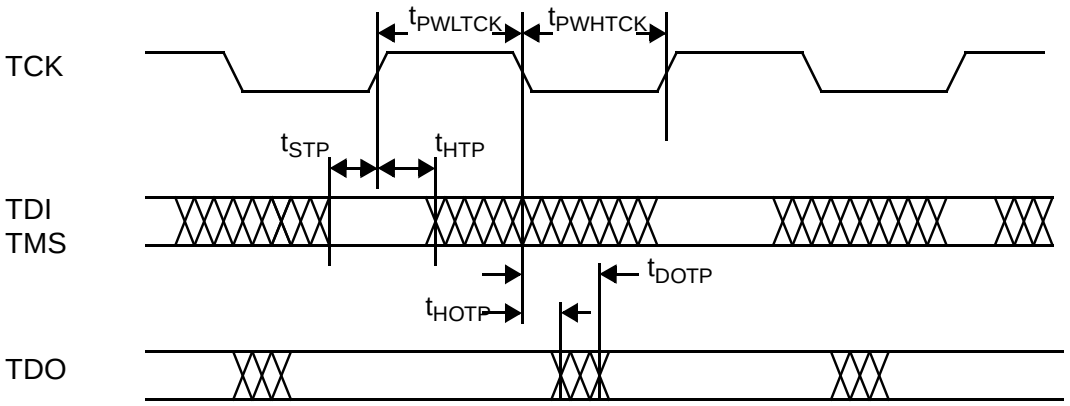


Figure 18. JTAG Test Port Timing

CONTROL REGISTERS

The encoder is controlled by a set of registers which allow adjustment of its operating parameters. The registers are written to and read from via the serial bus interface. Unless otherwise specified, all registers are read/write registers. The suffix “h” denotes hex numbers. In the detailed register description, the default value is followed by an “*”.

Table 10: Control Registers

Index	Mnemonic	Default	Description
00h	PIDC	91h	Part ID Register C (read only)
01h	PIDB	88h	Part ID Register B (read only)
02h	PIDA	79h	Part ID Register A (read only)
03h	REVID	01h	Part Revision Number (read only)
04h	GCR	00h	Global Control Register
05h	VOCR	00h	Video Output Control Register
06h	HANC	00h	Horizontal Ancillary Data Control Register
07h	ANCDID	00h	Ancillary Data ID Register
08h	FREQD*	43h	Subcarrier Frequency Byte 3 (MSBs)
09h	FREQC*	E0h	Subcarrier Frequency Byte 2
0Ah	FREQB*	F8h	Subcarrier Frequency Byte 1
0Bh	FREQA	3Eh	Subcarrier Frequency Byte 0 (LSBs)
0Ch	SCHM	00h	Subcarrier Phase Offset MSBs
0Dh	SCHL	00h	Subcarrier Phase Offset LSBs
0Eh	GPP	00h	General Purpose Port
0Fh	DDR	00h	General Purpose Port Data Direction Control
10-FFh			Reserved

* double buffer registers; newly loaded FREQD-B’s values will not take effect until FREQA has been updated.

Part ID Register									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
00h	**PIDC**	PID23	PID22	PID21	PID20	PID19	PID18	PID17	PID16
01h	**PIDB**	PID15	PID14	PID13	PID12	PID11	PID10	PID09	PID08
02h	**PIDA**	PID07	PID06	PID05	PID04	PID03	PID02	PID01	PID00

PID[23:00] Chip part ID number. This is a read only set of registers. The numbers contained in the registers are:
PIDA = 79h
PIDB = 88h
PIDC = 91h.

Part Revision ID Number									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
03h	**REVID**	REVID7	REVID6	REVID5	REVID4	REVID3	REVID2	REVID1	REVID0

REVID Chip revision ID number. This read only register is used to indicate the silicon revision level number.

Global Control Register									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
04h	**GCR**	4FSCS	GENEN	YCDLY	RMPEN	YCDIS	CDIS	FMT1	FMT0

4FSCS Subcarrier select.
- 1 SC_REF frequency equals 4 times color subcarrier frequency.
- 0 SC_REF frequency.*

GENEN Genlock (to external reference) mode enable.
- 1 The encoder will lock its internal subcarrier synthesizer to an external reference subcarrier input.
- 0 Normal operation.*

YCDLY Luma to chroma delay. This may be used to compensate for luma and chroma group delay variations of the external analog lowpass filter
- 1 The luminance signal is delayed by 37 nS relative to the chrominance signal.
- 0 Normal operation.*

RMPEN Modulated ramp enable.
- 1 The encoder outputs a modulated ramp for differential phase and gain measurements.
- 0 Normal operation.*

YCDIS Y/C output disable.
- 1 The Y and C outputs are disabled, and in a high impedance state.
- 0 Normal operation.*

CDIS Composite output disable.
- 1 The CVBS output is disabled, and in a high impedance state.
- 0 Normal operation.*

FMT Video format select. Note: the subcarrier frequency, pedestal level, and chroma bandwidth are programmed individually and are independent of the format register.
- 00 NTSC.*
- 01 PAL-B,G,H,I,N(Argentina).
- 10 PAL-M.
- 11 reserved.

Video Output Control Register									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
05h	**VOCR**	CSDIS	CLMDIS	CHRBW	SYNDIS	BURDIS	LUMDIS	CHRDIS	PEDEN

CSDIS Composite sync (COMPS) output disable. Control depends on the state of the DDR0 bit. See Table 6.

CLMDIS Clamp gating signal (CLAMP) output disable.
Control depends on the state of the DDR1 bit. See Table 6.

CHRBW Chroma bandwidth select.
1 Chrominance bandwidth is 1.3 MHz.
0 Chrominance bandwidth is 650 kHz.*

SYNDIS Sync disable. When active, the horizontal and vertical sync pulses are disabled, and the encoder will output blanking level during this time. Active video and color burst are not affected.
1 Disable active.
0 Normal operation.*

BURDIS Chroma burst (color burst) disable. Chroma data at the output is not affected by this register.
1 The chroma reference burst output is disabled.
0 Normal operation, burst is enabled.*

LUMDIS Luminance input disable. Color burst and sync are not affected by this register.
1 Luminance data into the IC are forced to black level.
0 Normal operation. Incoming luminance data (Y) is enabled.*

CHRDIS Chroma input disable. The color burst output is not affected by this register.
1 Chroma data into the IC is suppressed, enabling monochrome operation.
0 Normal operation. Incoming chroma (C) data is enabled.*

PEDEN Pedestal (setup) enable. When active, a 7.5 IRE (nominal) pedestal is inserted into the output video for lines 23-262 and 286-525 only. The gain factors are adjusted to keep chrominance from exceeding prescribed levels. Lines 1-22 and 263-285 don't contain setup. This register is valid for NTSC and PAL-M only.
1 Active (use only for NTSC and PAL-M).
0 Pedestal (setup) is disabled for all lines. The black and blanking levels are the same.*

Note: when SYNDIS=BURDIS=LUMDIS=CHRDIS=1, then the encoder outputs fixed DC at the blanking level.

Horizontal Ancillary Data (HANC) Control Register									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
06h	**HANC**	Reserved	NOLCK	FIELD2	FIELD1	FIELD0	AFREN	APHEN	ATMEN

Reserved Reserved. Do Not Use.

NOLCK Genlock status. *Read only.* NOLCK is valid only when GENEN = 1.

1 Indicates that lock has not been achieved.

0 Indicates that the internal subcarrier synthesizer is locked to the external reference.*

FIELD2-0 Field identification number *Read only.* These 3 bits indicate the digital field number.

000 Field 1
001 Field 2
010 Field 3
011 Field 4
100 Field 5
101 Field 6
110 Field 7
111 Field 8

AFREN Ancillary frequency data enable. When GLKEN = 1 (genlock to external reference), the encoder may assume that AFREN will be set to 0 by the firmware. In this case, the FREQ register value will be controlled by the genlocking circuit.

1 The encoder programs the subcarrier FREQ register from the ancillary data stream (depending on the state of the FRV bit).

0 The FREQ register is programmed through the microprocessor interface.*

APHEN Ancillary phase data enable. When GENEN = 1 (genlock to external reference), the encoder may assume that APHEN will be set to 0 by the firmware. In this case, the PHASE register value will be controlled by the genlocking circuit.

1 The encoder programs the subcarrier PHASE register from the ancillary data stream (depending on the state of the PHV bit).

0 A value of 0 is used for the PHASE register.*

ATMEN Ancillary timing reference data enable.

1 The encoder uses the timing reference data contained in the ancillary data stream (FIELD and SVF/).

0 The ancillary timing reference data is ignored.*

Ancillary Data ID Register									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
07h	**ANCDID**	ANCD7	ANCD6	ANCD5	ANCD4	ANCD3	ANCD2	ANCD1	PARITY

ANCD[7:1] The seven bits, ANCD7 through ANCD1, determine the data ID. The encoder uses the data ID to determine if the ancillary data it is receiving is meant for the encoder.

PARITY Bit 0 is an odd parity bit for the ancillary data ID byte mentioned above. The encoder does not use this bit.

Subcarrier Frequency Register									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
08h	**FREQD**	FRQ31	FRQ30	FRQ29	FRQ28	FRQ27	FRQ26	FRQ25	FRQ24
09h	**FREQC**	FRQ23	FRQ22	FRQ21	FRQ20	FRQ19	FRQ8	FRQ7	FRQ16
0Ah	**FREQB**	FRQ15	FRQ14	FRQ13	FRQ12	FRQ11	FRQ10	FRQ09	FRQ08
0Bh	**FREQA**	FRQ07	FRQ06	FRQ05	FRQ04	FRQ03	FRQ02	FRQ01	FRQ00

FRQ[31:00] These registers hold the 32 bit subcarrier frequency value. The FREQD-B registers are double buffered; the newly loaded msb values will not take effect until the lsb (FREQA) has been written.

Subcarrier Phase Offset Register									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0Ch	**SCHM**	SCH15	SCH14	SPH13	SCH12	SCH11	SCH10	SCPH9	SCPH8
0Dh	**SCHL**	SCH07	SCH06	SCH05	SCH04	SCH03	SCH02	SCH01	SCH00

SPH[15:00] These registers hold the static subcarrier phase offset. This is used to adjust the phase of the subcarrier relative to the 50% point of the leading edge of hsync (SCH phase). The nominal value is 0. This register is used to compensate for delays external to the encoder.

General Purpose Port									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0Eh	**GPP**	GPP7	GPP6	GPP5	GPP4	GPP3	GPP2	GPP1	GPP0

GPP7 - GPP0 Registers GPP7 through GPP0 are used to read and write to I/O pins D0 through D7. The direction of flow of these pins is set by the data direction register. Note that pins D7, D6, D1, and D0 are shared with other signals.

GPP7 = D7 I/O Pin.
GPP6 = D6 I/O Pin.
GPP5 = D5 I/O Pin.
GPP4 = D4 I/O Pin.
GPP3 = D3 I/O Pin.
GPP2 = D2 I/O Pin.
GPP1 = D1 I/O Pin.
GPP0 = D0 I/O Pin.

General Purpose Port Data Direction Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0Fh	**DDR**	DDR7	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0

DDR7 - DDR0 Registers DDR7 through DDR0 are used to control the direction of data flow of I/O pins D0 through D7. Setting DDR(i) (where i = 7 to 0) to a low will make that pin an input. Setting DDR(i) high will make that pin an output.

DDR7 = Data direction control for pin D7.
DDR6 = Data direction control for pin D6.
DDR5 = Data direction control for pin D5.
DDR4 = Data direction control for pin D4.
DDR3 = Data direction control for pin D3.
DDR2 = Data direction control for pin D2.
DDR1 = Data direction control for pin D1.
DDR0 = Data direction control for pin D0.

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Min	Max	Unit
Supply Voltage (Measured to GND)	V_{DD}	-0.5	+7.0	V
Digital Input Applied Voltage[2]	V_I	GND-0.5	V_{DD}+0.5	V
Digital Input Forced Current[3,4]	A_I	-100	100	mA
Digital Output Applied Voltage[2]	V_O	GND-0.5	V_{DD}+0.5	V
Digital Output Forced Current[3,4]	A_O	-100	100	mA
Digital Short Circuit Duration (single high output to VSS)	TD_{SC}		1	sec
Analog Short Circuit Duration (single output to VSSA)	TA_{SC}		infinite	sec
Ambient Operating Temperature Range	Ta	-60	+130	°C
Storage Temperature Range	Tstg	-65	+150	°C
Junction Temperature	Tj		+150	°C
Soldering Temperature (10 sec., 1/4” from pin)	Tsol		+300	°C
Vapor Phase Soldering (1 min.)	Tvsol		+220	°C
Storage Temperature	T_{stor}	-65	+150	°C

Notes: 1. Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to VSS.
3. Forcing voltage must be limited to a specified range.
4. Current is specified as conventional current, flowing into the device.

RECOMMENDED OPERATING CONDITIONS

Unless otherwise specified, all specifications shall be met over the operating temperature range (0 to 70 ^{o}C, case), with a digital supply voltage (V_{DD}) of 5.00 VDC ± 5% and analog supply voltage (V_{DDA}) of 5.00 VDC ± 5%.

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	4.75	5	5.25	V
Ambient Operating Temperature Range	Ta	0		70	°C

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Total Power Supply Current (Digital Plus Analog[1], F_{PXCK} = 27 MHz)	I_{DD}			160	mA
Total Power Supply Current (DACs Disabled[2], F_{PXCK} = 27 MHz)	I_{DDQ}			110	mA
Digital Input Voltage, Logic HIGH TTL Compatible Inputs	V_{IH}	2.0		V_{DD}	V
Digital Input Voltage, Logic HIGH Serial Port (SDA, SCL)	V_{IH}	0.7		V_{DD}	V
Digital Input Voltage, Logic LOW TTL Compatible Inputs	V_{IL}	V_{SS}		0.8	V
Digital Input Voltage, Logic LOW Serial Port (SDA, SCL)	V_{IL}	V_{SS}		0.3	V
Digital Input Current, Logic HIGH (V_{IN}= 4.0 V)	I_{IH}			10	µA
Digital Input Current, Logic LOW (V_{IN}=0.4 V)	I_{IL}			-10	µA
Digital Input Capacitance(f=1MHz,V_{IN}=2.4 V)	C_{IN}			7	pF
Digital Output Voltage, Logic HIGH CMOS Compatible Outputs (I_{OH}=-1 mA)	V_{OH}	3.7		V_{DD}	V
Digital Output Voltage Logic LOW CMOS Compatible Outputs (I_{OL}=4.0 mA)	V_{OL}	V_{SS}		0.4	V
Digital Output Voltage Logic LOW Serial Port (SDA) (I_{OL}=3.0 mA)	V_{OL1}	V_{SS}		0.4	V
Digital Output Voltage Logic LOW Serial Port (SDA) (I_{OL}=6.0 mA)	V_{OL2}	V_{SS}		0.6	V
Hi-Z Leakage Current, HIGH (V_{DD}=Max, V_{IN}=V_{DD})	I_{OZH}			10	µA
Hi-Z Leakage Current, LOW (V_{DD}=Max, V_{IN}=V_{SS})	I_{OZL}			-10	µA
Digital Input Capacitance (T_A=25 ^oC, F=1 MHz)	C_I			8	pF
Digital Output Capacitance (T_A=25 ^oC, F=1 MHz)	C_O			10	pF

Notes: 1.Maximum I_{DDD} and I_{DDA} with V_{DD} = V_{DDA} = +5.25 VDC and T_A = 0 to 70 ^oC. D/A converters loaded with R_L = 75 Ω.
2. I_{DDQ} when $\overline{\text{RESET}}$ = HIGH, CDIS = YCDIS = HIGH (DACs disabled).

PIXEL DATA PORT

Characteristics	Symbol	Min	Typ	Max	Unit
Master Clock Rate (PXCK input)	F_{PXCK}	26.9999	27.0	27.0001	MHz
Pixel Rate ($F_{PCK} = F_{PXCK}$ /2)	F_{PCK}		13.5		M_{pps}
PXCK Pulse Width, HIGH	$T_{PWH;PXCK}$	10	18.5		ns
PXCK Pulse Width, LOW	$T_{PWL;PXCK}$	14.5	18.5		ns
PXCK Rise Time (10% to 90% points)	T_{RP}			TBD	ns
PXCK Fall Time (10% to 90% points)	T_{FP}			TBD	ns
PD7-0 Setup Time	$T_{SU;PD}$	5			ns
PD7-0 Hold Time	$T_{HD;PD}$	3			ns
Process Delay (from PD input to DAC inputs)	T_{PD}		48		PXCX Periods

Note: Timing reference points are at the 50% level. Digital C_{LOAD} < 40 pF.

SERIAL MICROPROCESSOR PORT

Characteristics	Symbol	Min	Typ	Max	Unit
SCL Clock Frequency (F_{PXCK} = 27.0 MHz)	F_{SCL}		Note 3	500	kHz
SCL Clock LOW period	T_{LOW}	1.0			µs
SCL Clock HIGH period	T_{HIGH}	0.48			µs
SDA & SCL input rise time	T_R			240	ns
SDA & SCL input fall time	T_F			240	ns
SDA output fall time from $V_{IH\ MIN}$ to $V_{IL\ MAX}$; bus capacitance = 10 pF to 400 pF. Up to 3 mA current at $V_{OL1.}$	T_{OF1}			200	ns
SDA output fall time from $V_{IH\ MIN}$ to $V_{IL\ MAX}$; bus capacitance = 10 pF to 400 pF. Up to 6 mA current at $V_{OL2.}$	T_{OF2}			200	ns
Bus free time between a STOP and START condition.	T_{BUF}	1.0			µs
Hold time for START or repeated START condition. After this period, the first clock pulse is generated.	$T_{HD;STA}$	0.48			µs
Setup time for a repeated START condition.	$T_{SU;STA}$	0.48			µs
Data Setup Time	$T_{SU;DAT}$	80			ns
Data Hold Time	$T_{HD;DAT}$	0		0.72	µs
Setup Time for a STOP condition	$T_{SU;STO}$	0.48			µs
SDA output load capacitance	C_B			400	pF

Note:

1. All timing values are referred to $V_{IH\ MIN}$ and $V_{IL\ MAX}$ levels.
2. Timing specifications have been obtained by scaling the Philips I^2C Fast Mode Bus specs by 80%.
3. The nominal F_{SCL} to be used by this device is: F_{SCL} = (F_{PXCK}/56) = (27.0MHz/56) = 482.143 KHz.

JTAG INTERFACE

Characteristics	Symbol	Min	Typ	Max	Unit
Test Clock (TCK) Rate	F_{TCK}			10	MHz
TCK Pulse Width, LOW	T_{PWLTCK}	10			ns
TCK Pulse Width, HIGH	T_{PWHTCK}	10			ns
Test Port Setup Time (TDI, TMS)	T_{STP}	10			ns
Test Port Hold Time (TDI, TMS)	T_{HTP}	0			ns
Output Delay, TCK to TDO Valid	T_{DOTP}			30	ns
Output Hold Time, TCK to TDO Valid	T_{HOTP}		5		ns

Note: Timing reference points are at the 50% level. Digital C_{LOAD} < 40 pF.

MISCELLANEOUS DIGITAL SIGNALS

Characteristics	Symbol	Min	Typ	Max	Unit
RESET/ Active (LOW) Time	T_{SR}		1		µs
SC_SYNC Setup Time	$T_{SU;SC\_SYNC}$	10			ns
SC_SYNC Hold Time	$T_{HD;SC\_SYNC}$	0			ns
PAL_ID Setup Time	$T_{SU;PAL\_ID}$	10			ns
PAL_ID Hold Time	$T_{HD;PAL\_ID}$	0			ns
PAL_ID Duration	$T_{DUR;PAL\_ID}$	9			PXCK periods

Note: Timing reference points are at the 50% level. Digital C_{LOAD} < 40 pF.

ANALOG (DAC) OUTPUTS

Characteristics	Symbol	Min	Typ	Max	Unit
DAC Resolution	RES	10			bits
Power Supply Rejection Ratio (Full scale output) CBYPS = 0.1µF, f = DC to 1MHz, V_{RIP} = 100 mVp-p	PSRR	TBD			dB
Voltage Reference Output	V_{RO}	1.112	1.235	1.359	V
VREF Output Impedance	Z_R	1000			Ω
DAC Gain Factor	K_{DAC}	10.31	10.85	11.39	
K_{DAC} Imbalance Between DACs	K_{IMBAL}	-5		+5	%
DAC Reference Current (R_{REF} = Nom.)	I_{REF}		1.569		mA
Reference Resistor (V_{RO} = Nom.)	R_{REF}		787		Ω
Blanking Level Output Voltage (NTSC and PAL modes)	V_{BLANK}		0.300		V
Video Output Compliance Voltage	V_{OC}	-0.3		1.6	V
Video Output Resistance	R_{OUT}		15		kΩ
Video Output Capacitance (I_{OUT}=0 mA, f=1 MHz)	C_{OUT}		15-25		pF
Total Output Load Resistance	R_L		75		Ω
DAC Output Current Risetime (10% to 90% of full scale)	T_R		2		ns
DAC Output Current Falltime (90% to 10% of full scale)	T_F		2		ns
Analog Output Delay	T_{DOV}		20		ns

Notes: Timing reference points are at the 50% level. Analog C_{LOAD} < 10 pF Digital C_{LOAD} < 40 pF.

GENLOCK PERFORMANCE

Parameter	Units
Locking Range	±2 kHz
SC_REF Duty Cycle	50 ± 10%
Lock Time	40 lines maximum
Jitter	2 deg. p-p maximum

Video Performance

The encoder meets the requirements listed in the table below when configured using the application circuit of Figure 14. The test methods and test signals meet the requirements of NTC Report No. 7 or EIA/TIA-250. A Tektronix TSG1001 Programmable TV Generator and a Tektronix VM700A Video Measurement Set are used for measurement verification.

VIDEO PERFORMANCE CHARACTERISTICS

Test Name	Symbol	Test Waveform	Min	Typ	Max	Unit
Amplitude Response vs. Frequency	AMPRESP	Multiburst to 4.2 MHz			0.25	dBp-p
Differential Gain	DG	Modulated Staircase or Ramp (NTC-7 Composite)			1.5	% p-p
Differential Phase	DP	Modulated Staircase or Ramp (NTC-7 Composite)			1.0	deg p-p
Chroma Nonlinear Gain Distortion	CNLG	Three Level Chroma Signal (NTC-7 Combination)			1.0	IRE
Chroma Nonlinear Phase Distortion	CNLP	Three Level Chroma Signal (NTC-7 Combination)			1.0	deg
Chroma-to-Luma Intermodulation	CLIMD	Three Level Chroma Signal (NTC-7 Combination)			1	IRE
Chroma/Luma Gain Equality	CLGI	12.5T Modulated Pulse (NTC-7 composite) CHRBW = HIGH (1.3 MHz) YCDELAY = LOW.	97.5		102.5	%
Chroma/Luma Delay Inequality. (Analog filter delay excluded)	CLDI	12.5T Modulated Pulse NTC-7 composite) CHRBW = HIGH (1.3 MHz) YCDELAY = LOW.		0	5	ns
Luma Nonlinear Distortion	LNLD	5-Step Unmodulated Staircase			2.5	%
Noise Level[1]	NOISE1	100% Unmodulated Ramp			-61	dBrms
Noise Level[2]	NOISE2	100% Unmodulated Ramp			-72	dBrms
Chroma AM Noise	CAMN	Red Field, 500 kHz BW			-56	dBrms
Chroma PM Noise	CPMN	Red Field, 500 kHz BW			-58	dBrms
Field Time Waveform Distortion	FTWD	Field Square Wave			1.5	IREp-p
Line Time Waveform Distortion	LTWD	18 μS 100 IRE Bar (NTC-7 Composite)			0.5	IREp-p
Long Time Waveform Distortion: Initial Peak Overshoot Peak Overshoot after 5 seconds	LOTWD	10% / 90% APL Bounce			 15 1.5	IRE

VIDEO PERFORMANCE CHARACTERISTICS

Test Name	Symbol	Test Waveform	Min	Typ	Max	Unit
Short Time Waveform Distortion	STWD	100 IRE Step, 125 ns rise time (NTC-7 COmposite)			1	% SD
Line-by-Line DC Offset	LDCOFF	10% / 90% APL Bounce	-1		1	IRE
Dynamic Gain	DYNG		-1		1	IRE

Notes: 1. Noise level is unified weighted, 10 kHz to 5.0 MHz bandwidth, with Tilt Null ON measuring using VM700 “Measure Mode”. A trap at the color burst frequency may be used.

2. Noise level is unified weighted, 10 kHz to 5.0 MHz bandwidth, measured using VM700 “Auto Mode”.

KS0123 Design Hints

Figure 19 describes power supply decoupling. A clean power supply is crucial for proper operation of the device. Noise on the power supply lines will couple onto the analog inputs and ultimately result in poor picture quality. The digital and analog VDD supplies should be separately decoupled with external filter components. This is achieved by using a ferrite bead with a capacitor on either side. In addition to this filter, 0.1µF capacitors should be placed by each IC power pin. Additional decoupling can be achieved by placing 0.01µF capacitors in parallel with the 0.1µF capacitors. These components should be located close to the ENCODER device. The ENCODER ideally should be located near the input power supply and close to the video inputs connectors.

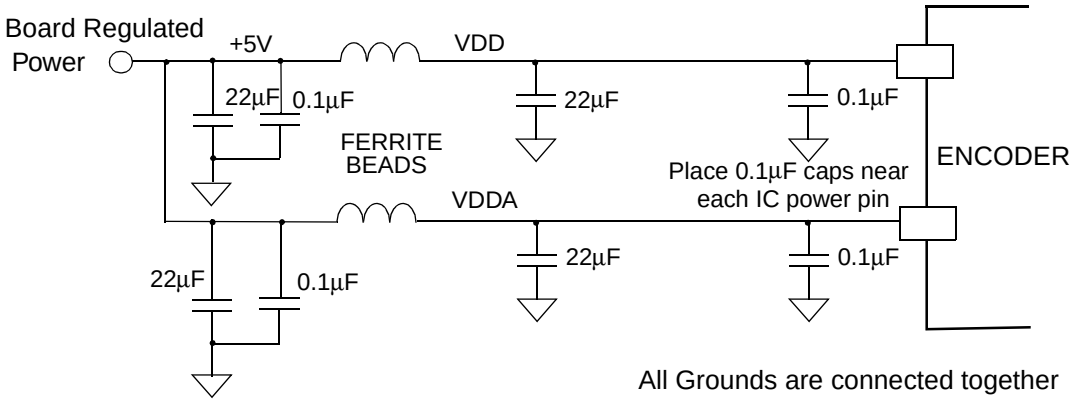


Figure 19. Power Supply Filtering

A number of different ferrite beads can be used for power supply decoupling. Wire wound ferrite beads are generally large, but offer greater current capacity and higher impedance for a given frequency (this depends on the ferrite material and number of windings). A larger current capacity is useful for decoupling many components, such as a board power supply. Bead on lead and surface mount ferrites do not afford a large impedance to AC, but the capacitors on each side of the ferrite should eliminate any excessive digital switching noise. Generally, pick a ferrite with the lowest DC resistance and highest impedance to signals centered around 27 MHz. The large capacitor on the component side of the ferrite provides low frequency filtering, and acts as a charge reservoir for rapid current requirements by the ENCODER. Generally, this is located near the ferrite. Some suggested ferrite beads are:

- TDK: Wire wound ZBF113T-01; Bead on lead BF45-4001; Surface mount CB50-1206. TDK can be reached at (708) 803-6100.
- Fair-Rite: Wire wound beads Fair-Rite 2943666671; Bead on lead 274300111; SM beads 2743021447. Fair-Rite is at (914) 895-2055.

Applications that reside in noisy environments or utilize a switching power supply should have local power regulation. For example, designs for the PC should use the 12 volt power supply and locally regulate the supply to 5 volts with a linear regulator.

For decoupling, use high quality RF capacitors. Type COG or NPO should be used. Avoid Z5U capacitors. Surface mounting of the filter components is highly recommended. If leaded components are used, keep the leads and traces as short as possible.

Use a multilayer PC board with separate power and ground planes. The surface mount package requires the top layer to be a signal layer. The top layer should contain the analog traces, avoid running digital signal traces (clocks and data lines) or other high speed lines directly under the device. The ground plane should be placed directly

below the top signal layer. A low impedance ground path from the device is essential to proper operation and isolation. Use one solid ground plane under the ENCODER, do not split the ground plane. The power plane is next with additional signal planes following. Surface mount passive components can be placed on the under side (solder side) of the final signal plane. Mounting passive components (which could not be located close to the ENCODER on the top signal layer) directly under the device should provide superior performance. A four layer PC board is sufficient for most applications, but noisy densely populated designs may require more layers.

The output video connectors should be located close to the ENCODER. Orient the package so that short leads can be used. The crystal oscillator components should also be mounted very close to the oscillator pins.

The edge rates of clocks and other high speed digital signals should be limited to reduce ringing and noise. Termination with a small series damping resistor (~15 ohms, depends on trace and board characteristics), located at the driving end of a long transmission line, may reduce ringing.