INTRODUCTION

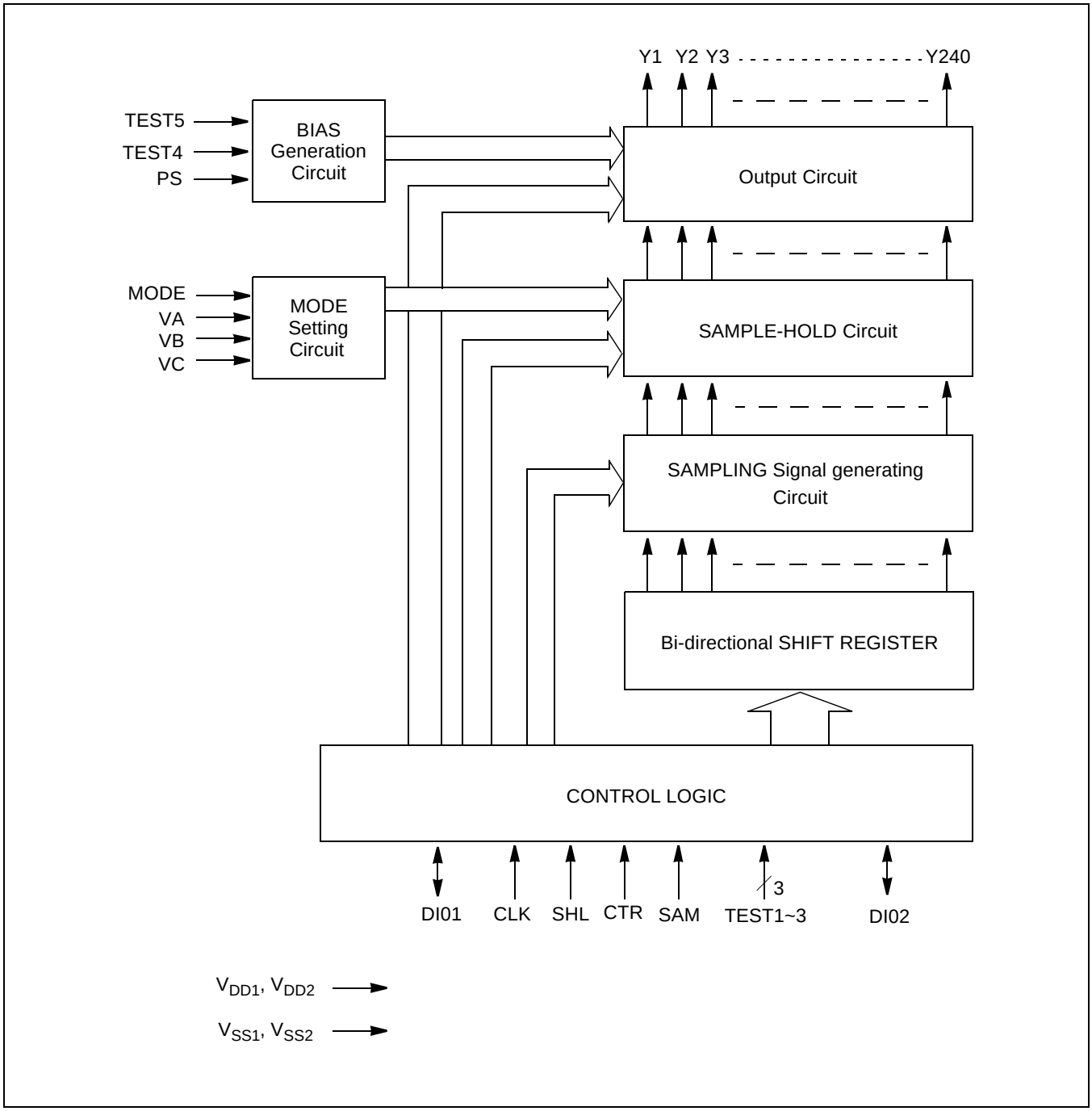
KS0606 is 240 output liquid crystal display (LCD) source driver. It is used in the liquid crystal display panel for pocket sized TV, CNS etc.

After sampling and holding at the SAMPLE-HOLD circuit at the clock synchronized timing, the R,G,B, 3CH. video signals are output simultaneously to all output pins.

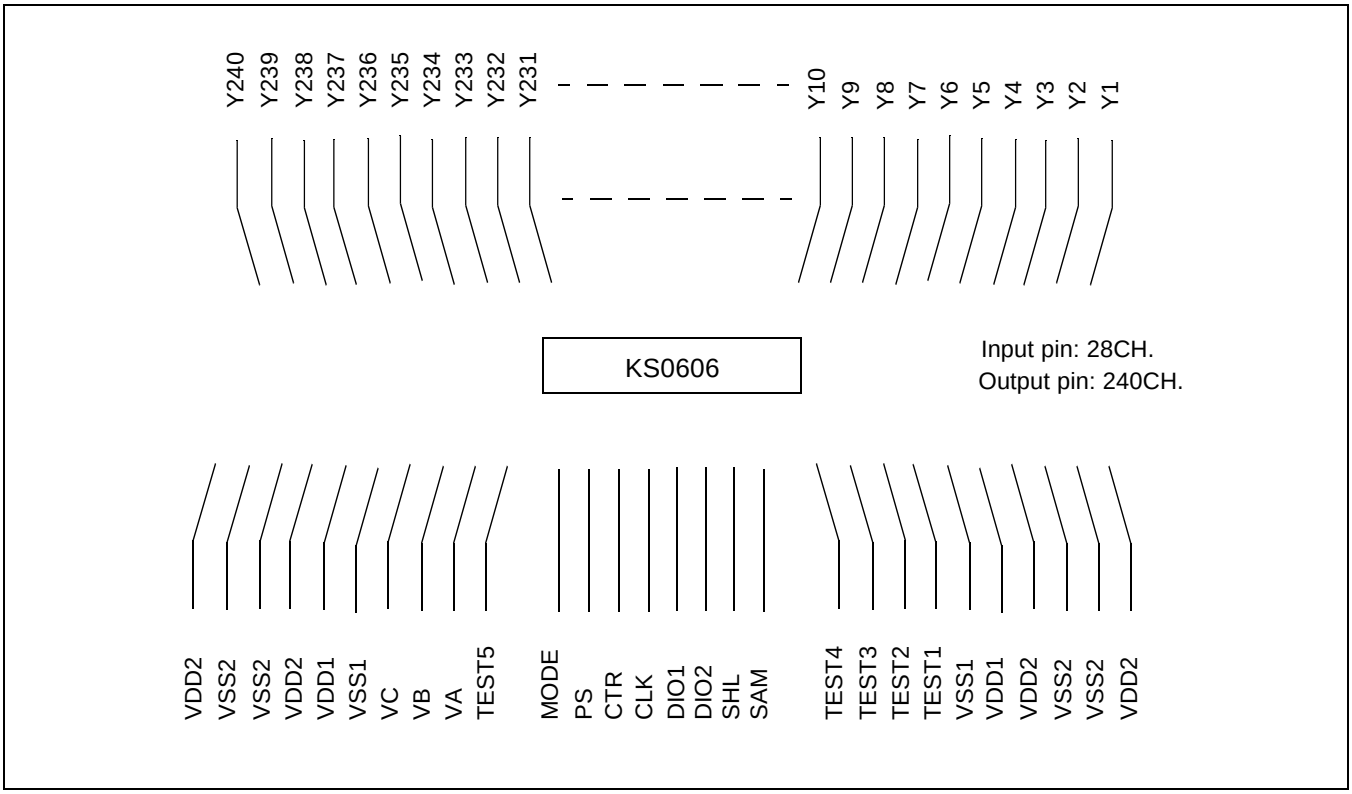
FEATURES

- ❑ Active matrix LCD source driver
- ❑ Video signal SAMPLING: Possible to switch the output direction of LCD drive output (Y1→Y240⇔Y240→Y1)
- ❑ POWER SAVE Function: Possible to set the liquid crystal driver output at HIGH IMPEDANCE(Hi-Z) and simultaneously able to reduce power consumption by stopping amp operation.
- ❑ SAMPLING Timing: Regular sampling and 3 points simultaneous sampling
- ❑ Video Signal Setting: compatible with STRIPE and DELTA array panel by the mode setting circuit
- ❑ LOGIC supply Voltage: 3.0V to 5.5V
- ❑ Driver supply Voltage: 3.0V to 5.5V
- ❑ SAMPLING Frequency: f_{MAX} = 25MHz (V_{DD1} = 3.0V)
- ❑ LCD driver output pins: 240 outputs
- ❑ Output dynamic range: 4.8 Vp-p (at 5V Driver supply voltage)
- ❑ COG

BLOCK DIAGRAM



PIN CONFIGURATION



NOTE: Looking at the CHIP from the top (if PATTERN present).

PIN DESCRIPTION

Symbol	Name	Description
V_{DD1}	LOGIC Power	3.0V to 5.5V
V_{DD2}	Driver Power	3.0V to 5.5V Set so that $V_{DD1} \leq V_{DD2}$.
V_{SS1}	LOGIC GROUND	Ground (0V)
V_{SS2}	Driver GROUND	Ground (0V)
Y1 to Y240	Output of driver LCD	Outputs the voltage corresponding to the video signal held in the SAMPLE-HOLD circuit when PS = “H” and becomes HIGH IMPEDANCE when PS = “L”.
VA,VB,VC	Video Signal Input	Video signal input pin. VA:GREEN signal input, VB: RED signal input, VC: BLUE signal input
MODE	Video Signal MODE Change Input	Sets the video signal that is sampled in the SAMPLE-HOLD circuit. Samples in VB, VA, VC order and VC, VB, VA order when it is “H” and “L”, respectively.
DI01	Left SHIFT, START PULSE Input/Output	SHL=H: START PULSE input pin. SHL=L: START PULSE output pin.
DI02	Right SHIFT, START PULSE Input/Output	SHL=H: START PULSE output pin. SHL=L: START PULSE input pin.
SHL	SHIFT Direction Select Input	Select pin for switching the video signal sampling order and DIO1/ DIO2 input/output. Samples video signals in Y1 → Y240 order when it is “H” and sets DI01 to start pulse signal input and DI02 to start pulse signal output. Samples video signal in Y240 → Y1 order when it is “L” and sets DIO2 to start pulse signal input and DIO1 to start pulse signal output.
CLK	SHIFT CLOCK Input	The video signal is sampled in order at CLK's RISING and FALLING edge.
CTR	Output Circuit Operation-Change Input	Setting pin for changing video signal sampling circuit and output OP-AMP operation.
SAM	SAMPLING MODE Change Input (H: Regular, L: simultaneous)	Setting pin for regular or simultaneous sampling. In regular sampling, one video signal is sampled at CLK’s rising and falling edeg. In simultaneous sampling, three video signals are sampled at CLK’s rising and falling edge. In any sampling, the sampling signal shifts at every CLK’s rising and falling edge. (half clock); its sampling period is 1CLK.
PS	POWER SAVE Setting Input	POWER SAVE Setting Terminal. At “H”, the video signal output pin outputs the video signal held in the SAMPLE-HOLD circuit and, at “L”, The Amp operation is stopped at the same time the video signal output pin becomes HIGH IMPEDANCE, thus, reduce power consumption.
TEST1 to 5	TEST pin	LSI TEST pin, TEST 1 to 4 and TEST5 connect to V_{DD1} and V_{DD2}

OPERATION

OUTPUT EXPANSION

By CASCADE connecting, the output pin can be expanded and applied large LCD panel.

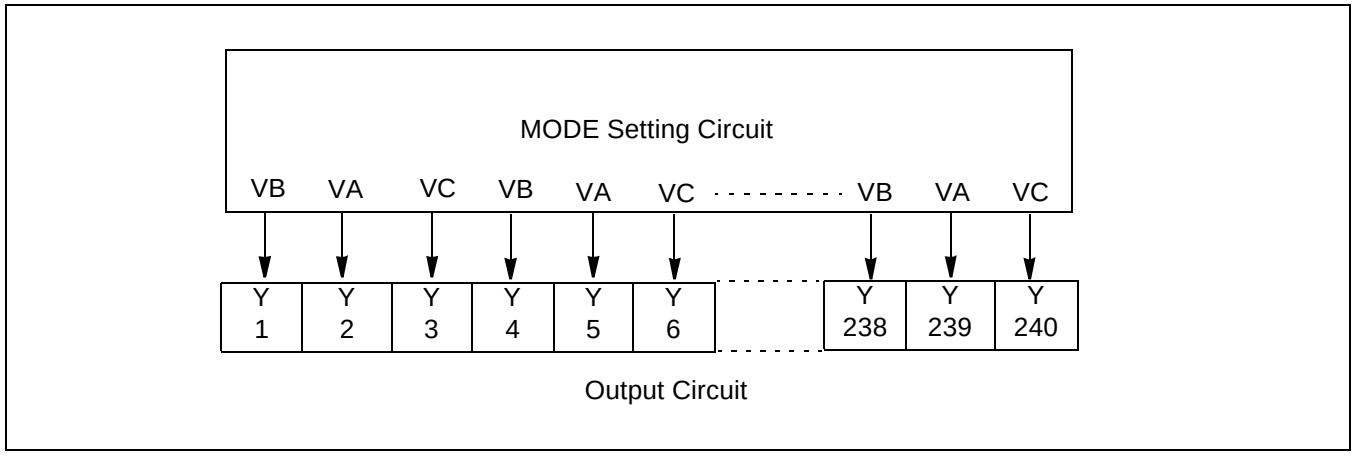
- **When SHL = "H",**
  Connect the previous DIO2 pin to the next DIO1 pin and connect input pin besides DIO1 and DIO2 to each device equally.

- **When SH L= "L",**
  Connect the previous DIO1 pin to the next DIO2 pin and connect input pin besides DIO1 and DIO2 to each device equally.

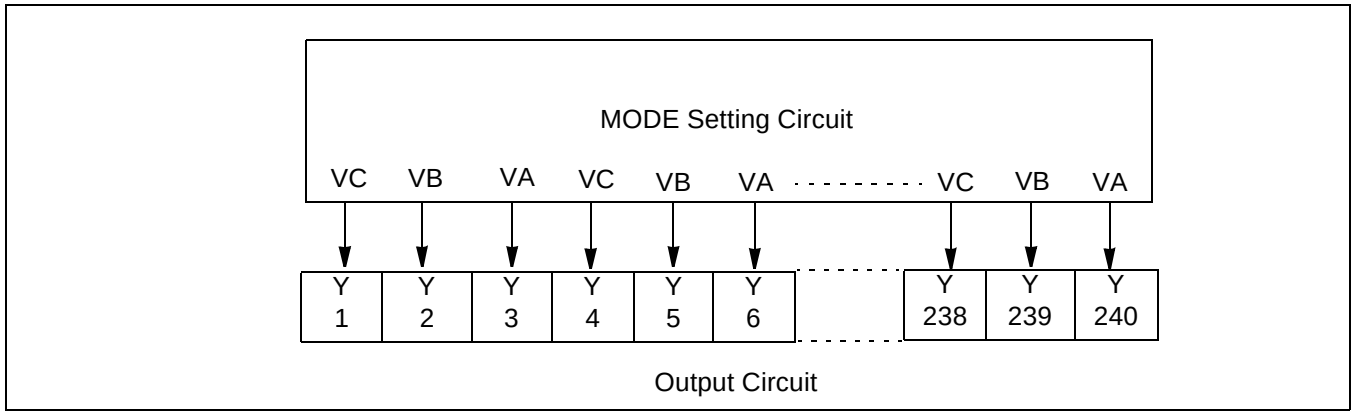
VIDEO SIGNAL MODE SETTING FUNCTION

The order of video signal corresponding to each output pin can be set as shown in the diagram below by changing the mode signal.

- **MODE = "H"**

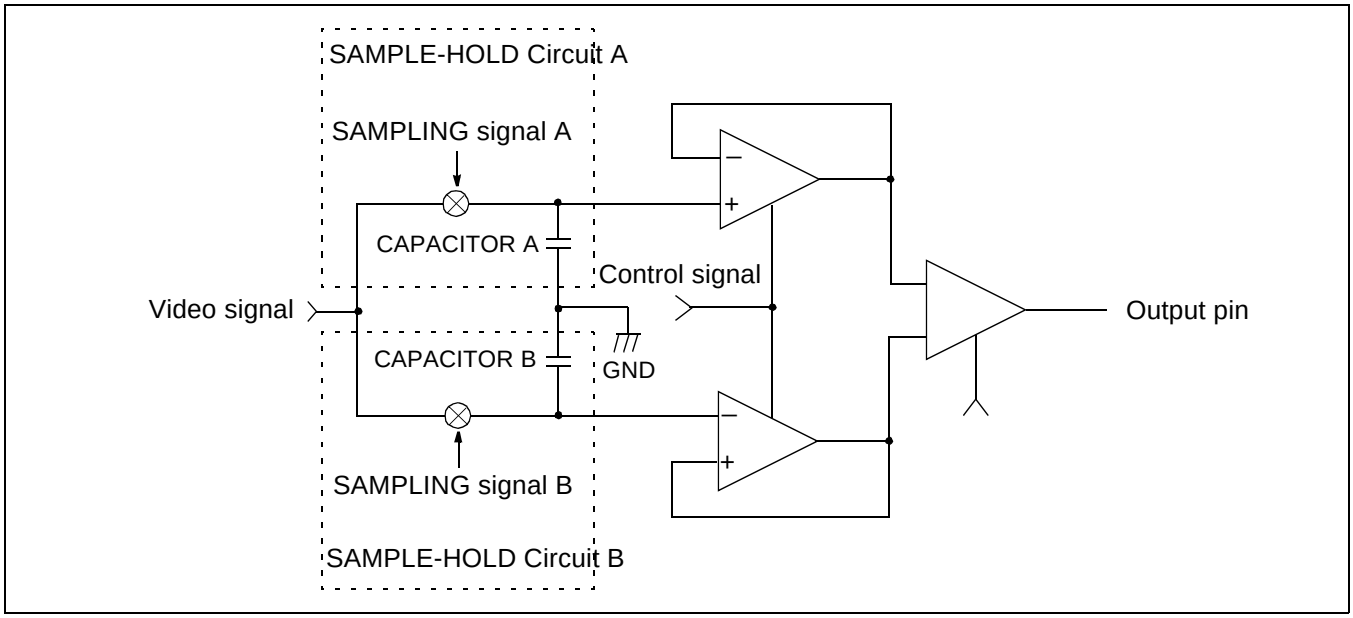


- **MODE = "L"**

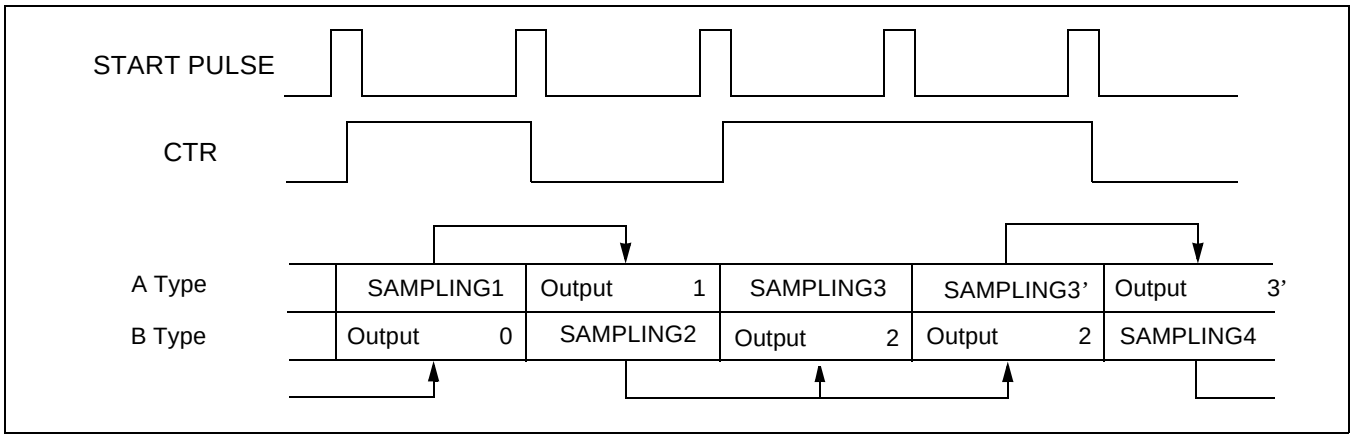


OUTPUT CIRCUIT CONFIGURATION

The KS0606 samples the video signal through 2 types of SAMPLE-HOLD circuit and outputs bi-directionally the voltage corresponding to this sampled data.
The diagrams below show the SAMPLE-HOLD and output circuits.
When CTR = “H”, SAMPLE-HOLD circuit A samples and SAMPLE-HOLD circuit B outputs the voltage sampled in capacitor B.
When CTR = “L”, SAMPLE-HOLD circuit B samples and SAMPLE-HOLD circuit A outputs the voltage sampled in capacitor A.



Therefore, sampling and output operations need to change the CRT signal repeatly to either “H” or “L” at every start pulse.
Also, Set to “H” or “L” at every more-than-one start pulse, the output voltage is the same voltage during this interval. The output voltage corresponds to the data sampled in previous.
The following shows the timing.

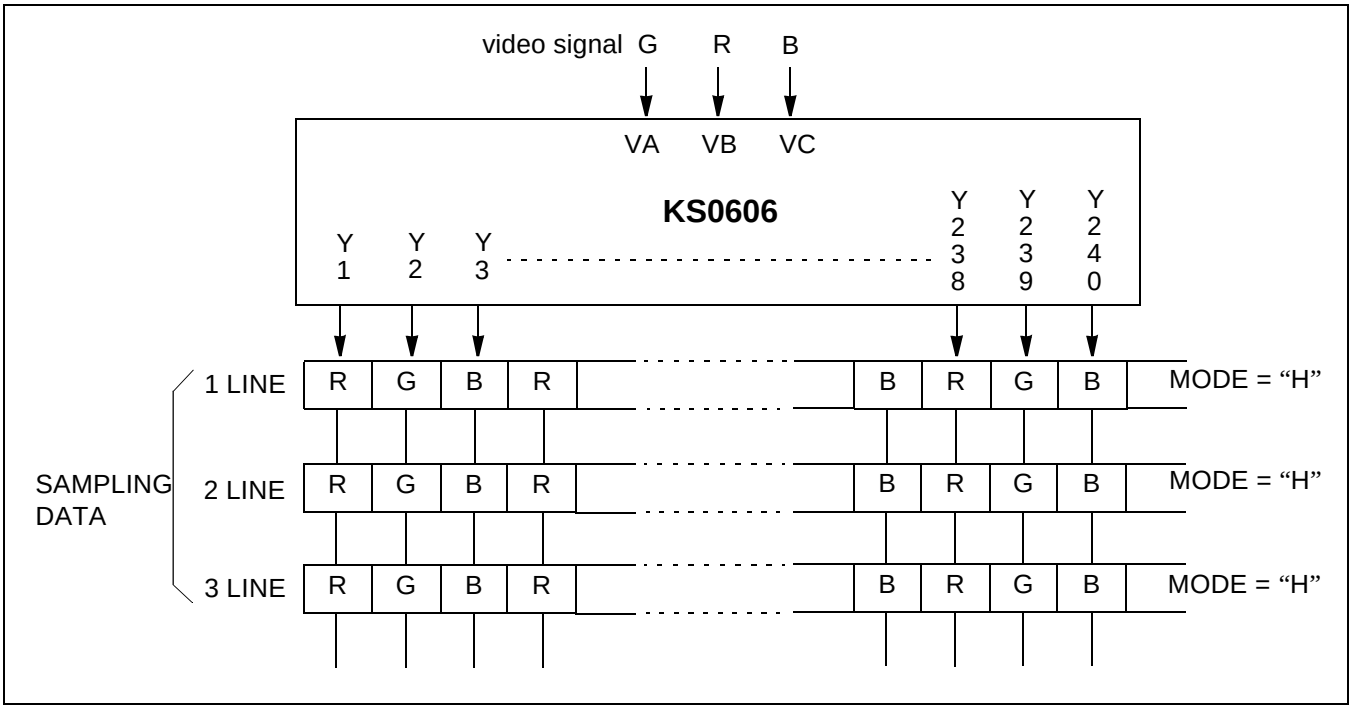


Also, the POWER SAVE function lowers the OP-AMP power consumption at the same time the output pin becomes HIGH IMPEDANCE when the PS pin is “L”. When using this function, the quality indication should be thoroughly reviewed.

EXAMPLE OF LIQUID CRYSTAL PANEL CONNECTION

According to video signal mode setting function in 5 page, connections to STRIPE and DELTA array panels are possible.

(1) STRIPE Array Panel Connection



Video signal Input pin Connection

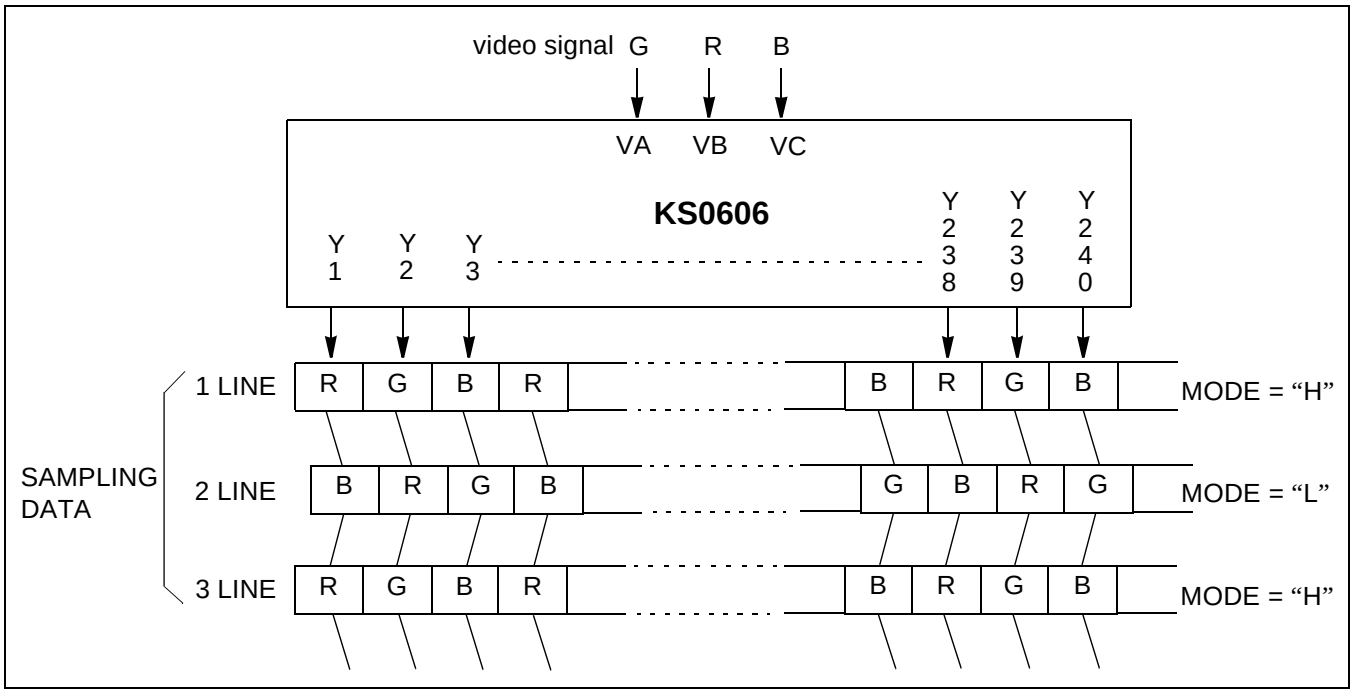
Video signal input pin	VA	VB	VC
Video signal	G	R	B

Video signal sampled by the SAMPLE-HOLD circuit and Mode Setting

	1LINE	2LINE	3LINE	4LINE and after
Y(3n+1)	R	R	R	R
Y (3n+2)	G	G	G	G
Y (3n+3)	B	B	B	B
MODE Setting	"H"	"H"	"H"	"H"

(n=o, 1, 2, ..., 79)

(2) DELTA Array Panel Connection



Video signal Input pin Connection

Video signal input pin	VA	VB	VC
Video signal	G	R	B

Video signal sampled by the SAMPLE-HOLD circuit and Mode Setting

	1LINE	2LINE	3LINE	4LINE and lower
Y(3n+1)	R	B	R	B⇔R interchangeable
Y(3n+2)	G	R	G	R⇔G interchangeable
Y(3n+3)	B	G	B	G⇔B interchangeable
MODE Setting	"H"	"L"	"H"	"L" ⇔ "H" interchangeable

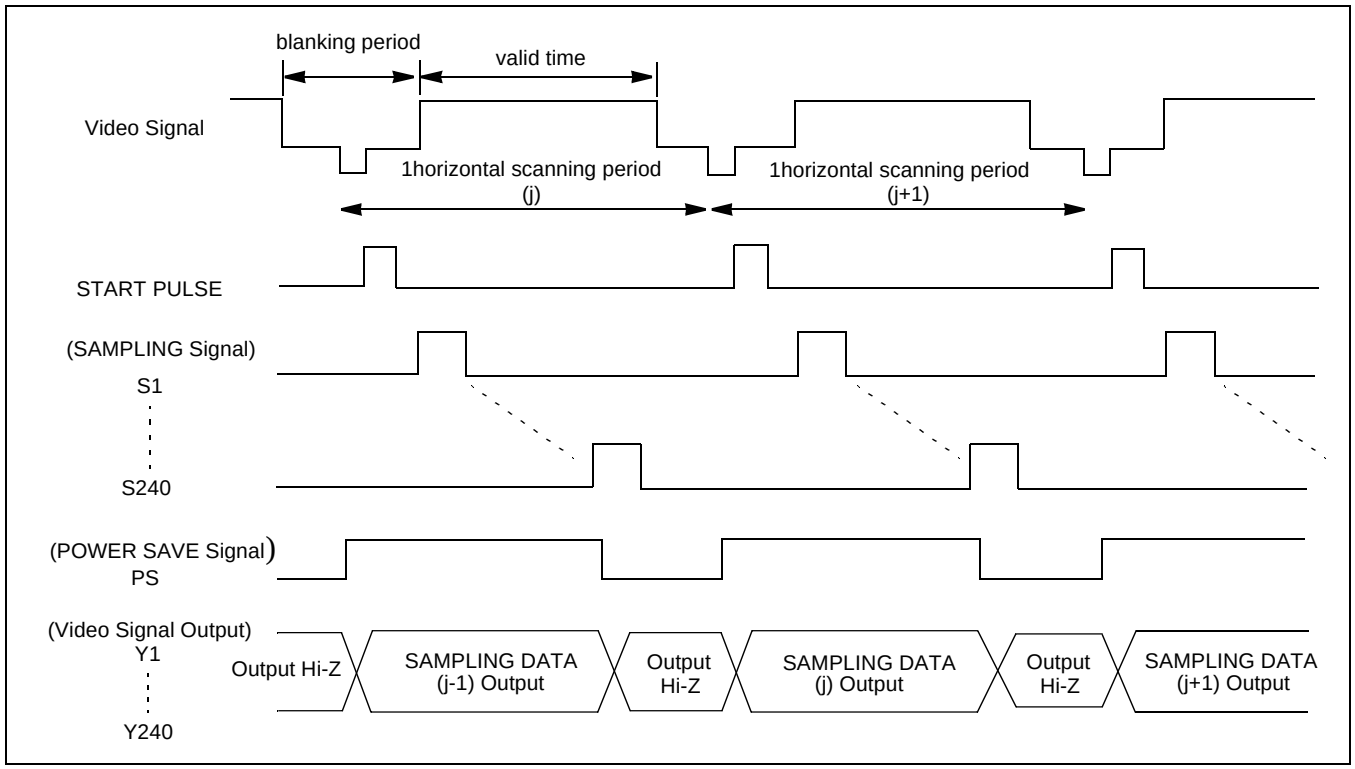
(n=o, 1, 2, ..., 79)

NOTES:

1. MODE setting is changed during blanking period.
2. To the CLK pin horizontal SHIFT CLOCK signal inputs by adjusting to the straying of the display pixel, connected to the same SOURCE BUS LINE, and delaying the phase every 1LINE.
   If the SOURCE BUS LINE connected, display pixel stray is half pixel, then delay the phase by 180°.
   Also, phase is delayed during a cycle.

OPERATING TIMING OUTLINE

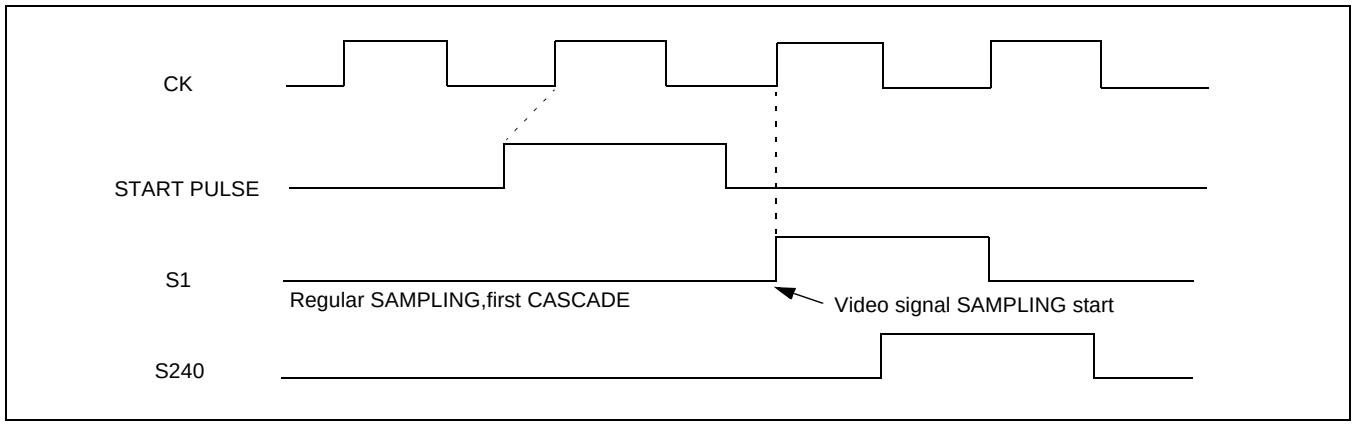
(1) Full Operating Timing



Samples a video signal based on the internal sampling pulse timing during 1 horizontal scanning period in each SAMPLE-HOLD circuit of the output circuit and outputs values corresponding to the sampling data.

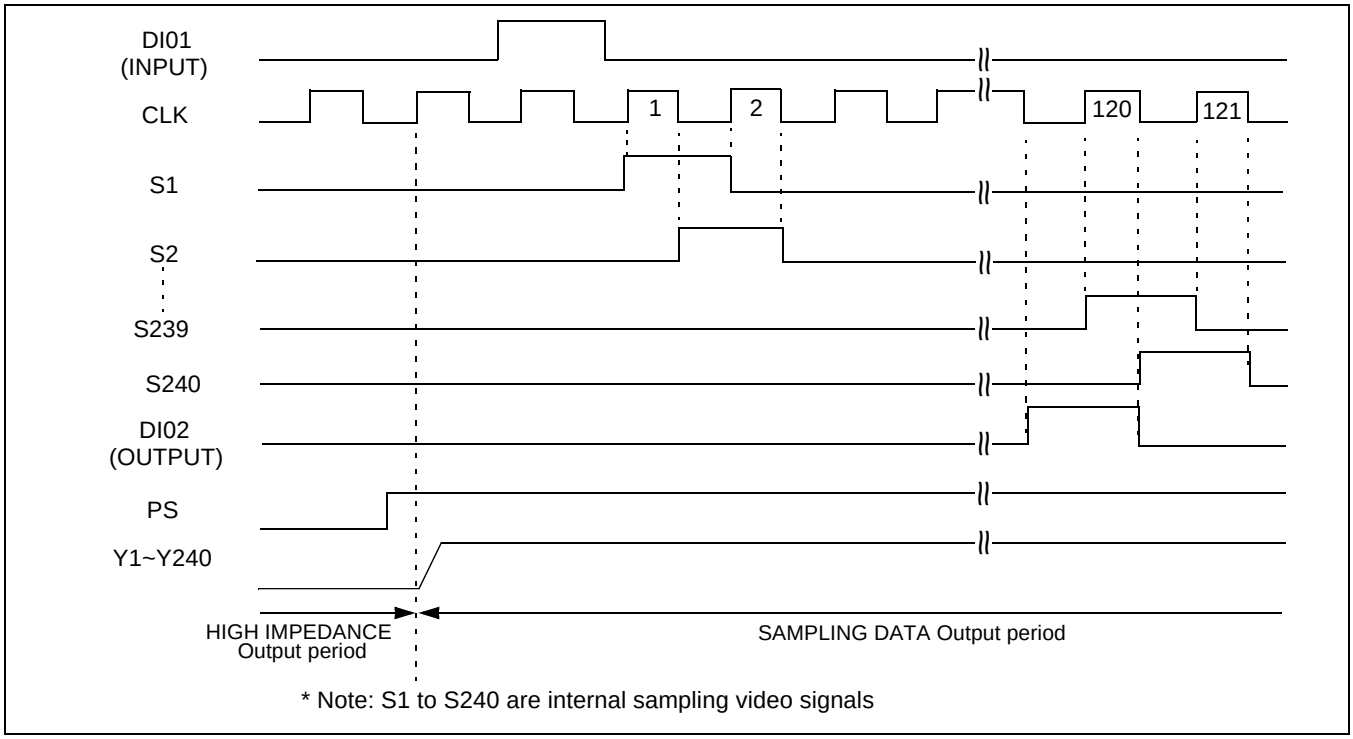
(2) Video Signal SAMPLING Start Timing

The video signal sampling(the internal sampling signal Sn) is general sampling with the first CASCADE and it starts after the START PULSE FALLING at the very first CLOCK RISING.



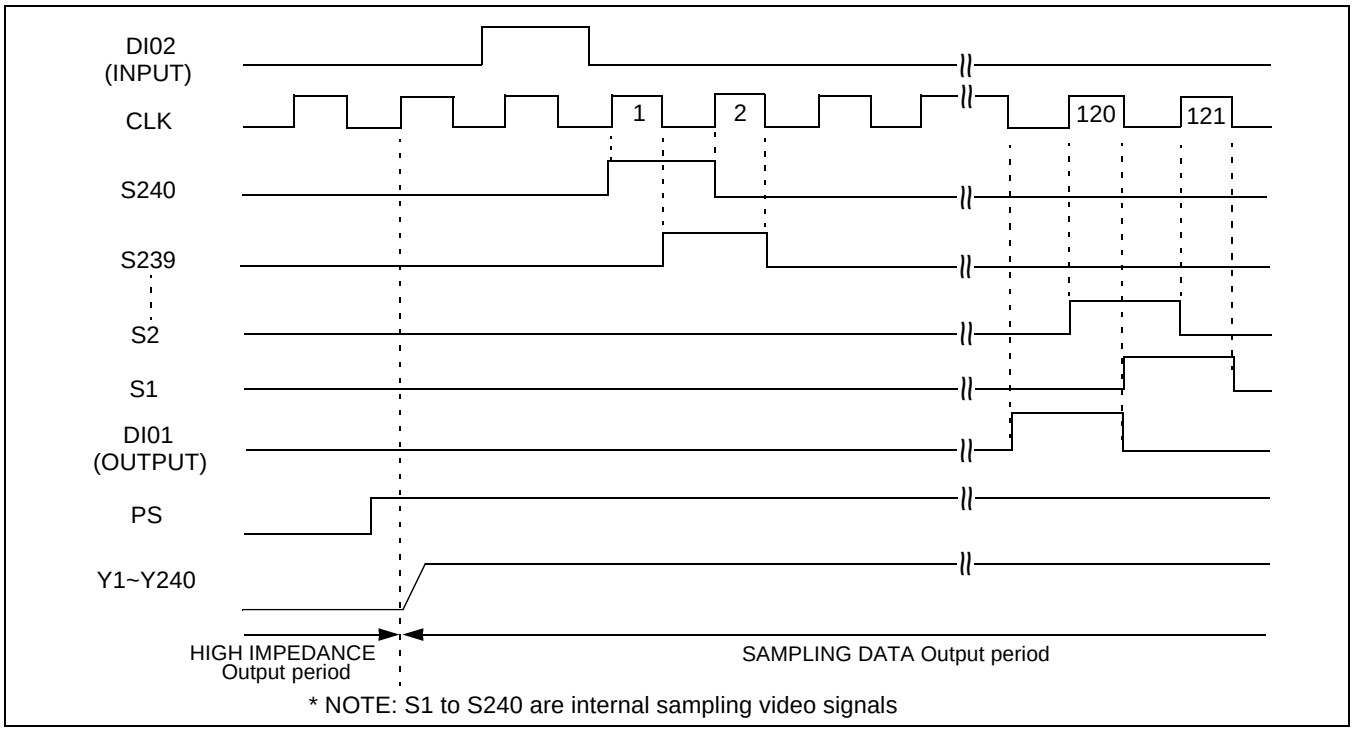
Regular SAMPLING Timing

- SHL = “H”



* Note: S1 to S240 are internal sampling video signals

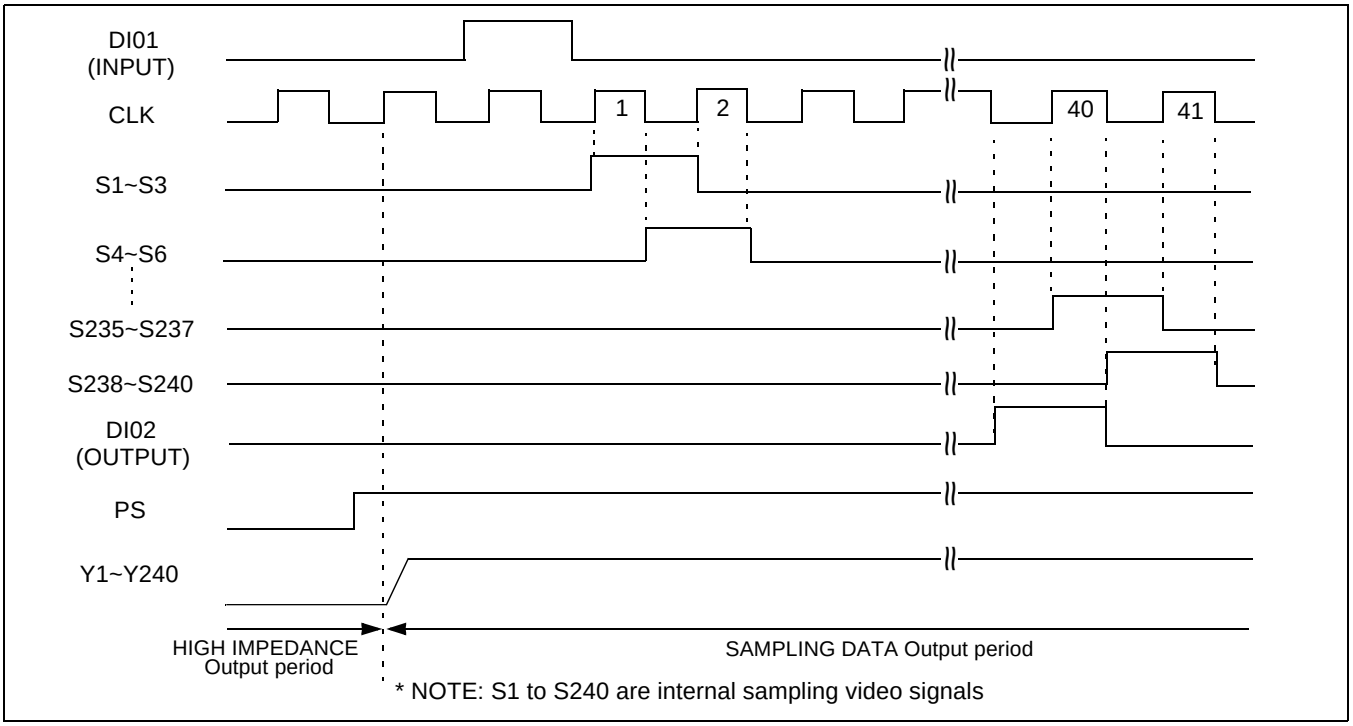
- SHL = “L”



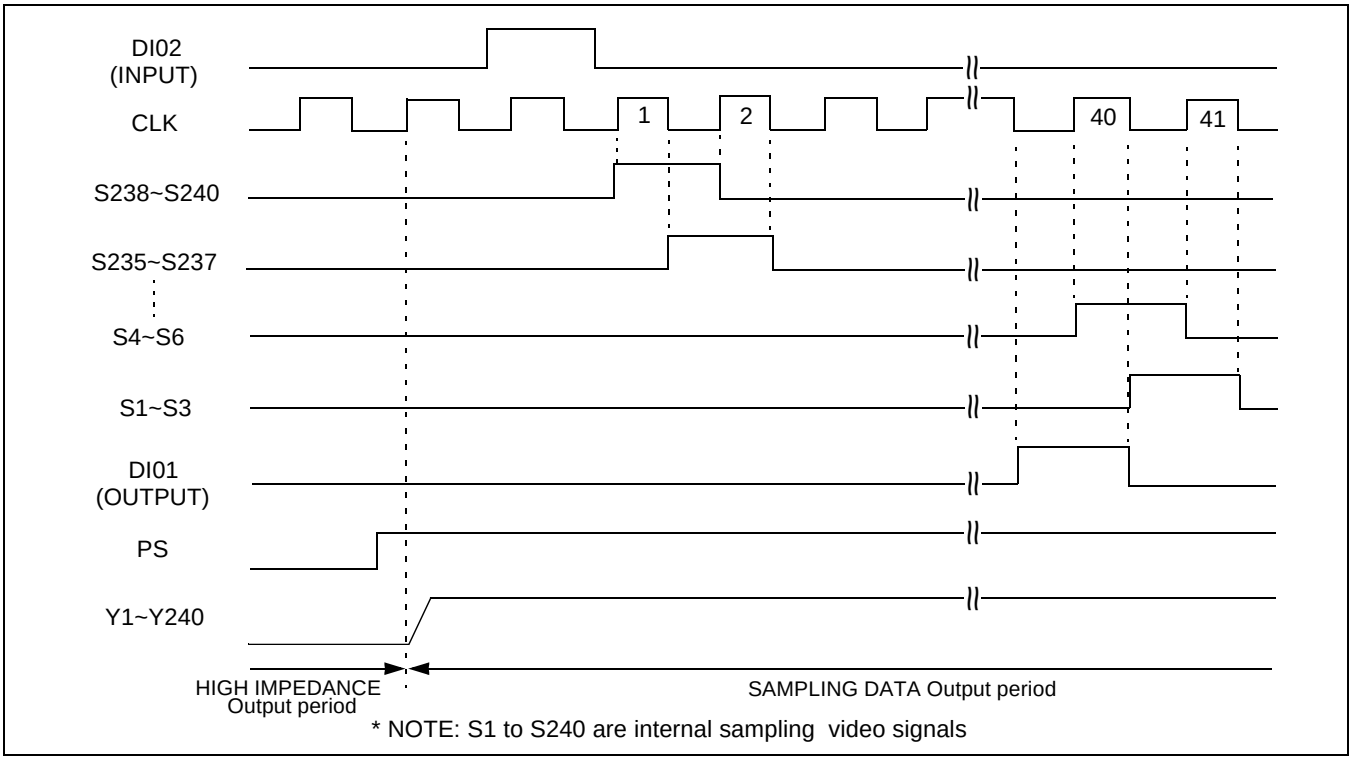
* NOTE: S1 to S240 are internal sampling video signals

POINTS SIMULTANEOUS SAMPLING TIMING

- SHL = “H”



- SHL = “L”



CAUTIONARY ITEMS

Input pin Setting

Because input pin DIO1, DIO2, CLK, CTR and MODE don't have either pull-up or pull-down inside LSI, these absolutely should not be used "OPEN".
Also, VA,VB and VC pin are for video signal inputs so required video inputs must be entered.

Except for VA, VB, VC, DIO1, DIO2, CLK, CTR and MODE, recommend all other inputs which have pull-up inside LSI, are set as either "H" or "L" and should not be used as "OPEN" to prevent malfunction due to noise etc.

Input Video Signal

The input video signals targets ANALOG signals(continuous signal).
Also, the video signal input frequency is possible up to a maximum of 12.5MHz.

BY-PASS Capacitor

When the LOGIC-side NOISE overlaps in the analog circuit of sample-hold circuits etc., analog characteristics (output voltage deviation, dynamic range etc.) can go bad so about 1μF BY-PASS CAPACITOR is inserted between VDD-VSS.
BY-PASS CAPACITOR value should be decided after sufficiently evaluating it,installed in an actual liquid crystal panel.

ABSOLUTE MAXIMUM RATING

(V_{SS1}=V_{SS2}=0 V)

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	V_{DD1}, V_{DD2}	–0.3 to +7.0	V
Input Voltage	VIN	–0.3 to V_{DD2}+0.3 (note 1)	V
		–0.3 to V_{DD1}+0.3 (note 2)	
Storage Temperature Range	Tstg	–45 to + 125	°C

If the device is used in excess of the above absolute ratings, it can be permanently damaged.
Voltage has V_{SS1} = V_{SS2} = 0V as reference.

NOTES:
1. VA,VB,VC and TEST5 Terminal
2. DIO1 to DIO2, CLK, SHL, CTR, SAM, TEST1 to TEST4, MODE, and PS Terminal

RECOMMENDED OPERATING RANGE

(Ta = –30°C to +85°C, V_{SS1} = V_{SS2} = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD1}	–	3.0	–	5.5	V
	V_{DD2}	–	3.0	–	5.5	V
Input Voltage	VIN	–	0	–	V_{DD1}/V_{DD2} (note)	V
Operating Temperature	Topr	–	–30	–	+85	°C

Voltages V_{SS1} and V_{SS2} have 0V as reference.
Power Supply voltage relationship: $V_{DD1} \leq V_{DD2}$

NOTE: At input voltage, VIN MAX, the VA, VB, VC, and TEST5 = V_{DD2}
DIO1 to DIO2, CLK, SHL, CTR, SAM, TEST1 to TEST4, MODE, and PS = V_{DD1}.

DC CHARACTERISTICS

(Ta = -30°C to +85°C, V_{DD1}=3.0V to 5.5V, V_{DD2}=3.0V to 5.5V, V_{SS1}=V_{SS2}=0V)

Parameter	Symbol	Condition/Applied Pin	Min.	Typ.	Max.	Unit
HIGH LEVEL Input Voltage	VIH	CLK, CTR, DIO1, DIO2, MODE, SHL, SAM, PS, TEST1 to 4	0.7V_{DD1}	–	V_{DD1}	V
LOW LEVEL Input Voltage	VIL		0	–	0.3V_{DD1}	
LOW LEVEL Input Current	IL1	CLK, CTR, DIO1, DIO2, MODE, TEST5 (VIN = 0V)	–	–	10	µA
	IL2	SHL, SAM, PS, TEST1 to 4 (VIN = V_{DD1}/V_{DD2})	–	–	400	µA
HIGH LEVEL Input Current	IH1	CLK,CTR,DIO1,DIO2,MODE, TEST5 SHL,SAM,PS,TEST1~4	–	–	10	µA
DYNAMIC RANGE	Vpp	VA, VB, VC	0.1	–	V_{DD1}-0.1	V
Output Voltage Deviation	ΔVO	(Note 1)	–20.0	–	20.0	mV
Current Consumption	IDDH1	At operation, V_{DD2}, (Note 2)	–	–	5.0	mA
	IDDH2	POWER SAVE,V_{DD2},(Note 3)	–	–	100	µA
	IDDL1	V_{DD1},(Note 2)	–	–	3	mA

NOTES:

1. START PULSE : Cycle t_{DIO} = 63.5µs
   CTR signal: Cycle t_{CTR} = 127.0µs
   Interchange “H” and “L” during blanking period
   CLK signal: frequency fCLK = 12.5 MHz
   VA = VB = VC = 0.1V to V_{DD2}-0.1V
   TEST5 = V_{DD2}
   Connect all other input pin to V_{DD1}/V_{DD2}
   Difference between the output voltage of each pin and average output voltage of all output pin in the chip.

2. START PULSE: cycle t_{DIO} = 63.5µs
   CTR signal: cycle t_{CTR}= 127.0µs
   Interchange “H” and “L” during blanking period
   CLK signal: frequency fCLK = 12.5 MHz
   Among the remaining input pin VA, VB, VC, TEST5 = V_{DD2} and all other input pin = V_{DD1}
   V_{DD1} = 3.3V, V_{DD2} = 5.0V

3. START PULSE: cycle t_{DIO} = 63.5µs
   CTR signal: cycle t_{CTR} = 127.0µs
   Interchange “H” and “L” during blanking period
   CLK signal frequency: fCLK = 12.5 MHz
   Pin set to GROUND: PS
   Among the remaining input pin VA, VB, VC, TEST5 = V_{DD2} and all other input pin = V_{DD1}.
   V_{DD1} = 3.3V, V_{DD2} = 5.0V

AC CHARACTERISTICS

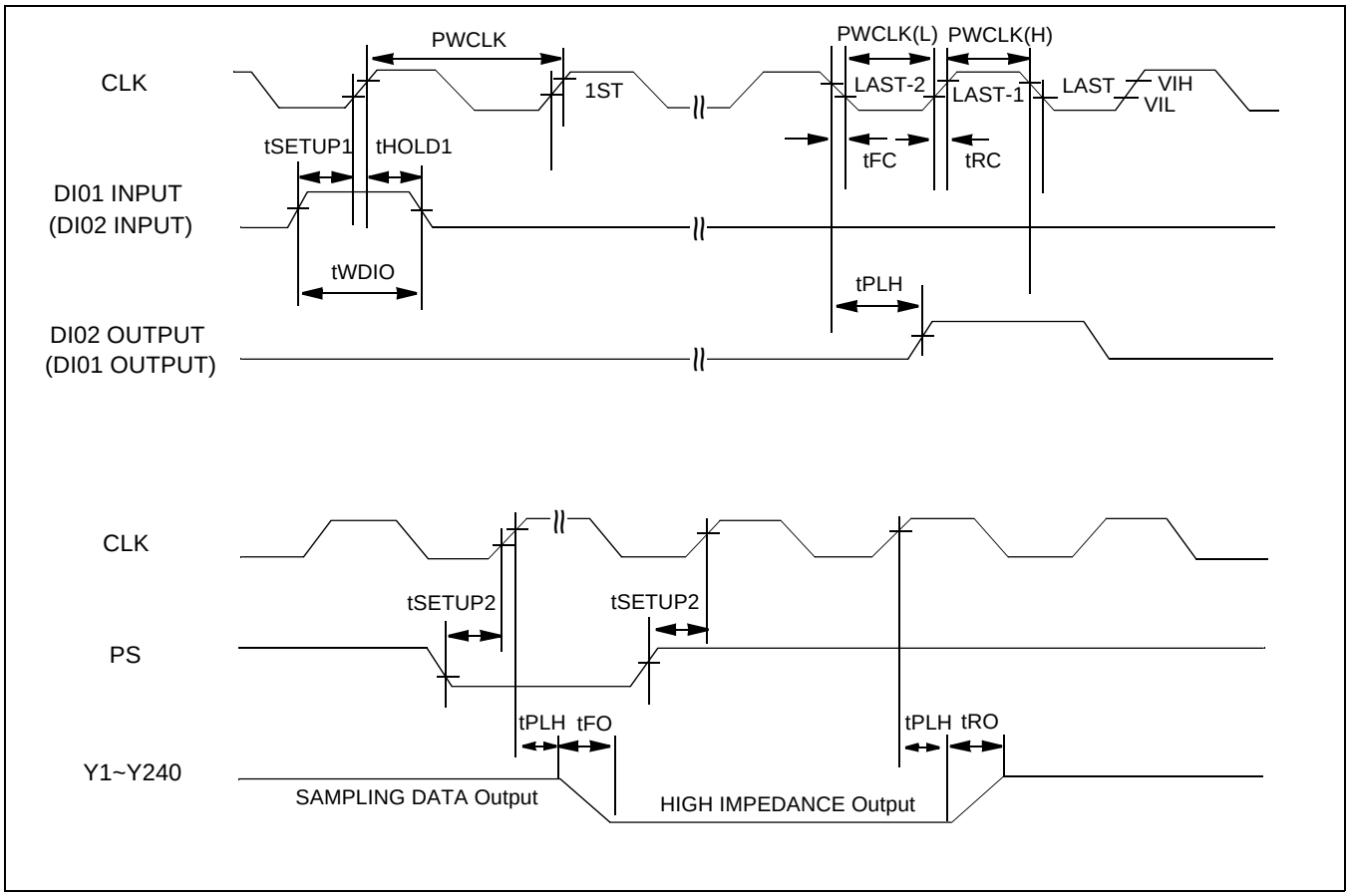
(Ta=-30°C to +85°C, V_{DD1}=3.0V~5.5V, V_{DD2}=3.0V~5.5V, V_{SS1}=V_{SS2}=0V)

Paratmeter	Symbol	Condition/Applied Pin	Min.	Typ.	Max.	Unit.
CLOCK frequency	fCLK	SAM = "H"/ CLK	–	–	12.5	MHz
		SAM = "L"/ CLK	–	–	7.0	MHz
CLOCK HIGH period	PWCLK(H)	SAM = "H"/ CLK	30	–	–	ns
		SAM = "L"/ CLK	50	–	–	ns
CLOCK LOW period	PWCLK(L)	SAM = "H"/ CLK	30	–	–	ns
		SAM = "L"/ CLK	50	–	–	ns
Input RISING time	tRC	SAM = "H"/ CLK,DIO1,DIO2	–	–	10	ns
		SAM = "L"/ CLK,DIO1,DIO2	–	–	20	ns
Input FALLING time	tFC	SAM = "H"/ CLK,DIO1,DIO2	–	–	10	ns
		SAM = "L"/ CLK,DIO1,DIO2	–	–	20	ns
START PULSE width	tWDIO	DIO1, DIO2	–	–	1/fCLK	ns
START PULSE SET-UP time	tSETUP1	DIO1, DIO2	15	–	–	ns
START PULSE HOLD time	tHOLD1	DIO1, DIO2	15	–	–	ns
START PULSE Output delay time	tPLH	CL = 15pF/ DIO1,DIO2	–	–	15	ns
PS signal SET-UP time	tSETUP2	PS	1/fCLK	–	–	ns
Output delay time	tPHL	CL = 150pF, Y1 to Y240, * Note 1	–	–	5/fCLK	ns
Output RISING time	tRO		–	10	20	µs
Output FALLING time	tFO		–	10	20	µs

NOTE:

1. START PPLSE signal cycle: t_{DIO} = 63.5µs
   CTR signal cycle: t_{CTR} = 127.0µs
   "H" ⇔ "L" interchange during blanking period
   CLK signal frequency: fCLK = 12.5MHz
   Among the remaining input pin VA, VB, VC,TEST5 = V_{DD2} and all other input pin = V_{DD1}
   V_{DD1} = 3.3V, V_{DD2} = 5.0V

AC Timing diagram (VIH = 0.7V_{DD1}, VIL = 0.3V_{DD1})



PAD COORDINATES

Table 1. PAD Coordinates

Pin Name	X (㎛)	Y (㎛)	Pin Name	X (㎛)	Y (㎛)	Pin Name	X (㎛)	Y (㎛)	Pin Name	X (㎛)	Y (㎛)
V_{DD2}	8160	95	Y33	5687	542	Y72	3152	542	Y111	617	542
V_{DD2}	8160	165	Y34	5622	542	Y73	3087	542	Y112	552	542
V_{DD2}	8160	235	Y35	5557	542	Y74	3022	542	Y113	487	542
V_{DD2}	8160	305	Y36	5492	542	Y75	2957	542	Y114	422	542
V_{DD2}	8160	375	Y37	5427	542	Y76	2892	542	Y115	357	542
V_{DD2}	8160	445	Y38	5362	542	Y77	2827	542	Y116	292	542
V_{DD2}	8160	515	Y39	5297	542	Y78	2762	542	Y117	227	542
Y1	7767	542	Y40	5232	542	Y79	2697	542	Y118	162	542
Y2	7702	542	Y41	5167	542	Y80	2632	542	Y119	97	542
Y3	7637	542	Y42	5102	542	Y81	2567	542	Y120	32	542
Y4	7572	542	Y43	5037	542	Y82	2502	542	Y121	-32	542
Y5	7507	542	Y44	4972	542	Y83	2437	542	Y122	-97	542
Y6	7442	542	Y45	4907	542	Y84	2372	542	Y123	-162	542
Y7	7377	542	Y46	4842	542	Y85	2307	542	Y124	-227	542
Y8	7312	542	Y47	4777	542	Y86	2242	542	Y125	-292	542
Y9	7247	542	Y48	4712	542	Y87	2177	542	Y126	-357	542
Y10	7182	542	Y49	4647	542	Y88	2112	542	Y127	-422	542
Y11	7117	542	Y50	4582	542	Y89	2047	542	Y128	-487	542
Y12	7052	542	Y51	4517	542	Y90	1982	542	Y129	-552	542
Y13	6987	542	Y52	4452	542	Y91	1917	542	Y130	-617	542
Y14	6922	542	Y53	4387	542	Y92	1852	542	Y131	-682	542
Y15	6857	542	Y54	4322	542	Y93	1787	542	Y132	-747	542
Y61	6792	542	Y55	4257	542	Y94	1722	542	Y133	-812	542
Y17	6727	542	Y56	4192	542	Y95	1657	542	Y134	-877	542
Y18	6662	542	Y57	4127	542	Y96	1592	542	Y135	-942	542
Y19	6597	542	Y58	4062	542	Y97	1527	542	Y136	-1007	542
Y20	6532	542	Y59	3997	542	Y98	1462	542	Y137	-1072	542
Y21	6467	542	Y60	3932	542	Y99	1397	542	Y138	-1137	542
Y22	6402	542	Y61	3867	542	Y100	1332	542	Y139	-1202	542
Y23	6337	542	Y62	3802	542	Y101	1267	542	Y140	-1267	542
Y24	6272	542	Y63	3737	542	Y102	1202	542	Y141	-1332	542
Y25	6207	542	Y64	3672	542	Y103	1137	542	Y142	-1397	542
Y26	6142	542	Y65	3607	542	Y104	1072	542	Y143	-1462	542

Table 1. PAD Coordinates (Continued)

Pin Name	X (㎛)	Y (㎛)	Pin Name	X (㎛)	Y (㎛)	Pin Name	X (㎛)	Y (㎛)	Pin Name	X (㎛)	Y (㎛)
Y27	6077	542	Y66	3542	542	Y105	1007	542	Y144	-1527	542
Y28	6012	542	Y67	3477	542	Y106	942	542	Y145	-1592	542
Y29	5947	542	Y68	3412	542	Y107	877	542	Y146	-1657	542
Y30	5882	542	Y69	3347	542	Y108	812	542	Y147	-1722	542
Y31	5817	542	Y70	3282	542	Y109	747	542	Y148	-1787	542
Y32	5752	542	Y71	3217	542	Y110	682	542	Y149	-1852	542
Y150	-1917	542	Y192	-4647	542	Y234	-7377	542	V_{DD2}	-5680	-504
Y151	-1982	542	Y193	-4712	542	Y235	-7442	542	MONC1	-5520	-504
Y152	-2047	542	Y194	-4777	542	Y236	-7507	542	MONC1	-5440	-504
Y153	-2112	542	Y195	-4842	542	Y237	-7572	542	MONC1	-5360	-504
Y154	-2177	542	Y196	-4907	542	Y238	-7637	542	MONC1	-5280	-504
Y155	-2242	542	Y197	-4972	542	Y239	-7702	542	V_{DD1}	-5120	-504
Y156	-2307	542	Y198	-5037	542	Y240	-7767	542	V_{DD1}	-5040	-504
Y157	-2372	542	Y199	-5102	542	V_{DD2}	-8160	515	V_{DD1}	-4960	-504
Y158	-2437	542	Y200	-5167	542	V_{DD2}	-8160	445	V_{DD1}	-4880	-504
Y159	-2502	542	Y201	-5232	542	V_{DD2}	-8160	375	V_{SS1}	-4720	-504
Y160	-2567	542	Y202	-5297	542	V_{DD2}	-8160	305	V_{SS1}	-4640	-504
Y161	-2632	542	Y203	-5362	542	V_{DD2}	-8160	235	V_{SS1}	-4560	-504
Y162	-2697	542	Y204	-5427	542	V_{DD2}	-8160	165	V_{SS1}	-4480	-504
Y163	-2762	542	Y205	-5492	542	V_{DD2}	-8160	95	VC	-4305	-504
Y164	-2827	542	Y206	-5557	542	V_{SS2}	-8160	-54	VC	-4200	-504
Y165	-2892	542	Y207	-5622	542	V_{SS2}	-8160	-124	VC	-4095	-504
Y166	-2957	542	Y208	-5687	542	V_{SS2}	-8160	-194	VC	-3905	-504
Y167	-3022	542	Y209	-5752	542	V_{SS2}	-8160	-264	VC	-3800	-504
Y168	-3087	542	Y210	-5817	542	V_{SS2}	-8160	-334	VC	-3695	-504
Y169	-3152	542	Y211	-5882	542	V_{SS2}	-8160	-404	VB	-3505	-504
Y170	-3217	542	Y212	-5947	542	V_{SS2}	-8160	-474	VB	-3400	-504
Y171	-3282	542	Y213	-6012	542	MONA1	-7840	-504	VB	-3295	-504
Y172	-3347	542	Y214	-6077	542	MONA2	-7680	-504	VB	-3105	-504
Y173	-3412	542	Y215	-6142	542	V_{SS2}	-7520	-504	VB	-3000	-504
Y174	-3477	542	Y216	-6207	542	V_{SS2}	-7440	-504	VB	-2895	-504
Y175	-3542	542	Y217	-6272	542	V_{SS2}	-7360	-504	VA	-2705	-504
Y176	-3607	542	Y218	-6337	542	V_{SS2}	-7280	-504	VA	-2600	-504
Y177	-3672	542	Y219	-6402	542	V_{SS2}	-7120	-504	VA	-2495	-504

Table 1. PAD Coordinates (Continued)

Pin Name	X (㎜)	Y (㎜)	Pin Name	X (㎜)	Y (㎜)	Pin Name	X (㎜)	Y (㎜)	Pin Name	X (㎜)	Y (㎜)
Y178	-3737	542	Y220	-6467	542	V_{SS2}	-7040	-504	VA	-2305	-504
Y179	-3802	542	Y221	-6532	542	V_{SS2}	-6960	-504	VA	-2200	-504
Y180	-3867	542	Y222	-6597	542	V_{SS2}	-6880	-504	VA	-2095	-504
Y181	-3932	542	Y223	-6662	542	V_{DD2}	-6720	-504	TEST5	-1905	-504
Y182	-3997	542	Y224	-6727	542	V_{DD2}	-6640	-504	TEST5	-1800	-504
Y183	-4062	542	Y225	-6792	542	V_{DD2}	-6560	-504	TEST5	-1695	-504
Y184	-4127	542	Y226	-6857	542	V_{DD2}	-6480	-504	MODE	-1505	-504
Y185	-4192	542	Y227	-6922	542	V_{DD2}	-6320	-504	MODE	-1400	-504
Y186	-4257	542	Y228	-6987	542	V_{DD2}	-6240	-504	MODE	-1295	-504
Y187	-4322	542	Y229	-7052	542	V_{DD2}	-6160	-504	PS	-1105	-504
Y188	-4387	542	Y230	-7117	542	V_{DD2}	-6080	-504	PS	-1000	-504
Y189	-4452	542	Y231	-7182	542	V_{DD2}	-5920	-504	PS	-895	-504
Y190	-4517	542	Y232	-7247	542	V_{DD2}	-5840	-504	CTR	-705	-504
Y191	-4582	542	Y233	-7312	542	V_{DD2}	-5760	-504	CTR	-600	-504
CTR	-495	-504	V_{DD1}	5120	-504						
CLK	-305	-504	MONC2	5280	-504						
CLK	-200	-504	MONC2	5360	-504						
CLK	-95	-504	MONC2	5440	-504						
CLK	95	-504	V_{DD2}	5680	-504						
CLK	200	-504	V_{DD2}	5760	-504						
CLK	305	-504	V_{DD2}	5840	-504						
DI01	495	-504	V_{DD2}	5920	-504						
DI01	600	-504	V_{DD2}	6080	-504						
DI01	705	-504	V_{DD2}	6160	-504						
DI01	1000	-504	V_{DD2}	6240	-504						
DI01	1105	-504	V_{DD2}	6320	-504						
DI02	1295	-504	V_{SS2}	6480	-504						
DI02	1400	-504	V_{SS2}	6560	-504						
DI02	1505	-504	V_{SS2}	6640	-504						
DI02	1800	-504	V_{SS2}	6720	-504						
DI02	1905	-504	V_{SS2}	6880	-504						
SHL	2095	-504	V_{SS2}	6960	-504						
SHL	2200	-504	V_{SS2}	7040	-504						
SHL	2305	-504	V_{SS2}	7120	-504						

Table 1. PAD Coordinates (Continued)

Pin Name	X (㎜)	Y (㎜)	Pin Name	X (㎜)	Y (㎜)	Pin Name	X (㎜)	Y (㎜)	Pin Name	X (㎜)	Y (㎜)
SAM	2495	-504	V_{SS2}	7280	-504						
SAM	2600	-504	V_{SS2}	7360	-504						
SAM	2705	-504	V_{SS2}	7440	-504						
TEST4	2895	-504	V_{SS2}	7520	-504						
TEST4	3000	-504	MOVB1	7680	-504						
TEST4	3105	-504	MOVB1	7840	-504						
TEST3	3295	-504	V_{SS2}	8160	-474						
TEST3	3400	-504	V_{SS2}	8160	-404						
TEST3	3505	-504	V_{SS2}	8160	-334						
TEST2	3695	-504	V_{SS2}	8160	-264						
TEST2	3800	-504	V_{SS2}	8160	-194						
TEST2	3905	-504	V_{SS2}	8160	-124						
TEST1	4095	-504	V_{SS2}	8160	-54						
TEST1	4200	-504									
TEST1	4305	-504									
V_{SS1}	4480	-504									
V_{SS1}	4560	-504									
V_{SS1}	4640	-504									
V_{SS1}	4720	-504									
V_{DD1}	4880	-504									
V_{DD1}	4960	-504									
V_{DD1}	5040	-504									

PAD FORMAT

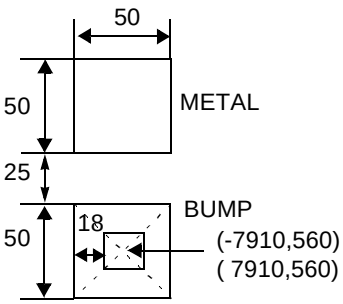
Chip Size(S/L 80μm included)

: 16680 X 1370 [μm^2]

Bump Size

- 40 X 105 : output pads
- 50 x 100 : power pads in short side
- 50 x 100 : input pads
- 60 x 100 : power pads in long side

COG Align Key



BUMP & ILB KEY

(7987.5, -504)

(-7987.5, -504)