INTRODUCTION

64G/S 300/309CH. SOURCE DRIVER

The KS0652 is a source driver for TFT LCD capable of dealing with displays with 64 gray scales.
Data input is based on digital input consisting of 6 bits by 3 dots, which can realize a full color display of 260,000 colors by output of 64 values γ - corrected.

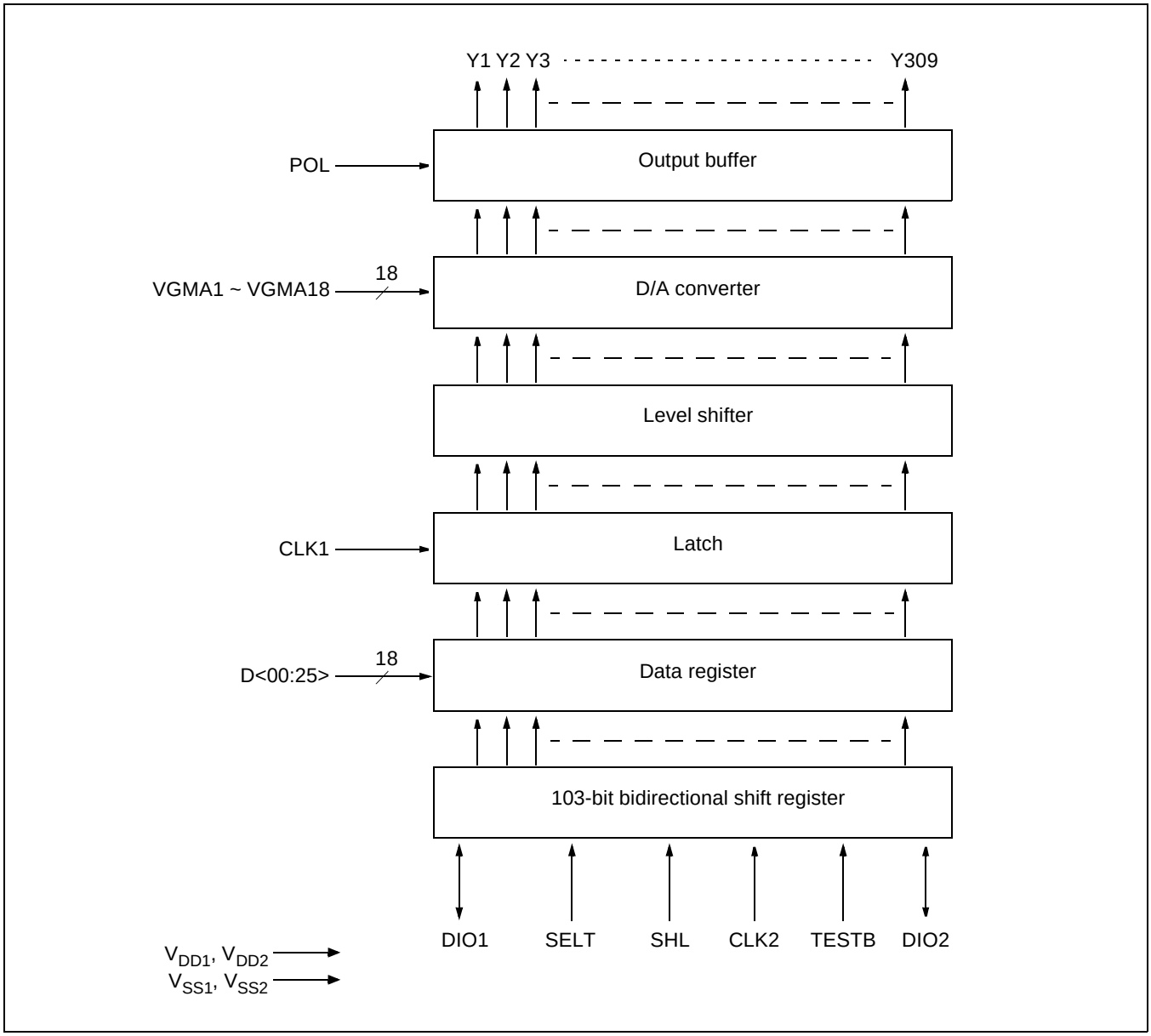
This source driver has an internal D/A converter and 18 (9-by-2) external power supplies.
Because the output dynamic range is as large as 6.0 to 12.6 Vp-p, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot line inversion when mounted on a single side, output gray scale voltages with different polarity can be output to the odd output pins and even output pins.

The KS0652 can be adjusted to be larger panel, and SHL (shift direction selection) pin makes LCD panel connection convenient. Maximum operating clock frequency is 55MHz in a 2.7V logic operation and it can be applied to the TFT LCD panel of SVGA to XGA standards.

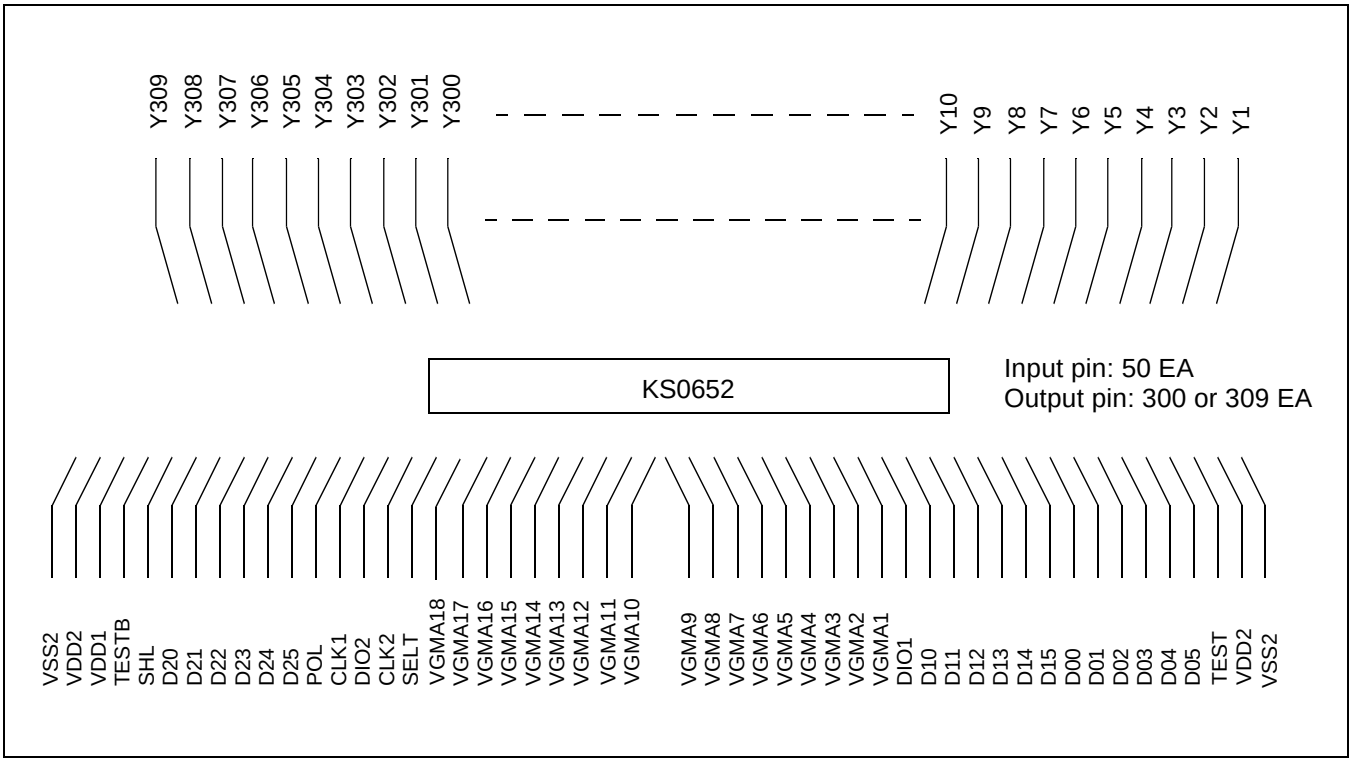
FEATURES

- ❑ Source driver for TFT LCD
- ❑ Capable of outputing 64 values by means of 9-by-2 external power supplies(18 units) and a D/A converter
- ❑ Dot inversion display is possible
- ❑ Pre-chargeless output buffer
- ❑ CMOS level input
- ❑ γ - correction is possible
- ❑ SHL(shift direction selection) pin makes LCD panel connection convenient
- ❑ Input of 6 bits(gray scale data) by 3 dots(R, G, B)
- ❑ Logic supply voltage: 2.7 to 3.6V
- ❑ Driver supply voltage: 6.4 to 13.0V
- ❑ Output dynamic range: 6.0 to 12.6 Vp-p
- ❑ Maximum operating clock frequency:
  f_{MAX} = 55MHz (internal data transfer speed when operating at 2.7V)
- ❑ Selectable 300/309 outputs
- ❑ Slim-type/bent-type TCP

BLOCK DIAGRAM



TCP PIN CONFIGURATION



NOTES:

1. This figure does not specify the dimensions of the TCP package.
2. In actual panel application, the power should be supplied through all the V_{DD2} and V_{SS2} pins simultaneously.

PIN DESCRIPTION

Pin symbol	Pin name	Description
V_{DD1}	Logic power supply	2.7V to 3.6V
V_{DD2}	Driver power supply	6.4V to 13.0V
V_{SS1}	Logic ground	Ground (0V)
V_{SS2}	Driver ground	Ground (0V)
Y1~Y309	Driver output	The D/A converted 64 gray scales analog voltage is output. When using 300 output mode, Y151 to Y159 becomes invalid and there is no output on the corresponding TCP terminal.
D0<0:5> D1<0:5> D2<0:5>	Display data input	The display data is input with a width of 18 bits, gray scale data(6 bits) × 3 dots(R,G,B) DX0 : LSB, DX5 : MSB
SHL	Shift direction select input	This pin controls the direction of shift register in cascade connection. The shift direction of the shift register is as follows: SHL = H: DIO1 input, Y1 → Y309, DIO2 output SHL = L: DIO2 input, Y309 → Y1, DIO1 output
DIO1	Right shift start pulse input/output	SHL = H: Used as the start pulse input pin SHL = L: Used as the start pulse output pin
DIO2	Left shift start pulse input/output	SHL = H: Used as the start pulse output pin SHL = L: Used as the start pulse input pin
CLK2	Shift clock input	Refer to the shift register′s shift clock input. The display data is loaded to the data register at the rising edge of CLK2. At the rising edge of the 103rd clock after start pulse input, the start pulse output reaches the high level, thus providing the start pulse of driver for next stage.
CLK1	Latch input	The contents of the data register are latched at the rising edge of CLK1, transferred to D/A converter, and output an analog voltage corresponding to display data. For CLK1 input timing, refer to Relationships between CLK1, start pulse(DIO1, DIO2) and blanking period(page 18).
VGMA1 to VGMA18	γ-corrected power supplies	Input the γ-corrected power supplies from external source. V_{DD2}>VGMA1>VGMA2>VGMA3>·····>VGMA17>VGMA18>V_{SS2} Keep gray scale power supply unchanged during the gray scale voltage output.
POL	Polarity inverting input	When POL = high, the reference voltages for odd number outputs are VGMA1 to VGMA9 and those for even number outputs are VGMA10 to VGMA18. When POL = low, the reference voltages for odd number outputs are VGMA10 to VGMA18 and those for even number outputs are VGMA1 to VGMA9.
SELT	Selection of output number	Pin for selecting 300/309 output mode. SELT = L: 309 outputs TEST = H: 300 outputs → Cannot use Y151 to Y159
TESTB	Test pin	TESTB = H: Normal operation TESTB = L: Test mode → OP AMP CUT-OFF This pin is internally pulled-up (Rpu = 30kΩ).

OPERATION DESCRIPTION

DISPLAY DATA TRANSFER

DIO1(or DIO2) = “H” is loaded into internal latch at the rising edge of CLK2, which starts the data transfer operation, and after the falling edge of DIO1(or DIO2), display data is valid at the rising edge of CLK2.
Once all the data of 300/309 channels is loaded into internal latch, it goes into standby state automatically, and any new data is not accepted even though CLK2 is provided until next DIO1(or DIO2) input.
When DIO1(or DIO2) is provided, new display data is valid at the next rising edge of CLK2 after the falling edge of DIO1(or DIO2).

EXTENSION OF OUTPUT

Output pin can be adjusted to an extended screen by cascade connection.

- SHL = “L”
  Connect DIO1 pin of previous stage to the DIO2 pin of next stage and all the input pins except DIO1 and DIO2 are connected together in each device.

- SHL = “H”
  Connect DIO2 pin of previous stage to the DIO1 pin of next stage and all the input pins except DIO1 and DIO2 are connected together in each device.

RELATIONSHIP BETWEEN INPUT DATA VALUE AND OUTPUT VOLTAGE

The LCD drive output voltages are determined by the input data and the eighteen γ-corrected power supplies (VGMA1 to VGMA18). Also, to be able to deal with dot line inversion when mounted on a single side, gradation voltages with different polarity can be output to the odd number output pins and even number output pins. Among 9-by-2 γ-corrected voltages, input gray scale voltages of the same polarity with respect to the common voltage, for the respective nine γ-corrected voltages of VGMA1 to VGMA9 and VGMA10 to VGMA18.
The γ-corrected power supplies, VGMA1 to VGMA9 and VGMA10 to VGMA18, are the same polarity inputs with the common electrode voltages.

- Detalis on display data

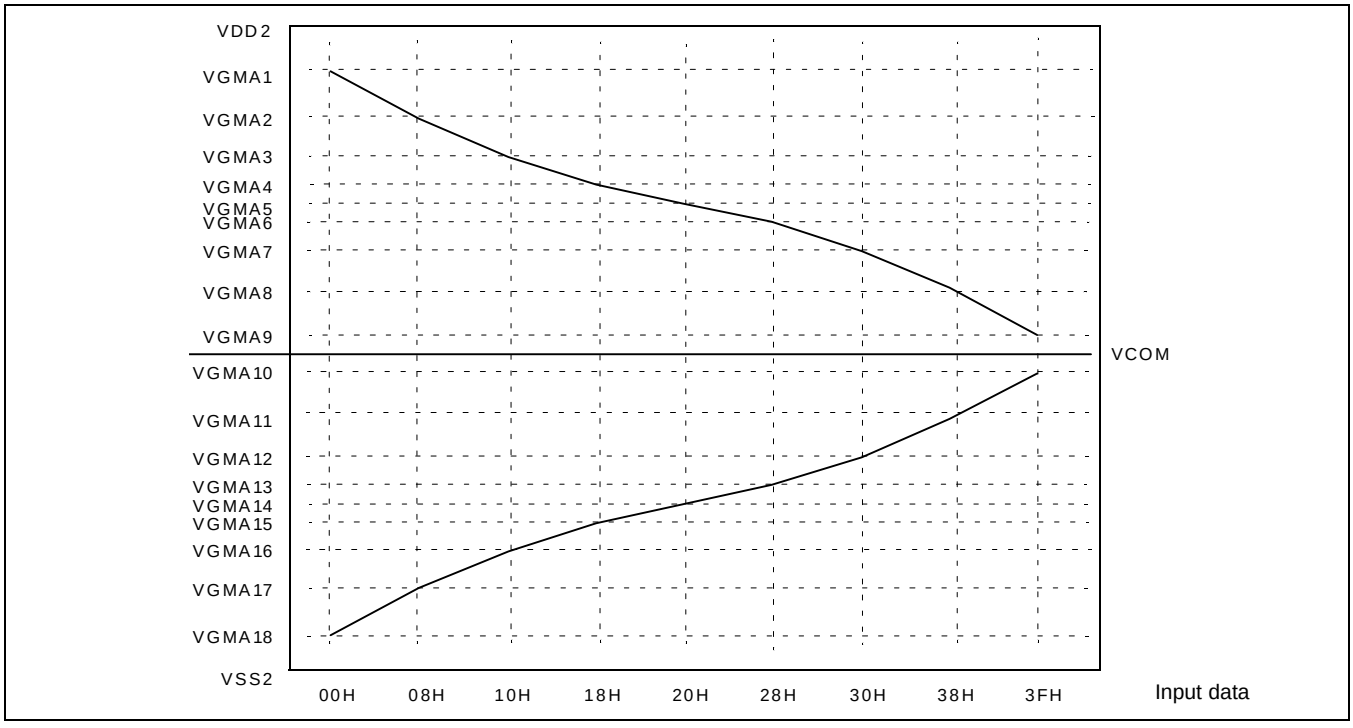
DX5	DX4	DX3	DX2	DX1	DX0
upper bits					lower bits

- Relationship between shift direction and output data
  SHL = "H" (right shift)

Output	Y1	Y2	Y3	.....	Y307	Y308	Y309
–	First			→	Last		
Data	D00 to D05	D10 to D15	D20 to D25	.....	D00 to D05	D10 to D15	D20 to D25

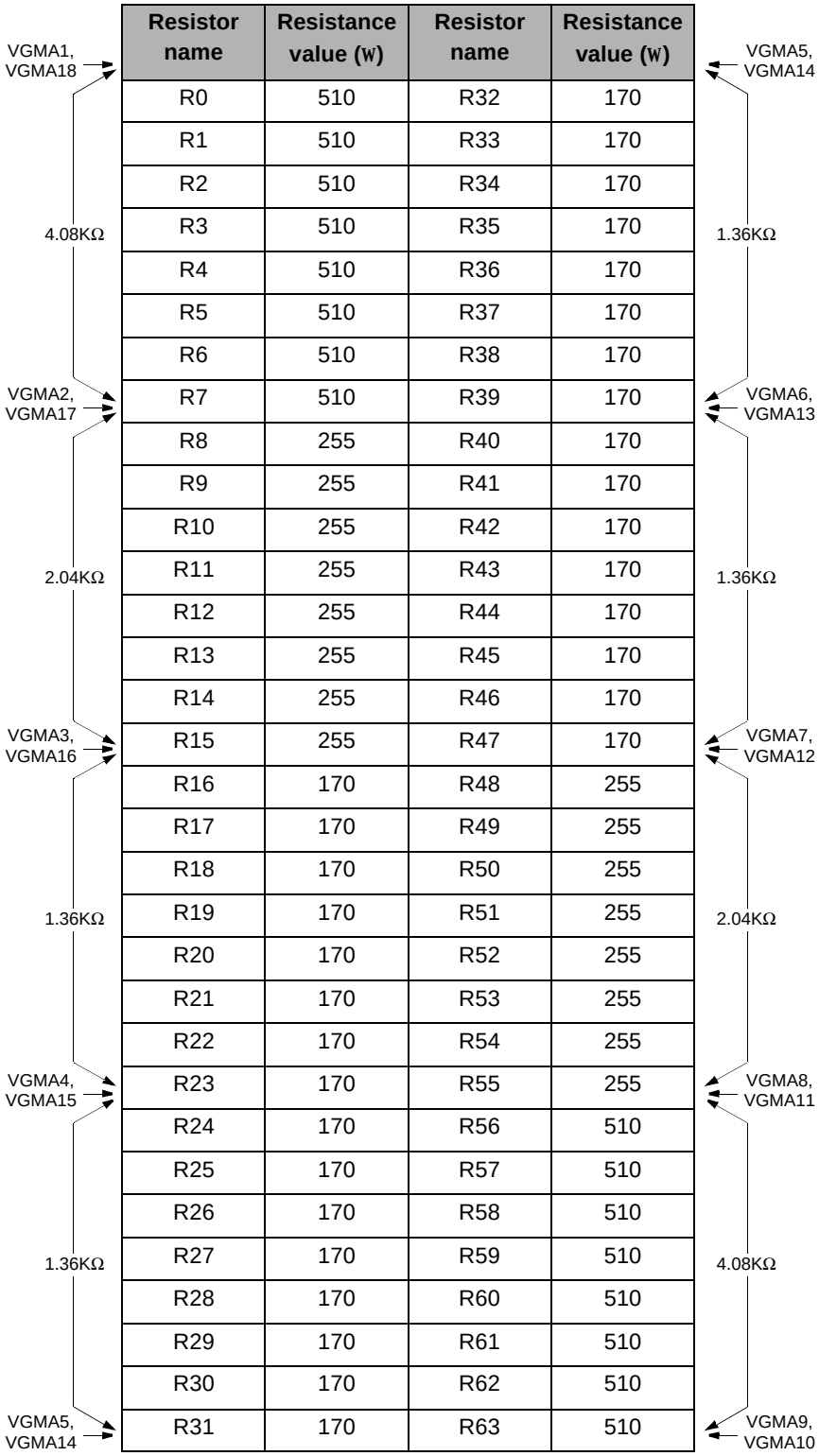
SHL= "L" (left shift)

Output	Y1	Y2	Y3	.....	Y307	Y308	Y309
–	Last			←	First		
Data	D00 to D05	D10 to D15	D20 to D25	.....	D00 to D05	D10 to D15	D20 to D25

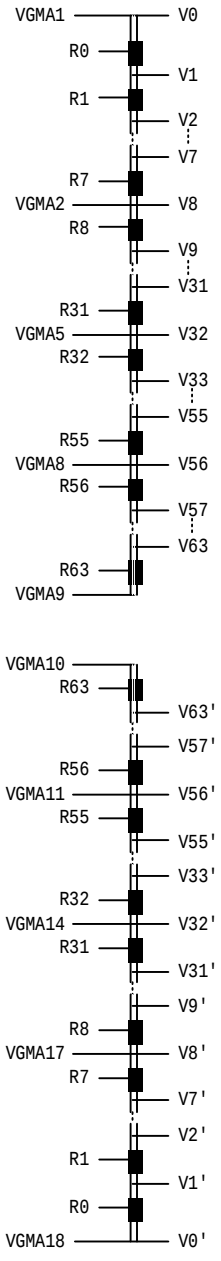


γ-Corrected Power Circuit and Relationship Input Data and Output Voltage

- Resistor strings (R0 to R63)



Resistor name	Resistance value (W)	Resistor name	Resistance value (W)
R0	510	R32	170
R1	510	R33	170
R2	510	R34	170
R3	510	R35	170
R4	510	R36	170
R5	510	R37	170
R6	510	R38	170
R7	510	R39	170
R8	255	R40	170
R9	255	R41	170
R10	255	R42	170
R11	255	R43	170
R12	255	R44	170
R13	255	R45	170
R14	255	R46	170
R15	255	R47	170
R16	170	R48	255
R17	170	R49	255
R18	170	R50	255
R19	170	R51	255
R20	170	R52	255
R21	170	R53	255
R22	170	R54	255
R23	170	R55	255
R24	170	R56	510
R25	170	R57	510
R26	170	R58	510
R27	170	R59	510
R28	170	R60	510
R29	170	R61	510
R30	170	R62	510
R31	170	R63	510



- **Relationship between input data and output voltage value(1)**

V_{DD2}>vgma1>vgma2>vgma3>vgma4>vgma5>vgma6>vgma7>vgma8>vgma9>V_{SS2}

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
00H	0	0	0	0	0	0	V0	VGMA1
01H	0	0	0	0	0	1	V1	VGMA1 + (VGMA2-VGMA1) × 1/8
02H	0	0	0	0	1	0	V2	VGMA1 + (VGMA2-VGMA1) × 2/8
03H	0	0	0	0	1	1	V3	VGMA1 + (VGMA2-VGMA1) × 3/8
04H	0	0	0	1	0	0	V4	VGMA1 + (VGMA2-VGMA1) × 4/8
05H	0	0	0	1	0	1	V5	VGMA1 + (VGMA2-VGMA1) × 5/8
06H	0	0	0	1	1	0	V6	VGMA1 + (VGMA2-VGMA1) × 6/8
07H	0	0	0	1	1	1	V7	VGMA1 + (VGMA2-VGMA1) × 7/8
08H	0	0	1	0	0	0	V8	VGMA2
09H	0	0	1	0	0	1	V9	VGMA2 + (VGMA3-VGMA2) × 1/8
0AH	0	0	1	0	1	0	V10	VGMA2 + (VGMA3-VGMA2) × 2/8
0BH	0	0	1	0	1	1	V11	VGMA2 + (VGMA3-VGMA2) × 3/8
0CH	0	0	1	1	0	0	V12	VGMA2 + (VGMA3-VGMA2) × 4/8
0DH	0	0	1	1	0	1	V13	VGMA2 + (VGMA3-VGMA2) × 5/8
0EH	0	0	1	1	1	0	V14	VGMA2 + (VGMA3-VGMA2) × 6/8
0FH	0	0	1	1	1	1	V15	VGMA2 + (VGMA3-VGMA2) × 7/8
10H	0	1	0	0	0	0	V16	VGMA3
11H	0	1	0	0	0	1	V17	VGMA3 + (VGMA4-VGMA3) × 1/8
12H	0	1	0	0	1	0	V18	VGMA3 + (VGMA4-VGMA3) × 2/8
13H	0	1	0	0	1	1	V19	VGMA3 + (VGMA4-VGMA3) × 3/8
14H	0	1	0	1	0	0	V20	VGMA3 + (VGMA4-VGMA3) × 4/8
15H	0	1	0	1	0	1	V21	VGMA3 + (VGMA4-VGMA3) × 5/8
16H	0	1	0	1	1	0	V22	VGMA3 + (VGMA4-VGMA3) × 6/8
17H	0	1	0	1	1	1	V23	VGMA3 + (VGMA4-VGMA3) × 7/8
18H	0	1	1	0	0	0	V24	VGMA4
19H	0	1	1	0	0	1	V25	VGMA4 + (VGMA5-VGMA4) × 1/8
1AH	0	1	1	0	1	0	V26	VGMA4 + (VGMA5-VGMA4) × 2/8
1BH	0	1	1	0	1	1	V27	VGMA4 + (VGMA5-VGMA4) × 3/8
1CH	0	1	1	1	0	0	V28	VGMA4 + (VGMA5-VGMA4) × 4/8
1DH	0	1	1	1	0	1	V29	VGMA4 + (VGMA5-VGMA4) × 5/8
1EH	0	1	1	1	1	0	V30	VGMA4 + (VGMA5-VGMA4) × 6/8
1FH	0	1	1	1	1	1	V31	VGMA4 + (VGMA5-VGMA4) × 7/8

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
20H	1	0	0	0	0	0	V32	VGMA5
21H	1	0	0	0	0	1	V33	VGMA5 + (VGMA6-VGMA5) × 1/8
22H	1	0	0	0	1	0	V34	VGMA5 + (VGMA6-VGMA5) × 2/8
23H	1	0	0	0	1	1	V35	VGMA5 + (VGMA6-VGMA5) × 3/8
24H	1	0	0	1	0	0	V36	VGMA5 + (VGMA6-VGMA5) × 4/8
25H	1	0	0	1	0	1	V37	VGMA5 + (VGMA6-VGMA5) × 5/8
26H	1	0	0	1	1	0	V38	VGMA5 + (VGMA6-VGMA5) × 6/8
27H	1	0	0	1	1	1	V39	VGMA5 + (VGMA6-VGMA5) × 7/8
28H	1	0	1	0	0	0	V40	VGMA6
29H	1	0	1	0	0	1	V41	VGMA6 + (VGMA7-VGMA6) × 1/8
2AH	1	0	1	0	1	0	V42	VGMA6 + (VGMA7-VGMA6) × 2/8
2BH	1	0	1	0	1	1	V43	VGMA6 + (VGMA7-VGMA6) × 3/8
2CH	1	0	1	1	0	0	V44	VGMA6 + (VGMA7-VGMA6) × 4/8
2DH	1	0	1	1	0	1	V45	VGMA6 + (VGMA7-VGMA6) × 5/8
2EH	1	0	1	1	1	0	V46	VGMA6 + (VGMA7-VGMA6) × 6/8
2FH	1	0	1	1	1	1	V47	VGMA6 + (VGMA7-VGMA6) × 7/8
30H	1	1	0	0	0	0	V48	VGMA7
31H	1	1	0	0	0	1	V49	VGMA7 + (VGMA8-VGMA7) × 1/8
32H	1	1	0	0	1	0	V50	VGMA7 + (VGMA8-VGMA7) × 2/8
33H	1	1	0	0	1	1	V51	VGMA7 + (VGMA8-VGMA7) × 3/8
34H	1	1	0	1	0	0	V52	VGMA7 + (VGMA8-VGMA7) × 4/8
35H	1	1	0	1	0	1	V53	VGMA7 + (VGMA8-VGMA7) × 5/8
36H	1	1	0	1	1	0	V54	VGMA7 + (VGMA8-VGMA7) × 6/8
37H	1	1	0	1	1	1	V55	VGMA7 + (VGMA8-VGMA7) × 7/8
38H	1	1	1	0	0	0	V56	VGMA8
39H	1	1	1	0	0	1	V57	VGMA8 + (VGMA8-VGMA7) × 1/8
3AH	1	1	1	0	1	0	V58	VGMA8 + (VGMA8-VGMA7) × 2/8
3BH	1	1	1	0	1	1	V59	VGMA8 + (VGMA8-VGMA7) × 3/8
3CH	1	1	1	1	0	0	V60	VGMA8 + (VGMA8-VGMA7) × 4/8
3DH	1	1	1	1	0	1	V61	VGMA8 + (VGMA8-VGMA7) × 5/8
3EH	1	1	1	1	1	0	V62	VGMA8 + (VGMA8-VGMA7) × 6/8
3FH	1	1	1	1	1	1	V63	VGMA8 + (VGMA8-VGMA7) × 7/8

- **Relationship between input data and output voltage value(2)**

V_{DD2}>vgma10>vgma11>vgma12>vgma13>vgma14>vgma15>vgma16>vgma17>vgma18>V_{SS2}

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
00H	0	0	0	0	0	0	V0′	VGMA18
01H	0	0	0	0	0	1	V1′	VGMA18 + (VGMA17-VGMA18) × 1/8
02H	0	0	0	0	1	0	V2′	VGMA18 + (VGMA17-VGMA18) × 2/8
03H	0	0	0	0	1	1	V3′	VGMA18 + (VGMA17-VGMA18) × 3/8
04H	0	0	0	1	0	0	V4′	VGMA18 + (VGMA17-VGMA18) × 4/8
05H	0	0	0	1	0	1	V5′	VGMA18 + (VGMA17-VGMA18) × 5/8
06H	0	0	0	1	1	0	V6′	VGMA18 + (VGMA17-VGMA18) × 6/8
07H	0	0	0	1	1	1	V7′	VGMA18 + (VGMA17-VGMA18) × 7/8
08H	0	0	1	0	0	0	V8′	VGMA17
09H	0	0	1	0	0	1	V9′	VGMA17 + (VGMA16-VGMA17) × 1/8
0AH	0	0	1	0	1	0	V10′	VGMA17 + (VGMA16-VGMA17) × 2/8
0BH	0	0	1	0	1	1	V11′	VGMA17 + (VGMA16-VGMA17) × 3/8
0CH	0	0	1	1	0	0	V12′	VGMA17 + (VGMA16-VGMA17) × 4/8
0DH	0	0	1	1	0	1	V13′	VGMA17 + (VGMA16-VGMA17) × 5/8
0EH	0	0	1	1	1	0	V14′	VGMA17 + (VGMA16-VGMA17) × 6/8
0FH	0	0	1	1	1	1	V15′	VGMA17 + (VGMA16-VGMA17) × 7/8
10H	0	1	0	0	0	0	V16′	VGMA16
11H	0	1	0	0	0	1	V17′	VGMA16 + (VGMA15-VGMA16) × 1/8
12H	0	1	0	0	1	0	V18′	VGMA16 + (VGMA15-VGMA16) × 2/8
13H	0	1	0	0	1	1	V19′	VGMA16 + (VGMA15-VGMA16) × 3/8
14H	0	1	0	1	0	0	V20′	VGMA16 + (VGMA15-VGMA16) × 4/8
15H	0	1	0	1	0	1	V21′	VGMA16 + (VGMA15-VGMA16) × 5/8
16H	0	1	0	1	1	0	V22′	VGMA16 + (VGMA15-VGMA16) × 6/8
17H	0	1	0	1	1	1	V23′	VGMA16 + (VGMA15-VGMA16) × 7/8
18H	0	1	1	0	0	0	V24′	VGMA15
19H	0	1	1	0	0	1	V25′	VGMA15 + (VGMA14-VGMA15) × 1/8
1AH	0	1	1	0	1	0	V26′	VGMA15 + (VGMA14-VGMA15) × 2/8
1BH	0	1	1	0	1	1	V27′	VGMA15 + (VGMA14-VGMA15) × 3/8
1CH	0	1	1	1	0	0	V28′	VGMA15 + (VGMA14-VGMA15) × 4/8
1DH	0	1	1	1	0	1	V29′	VGMA15 + (VGMA14-VGMA15) × 5/8
1EH	0	1	1	1	1	0	V30′	VGMA15 + (VGMA14-VGMA15) × 6/8
1FH	0	1	1	1	1	1	V31′	VGMA15 + (VGMA14-VGMA15) × 7/8

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
20H	1	0	0	0	0	0	V32′	VGMA14
21H	1	0	0	0	0	1	V33′	VGMA14 + (VGMA13-VGMA14) × 1/8
22H	1	0	0	0	1	0	V34′	VGMA14 + (VGMA13-VGMA14) × 2/8
23H	1	0	0	0	1	1	V35′	VGMA14 + (VGMA13-VGMA14) × 3/8
24H	1	0	0	1	0	0	V36′	VGMA14 + (VGMA13-VGMA14) × 4/8
25H	1	0	0	1	0	1	V37′	VGMA14 + (VGMA13-VGMA14) × 5/8
26H	1	0	0	1	1	0	V38′	VGMA14 + (VGMA13-VGMA14) × 6/8
27H	1	0	0	1	1	1	V39′	VGMA14 + (VGMA13-VGMA14) × 7/8
28H	1	0	1	0	0	0	V40′	VGMA13
29H	1	0	1	0	0	1	V41′	VGMA13 + (VGMA12-VGMA13) × 1/8
2AH	1	0	1	0	1	0	V42′	VGMA13 + (VGMA12-VGMA13) × 2/8
2BH	1	0	1	0	1	1	V43′	VGMA13 + (VGMA12-VGMA13) × 3/8
2CH	1	0	1	1	0	0	V44′	VGMA13 + (VGMA12-VGMA13) × 4/8
2DH	1	0	1	1	0	1	V45′	VGMA13 + (VGMA12-VGMA13) × 5/8
2EH	1	0	1	1	1	0	V46′	VGMA13 + (VGMA12-VGMA13) × 6/8
2FH	1	0	1	1	1	1	V47′	VGMA13 + (VGMA12-VGMA13) × 7/8
30H	1	1	0	0	0	0	V48′	VGMA12
31H	1	1	0	0	0	1	V49′	VGMA12 + (VGMA11-VGMA12) × 1/8
32H	1	1	0	0	1	0	V50′	VGMA12 + (VGMA11-VGMA12) × 2/8
33H	1	1	0	0	1	1	V51′	VGMA12 + (VGMA11-VGMA12) × 3/8
34H	1	1	0	1	0	0	V52′	VGMA12 + (VGMA11-VGMA12) × 4/8
35H	1	1	0	1	0	1	V53′	VGMA12 + (VGMA11-VGMA12) × 5/8
36H	1	1	0	1	1	0	V54′	VGMA12 + (VGMA11-VGMA12) × 6/8
37H	1	1	0	1	1	1	V55′	VGMA12 + (VGMA11-VGMA12) × 7/8
38H	1	1	1	0	0	0	V56′	VGMA11
39H	1	1	1	0	0	1	V57′	VGMA11 + (VGMA10-VGMA11) × 1/8
3AH	1	1	1	0	1	0	V58′	VGMA11 + (VGMA10-VGMA11) × 2/8
3BH	1	1	1	0	1	1	V59′	VGMA11 + (VGMA10-VGMA11) × 3/8
3CH	1	1	1	1	0	0	V60′	VGMA11 + (VGMA10-VGMA11) × 4/8
3DH	1	1	1	1	0	1	V61′	VGMA11 + (VGMA10-VGMA11) × 5/8
3EH	1	1	1	1	1	0	V62′	VGMA11 + (VGMA10-VGMA11) × 6/8
3FH	1	1	1	1	1	1	V63′	VGMA11 + (VGMA10-VGMA11) × 7/8

MAXIMUM ABSOLUTE LIMIT

(V_{SS1} = V_{SS2} = 0V)

Characteristic	Symbol	Value	Unit
Digital supply voltage	V_{DD1}	–0.3 to 6.5	V
Analog supply voltage	V_{DD2}	–0.3 to 15.0	V
Input voltage	VGMA1 to 18	–0.3 to V_{DD2}+0.3	V
	Others	–0.3 to V_{DD1}+0.3	V
Ouput voltage	DIO1,DIO2	–0.3 to V_{DD1}+0.3	V
	Y1 to Y309	–0.3 to V_{DD2}+0.3	V
Operating power dissipation	Pd	150	mW
Operating temperature	Topr	–20 to 75	°C
Storage temperature	Tstg	–55 to 125	°C

— Turn on power order : V_{DD1} → control signal input → V_{DD2} → VGMA1 ~ VGMA18
Turn off power order : VGMA1 ~ VGMA18 → V_{DD2} → control signal input → V_{DD1}

— If LSIs are used beyond the above maximum absolute limits, they may be permanently destroyed.

RECOMMENDED OPERATING RANGE

(Ta = –20 to 75°C, V_{SS1} = V_{SS2} = 0V)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Digital supply voltage	V_{DD1}	2.7	3.0	3.6	V
Analog supply voltage	V_{DD2}	6.4	9.0	13.0	V
γ-corrected voltage	VGMA1 to VGMA9	0.5V_{DD2}+0.2	-	V_{DD2}-0.2	V
	VGMA10 to VGMA18	0.2	-	0.5V_{DD2}-0.2	V
Driver part output voltage	Vyo	0.2	-	V_{DD2}-0.2	V
Maximum clock frequency	f_{max}	–	-	55	MHz
Output load capacitance	C_L	–	-	150	pF

ELECTRICAL CHARACTERISTICS

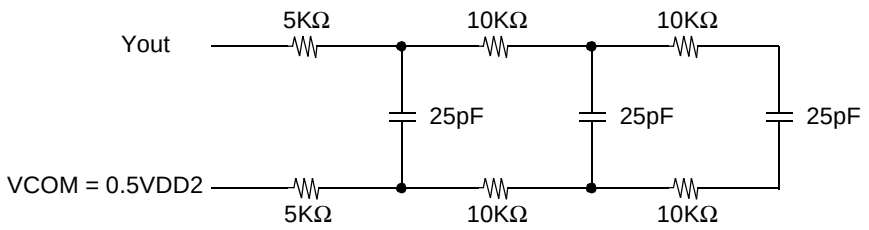
DC Characteristics (Ta = -20 to +75°C, V_{DD1} = 2.7 to 3.6V, V_{DD2} = 6.4 to 13.0V, V_{SS1} = V_{SS2} = 0V)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VIH	SHL, SELT, CLK2, D00 to D25, CLK1, POL, DIO1 (DIO2)	0.75V_{DD1}	–	V_{DD1}	V
Low level input voltage	VIL		0	–	0.25VDD1	V
Input leakage current	IL	D00 to D25, SHL, CLK2, CLK1, POL, SELT	–1	–	1	µA
High level output voltage	VOH	DIO1(DIO2), IO = -1.0mA	V_{DD1}-0.5	–	-	V
Low level output voltage	VOL	DIO1(DIO2), IO = +1.0mA	–	–	0.5	V
Resistance between γ-corrected voltage pins	R0 to R63	Refer to γ-corrected power supply circuit	Rn × 0.77	refer to 7 page	Rn × 1.23	Ω
Driver output current	IVOH	V_{DD2} = 9.0V, Vx = 2.5V, Vyo = 8.5V	–	–1.0	–0.5	mA
	IVOL	V_{DD2} = 9.0V, Vx = 6.5V, Vyo = 0.5V	0.5	1.0	-	mA
Output voltage deviation	DVO	Input data: 00H to 3FH	–	± 8	± 15	mV
Output voltage range	VYO	Input data: 00H to 3FH	V_{SS2}+0.2	-	V_{DD2}-0.2	V
Logic part dynamic current consumption	IDD1	Note1, V_{DD1} = 3.0V	–	2.0	3.5	mA
Driver part dynamic current consumption	IDD2	Note1, Note2, Note3 V_{DD1} = 3.0V, V_{DD2} = 9.0V, VGMA1 = 8.5V, VGMA9 = 5.0V, VGMA10 = 4.0V, VGMA18 = 0.5V	–	5.0	7.0	mA

Vyo is the output voltage of analog output pins Y1 to Y309.
Vx is the voltage applied to analog output pins Y1 to Y309.

NOTES:

1. CLK1 period is defined to be 20µs at f_{CLK2} = 33MHz, data pattern = 1010 · · · (checkerboard pattern), Ta = 25°C
2. The current consumption per driver when XGA signle-sided mounting(10 units) are connected in cascade
3. Yout load condition



AC Characteristics

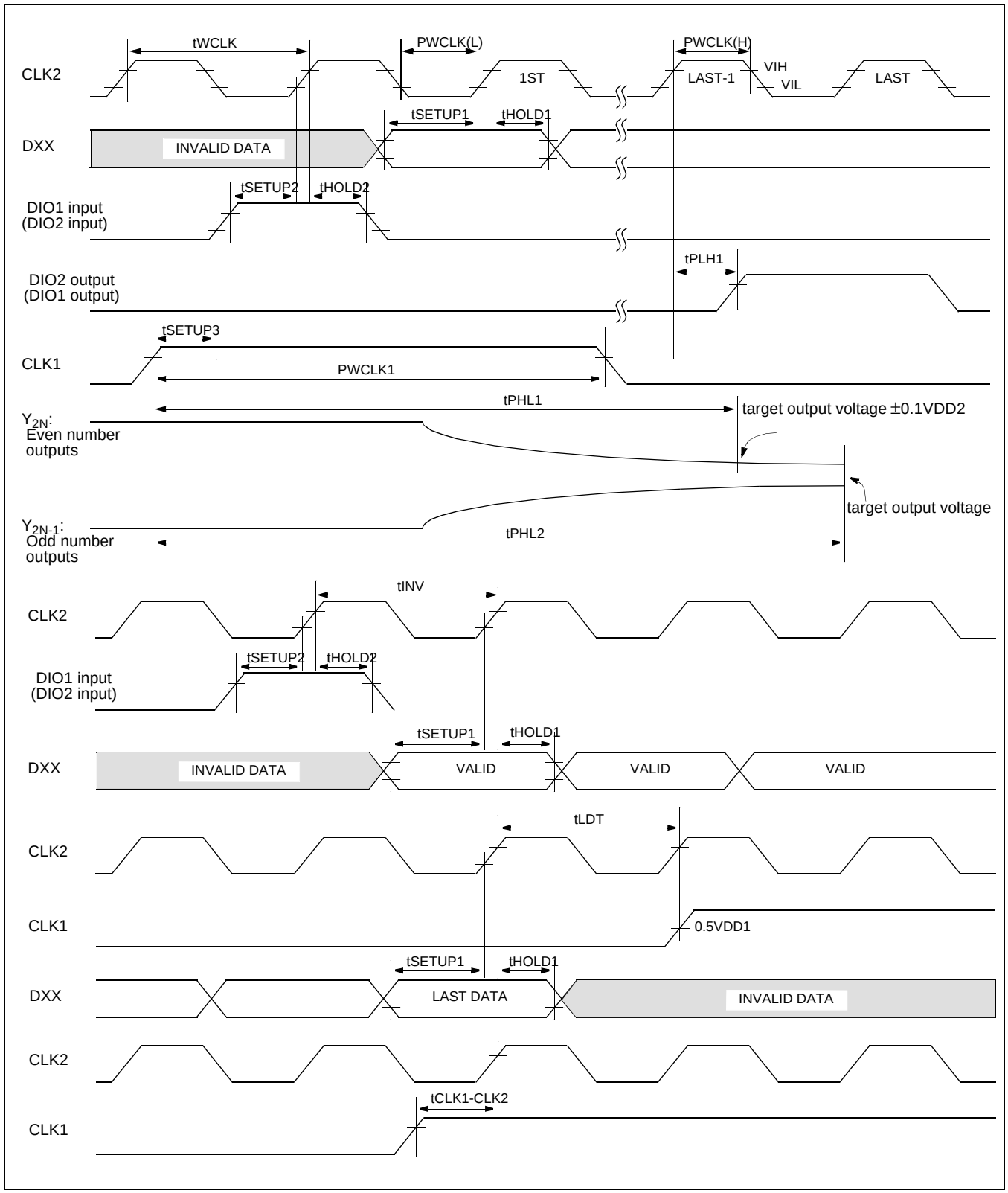
(Ta = -20 to +75°C, V_{DD1} = 2.7 to 3.6V, V_{DD2} = 6.4 to 13.0 V, V_{SS1} = V_{SS2} = 0V)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse width	PWCLK	–	18	–	–	ns
Clock pulse low period	PWCLK(L)	–	4	–	–	
Clock pulse high period	PWCLK(H)	–	4	–	–	
Data setup time	tSETUP1	–	4	–	–	
Data hold time	tHOLD1	–	0	–	–	
Start pulse setup time	tSETUP2	–	4	–	–	
Start pulse hold time	tHOLD2	–	0	–	–	
Start pulse delay time	tPLH1	CL = 20pF	-	–	12	
CLK1-DIO(input) setup time	tSETUP3	–	1	–	–	CLK2 period
CLK1 high pulse width	PWCLK1	–	3	–	–	
Driver output delay time1	tPHL1	refer to Note3 (15 page), Note4	–	–	5	µs
Driver output delay time2	tPHL2	refer to Note3 (15 page), Note5	–	–	10	
Data invalid period	tINV	Note6	1			CLK2 period
Last data timing	tLDT	–	1	–	–	
CLK1 - CLK2 time	tCLK1-CLK2	CLK1 ↑ or ↓ → CLK2 ↑	6	–	–	ns
POL - CLK1 time	tPOL-CLK1	POL ↑ or ↓ → CLK2 ↑	–9	–	–	
CLK1 - POL time	tCLK1-POL	CLK1 ↓ → POL ↑ or ↓	12	–	–	

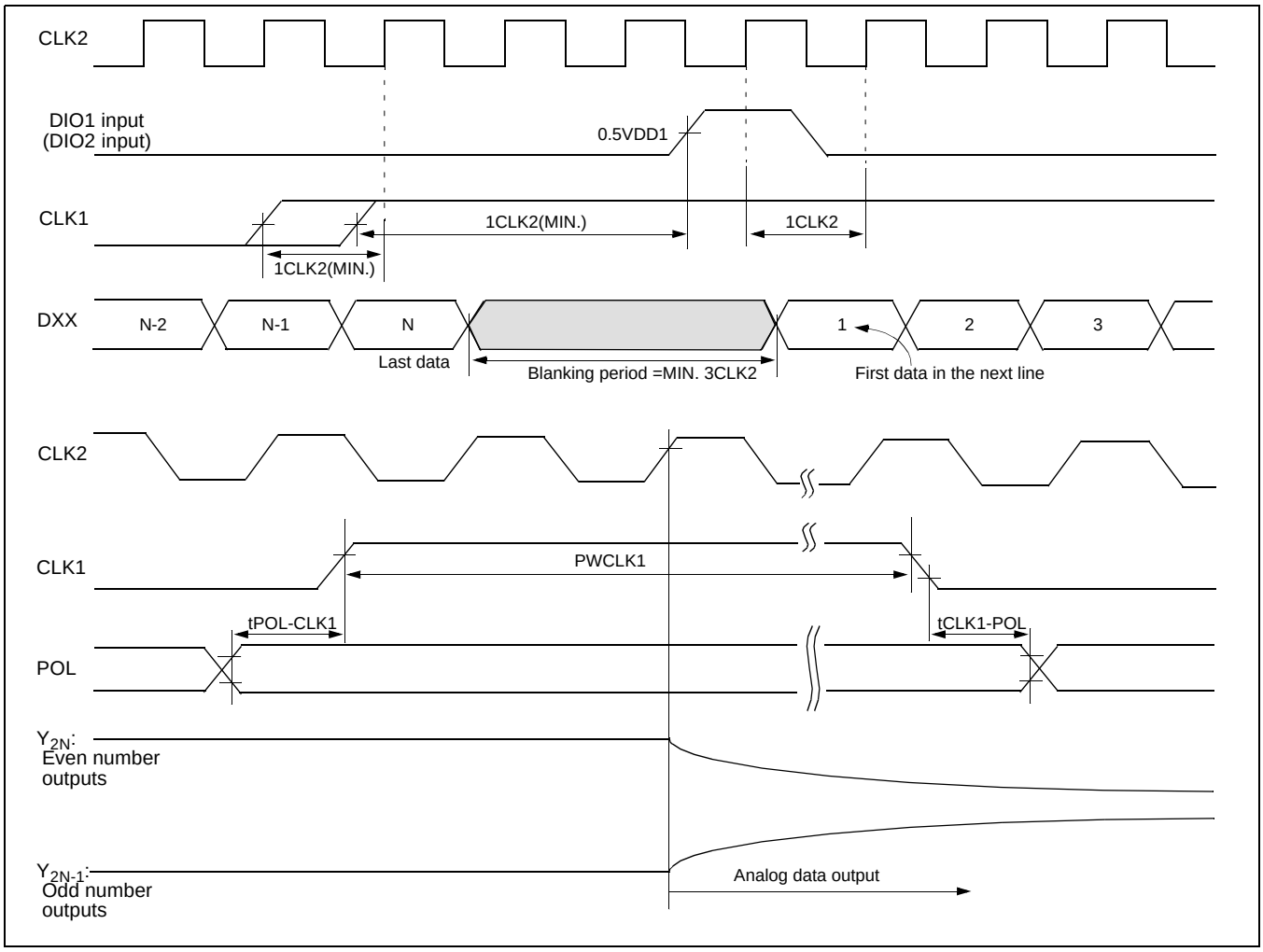
NOTES:

4. The value is specified when the drive output voltage value reaches the target output voltage level of 90%
5. The value is specified when the drive output voltage value reaches the target output voltage level of 6-bit accuracy
6. Set the rising edge of the first CLK2 after the rising edge of DIO1(or DIO2)

AC Characteristics waveform (VIH = 0.75V_{DD1}, VIL = 0.25V_{DD1})



· Relationships between CLK1, start pulse(DIO1,DIO2) and blanking period



· Relationships between CLK1, POL and outputs