## INTRODUCTION

The KS0655 is a TFT LCD gate driver.
This LSI can drive either 128 output pins or 120 output pins. It is highly recommended that you fix the driving source voltage (VOFF) for the gate line-off to the lowest power (V_{SS}) of the device.
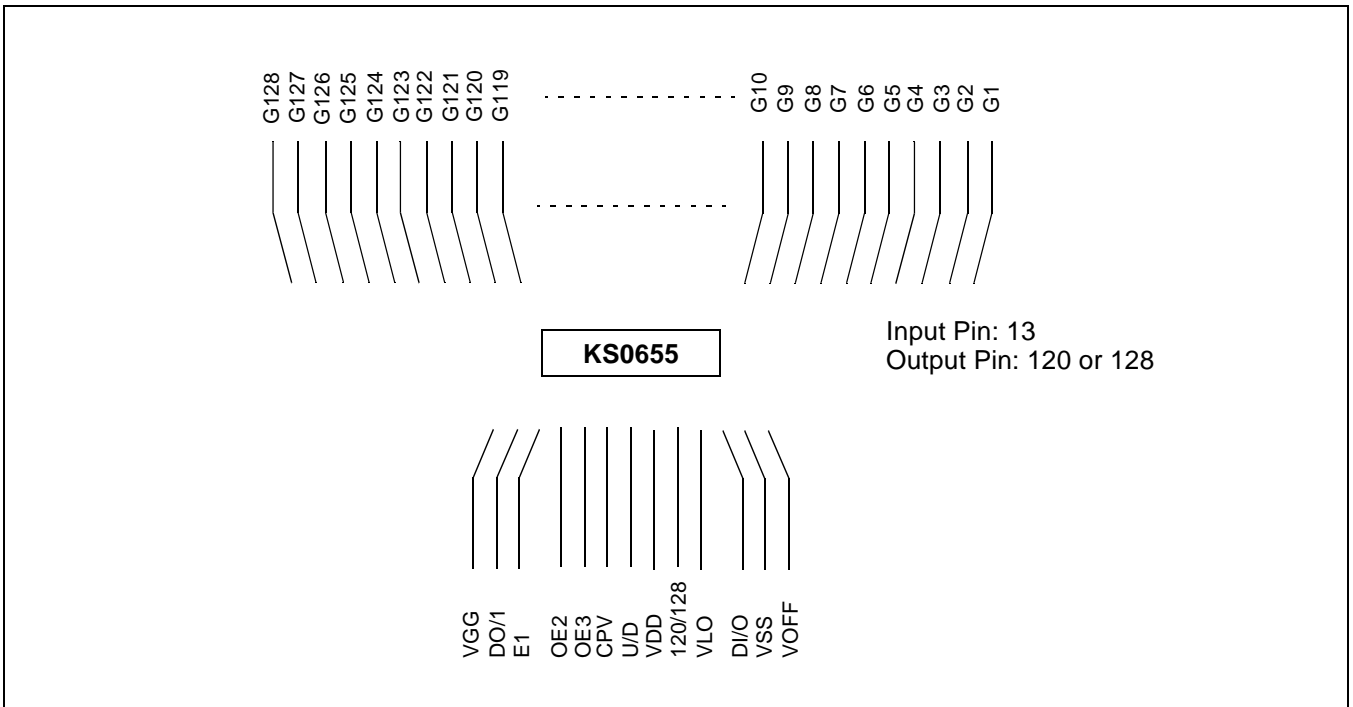
FEATURES

❏ Gate driver for TFT LCD

❏ TFT LCD drive output pin: 120/$\overline{128}$

❏ High voltage drive: VOFF + 40V (MAX.), if V_{SS} = VOFF = 0V

❏ Data transfer method: bi-directional shift register

❏ Source voltage (V_{DD}-VLO): 3.0 to 5.5 V

❏ Tape Carrier Package (TCP)

BLOCK DIAGRAM

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TCP PIN CONFIGURATION

Input Pin: 13
Output Pin: 120 or 128

KS0655
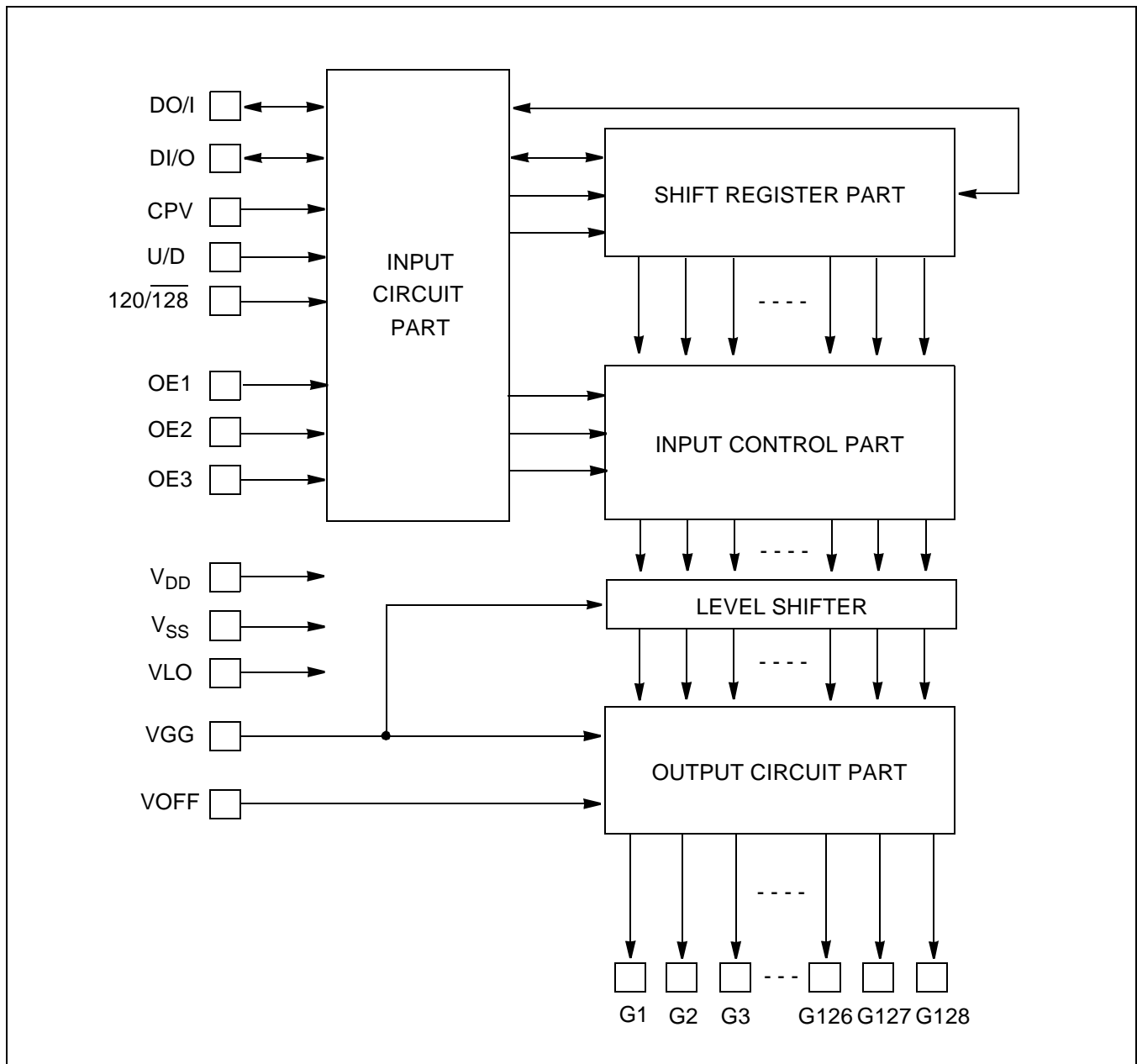
NOTE: This figure does not specify the dimensions of the TCP package.

PIN DESCRIPTION

Pin Symbol	Pin Name	Description
V_{DD}	Power supply	Voltage source for internal logic operation
V_{SS}	Power supply	Voltage source for internal logic operation and LCD panel control
VGG	Power supply	Voltage source for LCD panel control(plus)
VLO	Power supply	Source voltage of logic input low level
VOFF	Analog input (TFT gate off level)	When the data of the shift register is "L", output drive voltage is VOFF. When OE1 to 3 is "H", output drive voltage is VOFF apart from the data of the shift register. Supply voltage level is same to the lowest power level of device (V_{SS}).
G1 to G128	Driver output	Output drive voltage is VGG or VOFF for driving TFT LCD panel, depending on the data of shift register or the state of OE1 to 3. The status of each output pin changes in synchronization with the rising edge of shift clock CPV. Output pins G61 through G68 are invalid in 120 output mode.
DI/O DO/I	Vertical shift data input/output	Depending on the state of U/D, the functions of these two pins are determined as follows: <table><tr><td>U/D</td><td>DI/O</td><td>DO/I</td></tr><tr><td>"H" (V_{DD}) "L" (V_{SS} to VLO)</td><td>Input Output</td><td>Output Input</td></tr></table> **Input** : Input data which is transferred to these pins is stored in the first shift register at the rising edge of CPV. **Output** : Output data which is changing at the falling edge of CPV is transferred to the input pin of the next IC, which is cascaded.
U/D	Select pin of the shift data direction	Data in the shift register is synchronized with the rising edge of CPV and is transferred to the next register as follows: <table><tr><td>U/D</td><td>Shift direction</td></tr><tr><td>"H" (V_{DD}) "L" (V_{SS} to VLO)</td><td>G1 → G2 → G3 → G4 → G5..... → G128 G128 → G127 → G126 → G125 →..... → G1</td></tr></table> This pin is recommended to fix the DC level.
OE1 to 3	Output enable input	These pins control the state of output drive pins (G1 to G128).This pin fixes the driver output to the "L" level when it is high. However, the shift register is not cleared. OE1 to 3 = "L": Output level is VGG or VOFF corresponding to the data. OE1 to 3 = "H": Output level is VOFF.
120/$\overline{128}$	Selection of number of outputs	Selects number of outputs. 120/$\overline{128}$ = "H": 120 output mode 120/$\overline{128}$ = "L": 128 output mode
CPV	Shift clock input	Vertical shift clock input for the internal shift register. The contents of internal shift register is shifted at the rising edge of CPV.

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OPERATION DESCRIPTION

OPERATION METHOD

The input shift data (DI) of DI/O (When U/D is "H") or DO/I (When U/D is "L") is synchronized with the rising edge of CPV and stored in the first shift register.

While stored data is transferred to the next register at the next rising edge of CPV, new data of DI (Input shift data) is stored simultaneously.

The output pin (G1 to G128) supplies VGG voltage or VOFF voltage to the TFT LCD panel depending on the data of the shift register.

The output shift data (DO) of DO/I (When U/D is "H") or DI/O (When U/D is "L") is synchronized with the falling edge of CPV, and DO of the last register (G1 or G128) is transferred to the next IC.

The output voltage level of DO is V_{DD} with "H" data, V_{SS} with "L" data.

The mutual relationship of U/D and shift data I/O pin is as follows:

$\overline{120/128}$	U/D pin	Shift data I/O		Data transfer direction
		Input	Output	
128 output	"H"	DI/O	DO/I	G1 → G2 → G3 → G4 → G5 →..... → G128
	"L"	DO/I	DI/O	G128 → G127 → G126 → G125 →..... → G1
120 output	"H"	DI/O	DO/I	G1 → G2 ..... G59 → G60 → G69 → G70 ..... G127 → G128
	"L"	DO/I	DI/O	G128 → G127 ..... G70 → G69 → G60 → G59 ..... G2 → G1

OUTPUT PIN (G1 TO G128)

If the data of the shift register to an output drive pin is 'H", VGG voltage is output. Otherwise, VOFF voltage is output.
But, when OE1 to 3 to an output drive pin is 'H", VOFF voltage is output irrespective of the data of the shift register.

Condition		Mode	Control pin to LCD panel	
Pin	State	120/128	Output pin by OE signal	Output
OE1	"H"	120 output mode	G1,G4,G7,...., G55,G58,G69,G72,...., G123,G126	VOFF
OE2			G2,G5,G8,...., G56,G59,G70,G73,...., G124,G127	
OE3			G3,G6,G9,...., G57,G60,G71,G74,...., G125,G128	
OE1	"L"		G1,G4,G7,...., G55,G58,G69,G72,...., G123,G126	Normal output (VGG/VOFF)
OE2			G2,G5,G8,...., G56,G59,G70,G73,...., G124,G127	
OE3			G3,G6,G9,...., G57,G60,G71,G74,...., G125,G128	
OE1	"H"	128 output mode	G1,G4,G7,..........................., G121,G124,G127	VOFF
OE2			G2,G5,G8,..........................., G122,G125,G128	
OE3			G3,G6,G9,..........................., G123,G126	
OE1	"L"		G1,G4,G7,..........................., G121,G124,G127	Normal output (VGG/VOFF)
OE2			G2,G5,G8,..........................., G122,G125,G128	
OE3			G3,G6,G9,..........................., G123,G126	

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VOLTAGE BIAS

It is recommended that you fix VOFF which is the "L" level of the LCD output drive voltage, to V_{SS} which is the lowest power of device.

EX1) Negative output voltage mode
Logic input: Input switching level is from 0 V to V_{DD} (3.3V)
Power voltage:
VGG = 33V
V_{DD} = 3.3V
VLO = 0V
VOFF = -7V
V_{SS} = -7V

LCD output drive voltage:
"H" level = VGG (33V)
"L" level = VOFF (-7V)

EX2) Positive output voltage mode
Logic input: Input switching level is from 0V to V_{DD} (3.3 V)
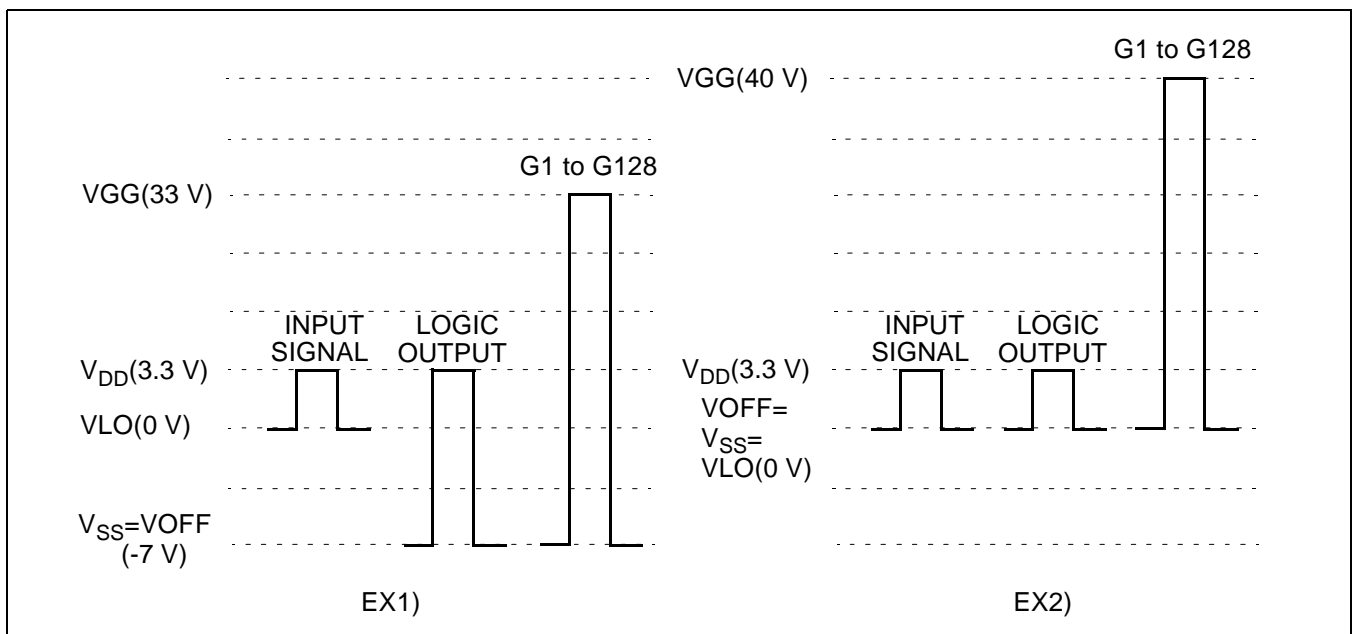Power voltage:
VGG = 40V
V_{DD} = 3.3V
VOFF = V_{SS} = VLO = 0V

LCD output drive voltage:
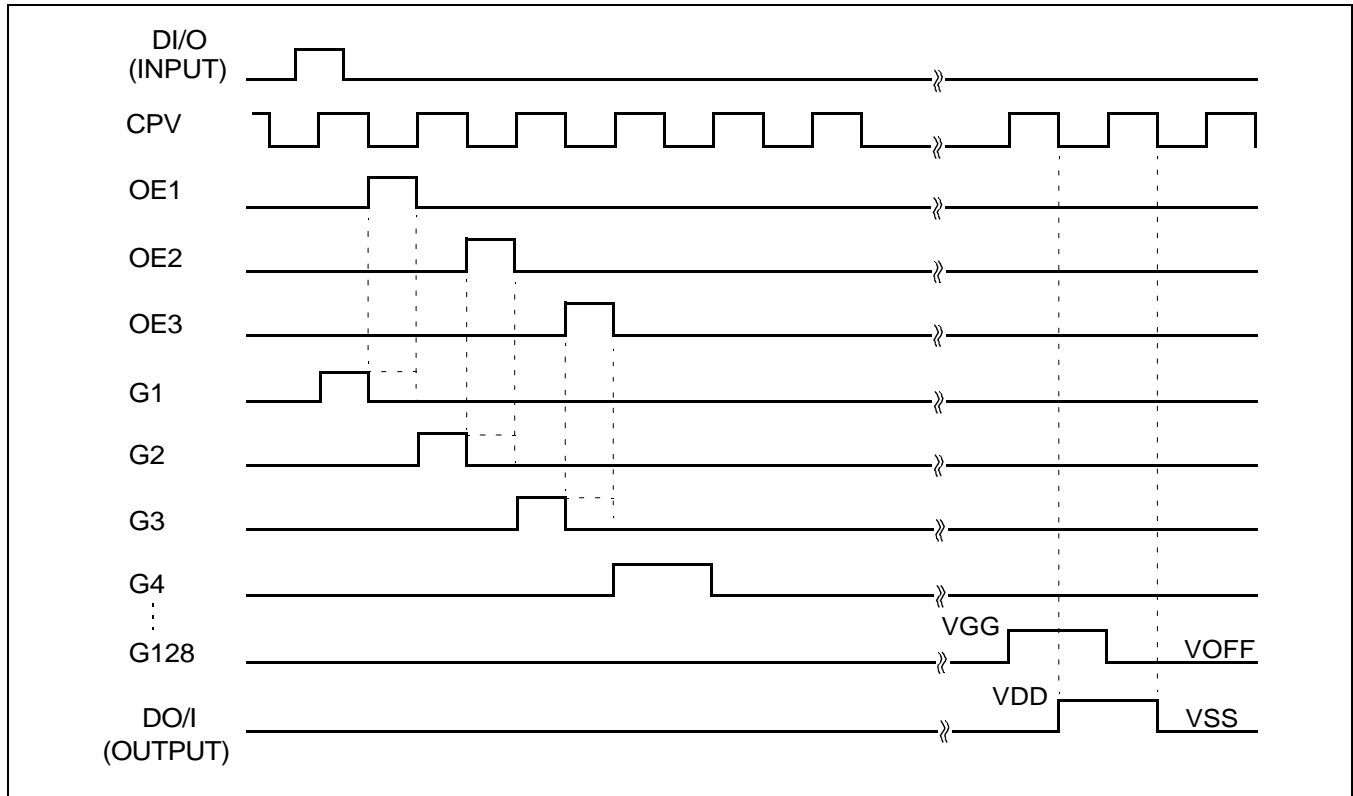"H" level = VGG (40V)
"L" level = VOFF (0V)

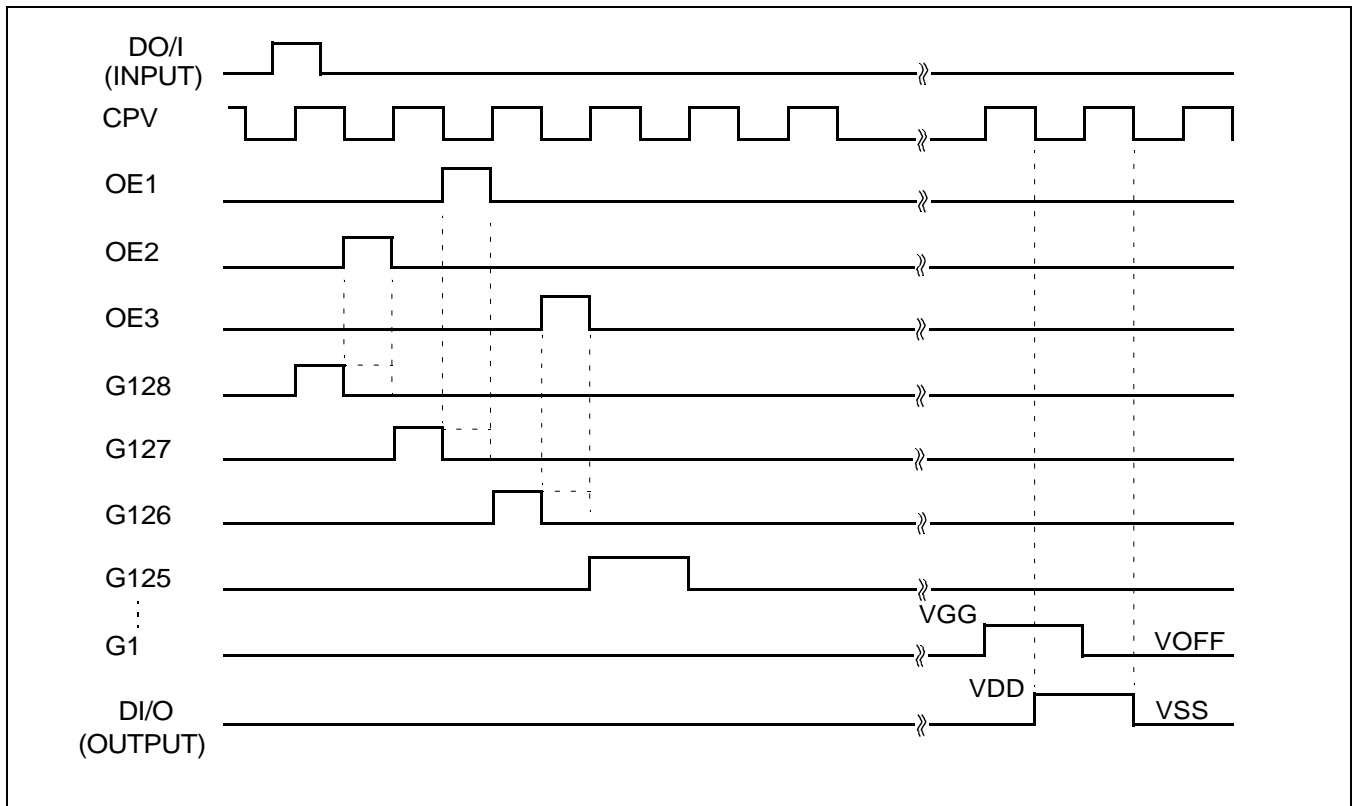— Input signal (DI/O, DO/I, CPV, OE1 to 3) swings from VIL to VIH.

RECOMMENDED TIMING

128 OUTPUT MODE (120/$\overline{128}$ = "L")
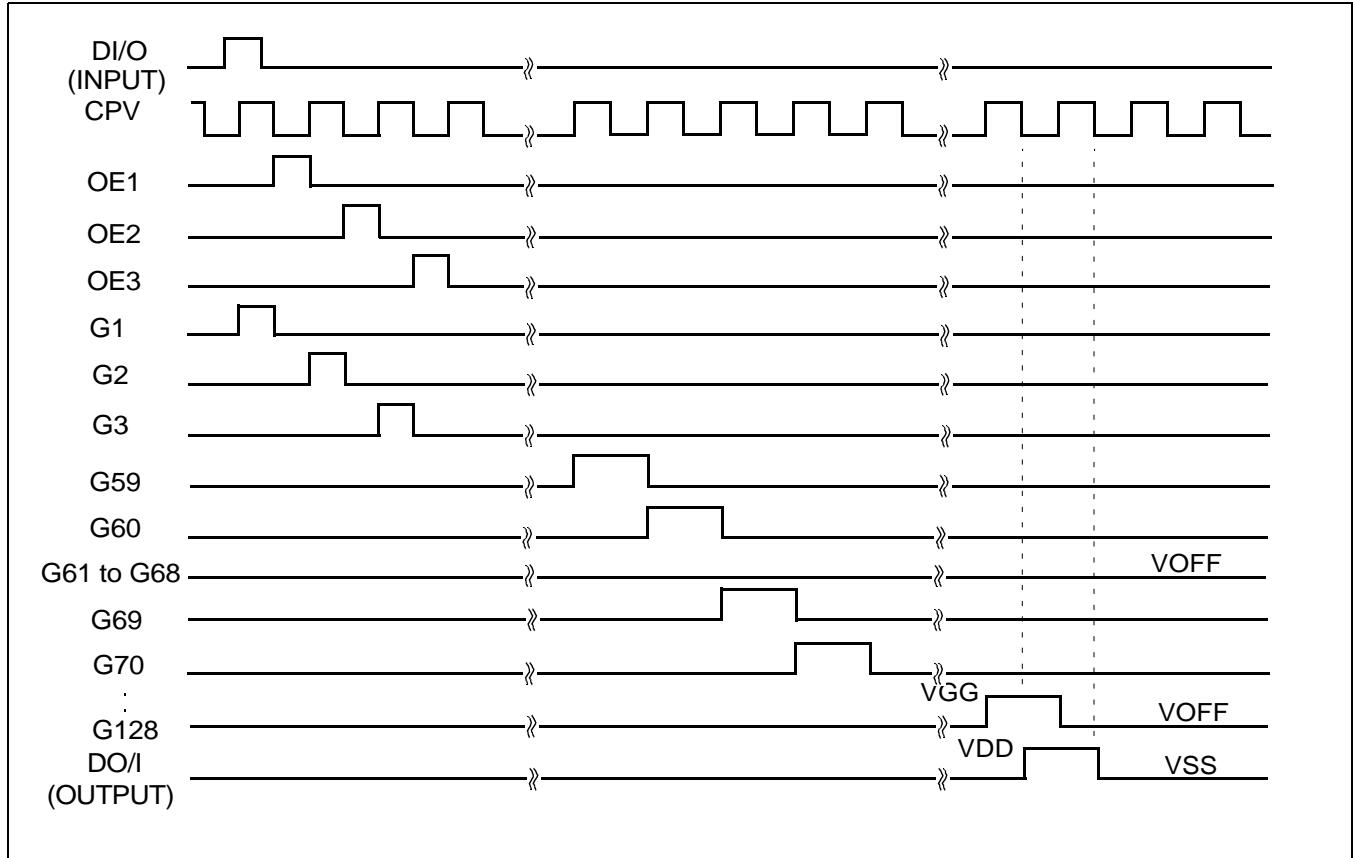
- UP MODE (When U/D = "H")

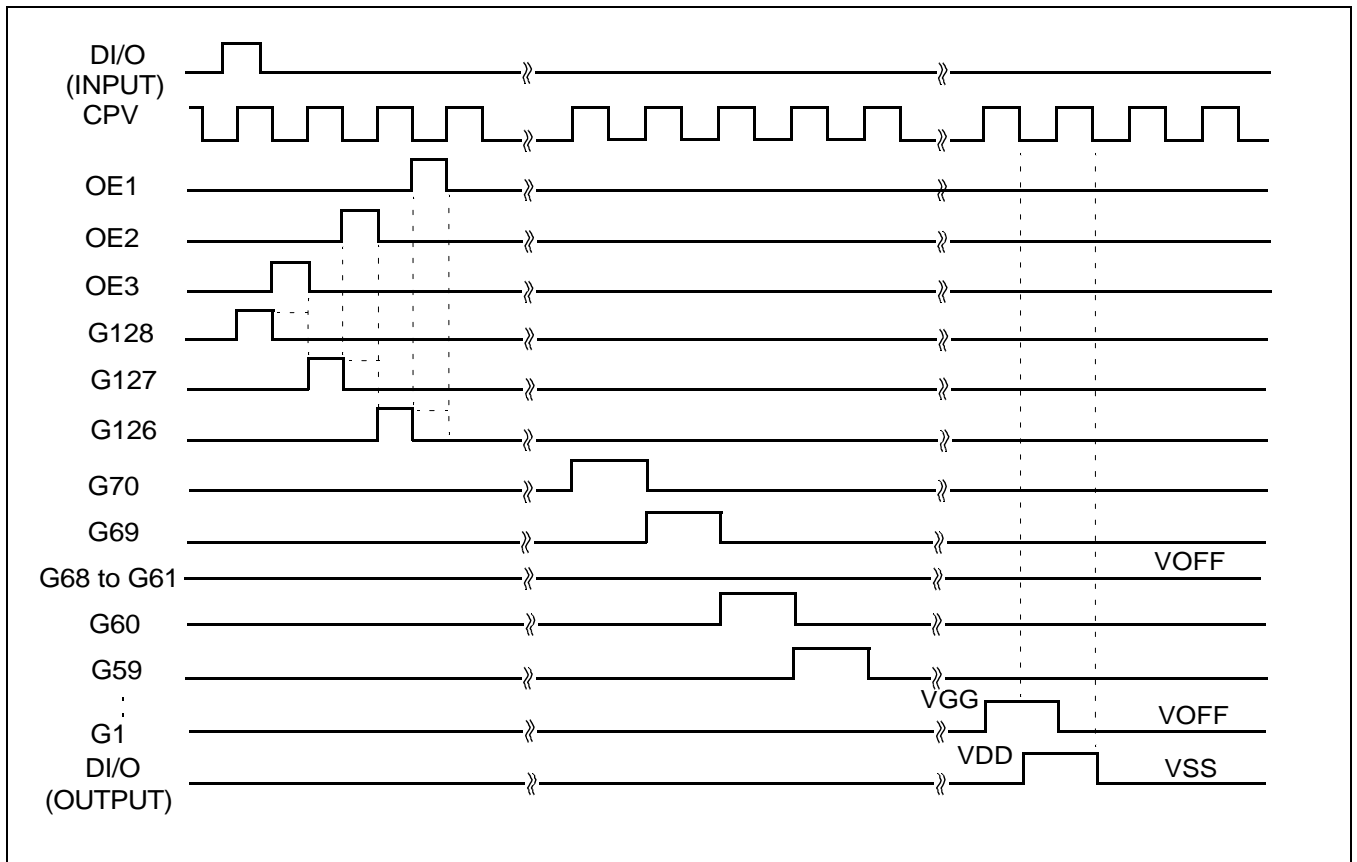• DOWN MODE (When U/D = "L")

120 OUTPUT MODE (120/$\overline{128}$ = "H")

- UP MODE (When U/D = "H")

- DOWN MODE (When U/D = "L")

MAXIMUM ABSOLUTE LIMIT

(V_{SS} = VOFF = 0V)

Characteristic	Symbol	Value	Unit	Application pin
Power supply voltage (1)	V_{GG}	−0.3 to 45.0	V	−
Power supply voltage (2)	V_{DD}	−0.3 to 22.0	V	−
Power supply voltage (3)	V_{LO}	−0.3 to V_{DD}+0.3	V	−
Input voltage	V_{IN}	−0.3 to V_{DD}+0.3	V	−
Operation temperature	T_{OPR}	−20 to 75	°C	−
Storage temperature	T_{STG}	−55 to 150	°C	−

*Power ON/OFF sequence
   Turn on power order: VLO → V_{DD} → V_{SS}, VOFF → control signal input → VGG
   Turn off power order: VGG → control signal input → V_{SS}, VOFF → V_{DD} → VLO
*If LSIs are used beyond the above maximum absolute limits, they may be permanently destroyed.
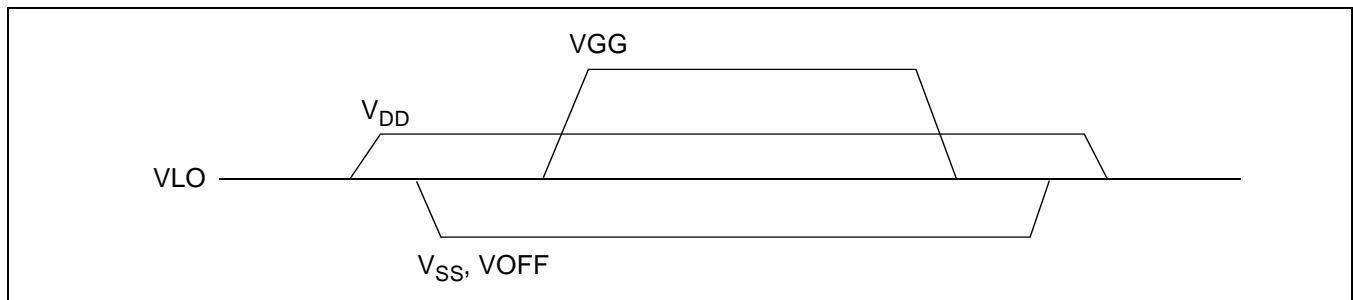
RECOMMENDED OPERATING RANGE

(V_{SS} = VOFF = 0V)

Characteristic	Symbol	Value	Unit	Remark
Power supply voltage (1)	VGG	22.0 to 40.0	V	−
Power supply voltage (2)	V_{DD}	3.0 to 20.5	V	−
Power supply voltage (3)	VLO	V_{DD}-5.5 to V_{DD}-3.0	V	VLO ≥ V_{SS}
Operation frequency	fCPV	DC to 100	kHz	−
Output load	CL	500 (MAX)	pF/PIN	−

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DC CHARACTERISTICS

(Ta = −20 to +75°C, VGG-V_{SS} = 22 to 40V, V_{DD}-V_{SS} = 3.0 to 20.5V, VOFF-V_{SS} = 0V, V_{DD}-VLO = 3.0 to 5.5V)

Characteristic	Symbol	Condition	Value		Unit	Application pin
			Min.	Max.		
Low input voltage	VIL	*1	V_{SS}	VLO+0.1VX	V	*2
High input voltage	VIH		VLO+0.9VX	V_{DD}	V	
Low output voltage	VOL	IOL = 40 µA	V_{SS}	V_{SS}+0.4	V	DI/O, DO/I
High output voltage	VOH	IOH = -40 µA	V_{DD}-0.4	V_{DD}	V	*3
Low output resistance	ROL	VOUT = 0.5 V VGG = 40 V V_{SS} = VOFF = 0 V	−	500	Ω	G1 to G128
High output resistance	ROH	VOUT = VGG-0.5 V VGG = 40 V V_{SS} = VOFF = 0 V	−	500	Ω	G1 to G128
Input leakage current	ILK	−	-5	5	µA	*2
Power supply current (1)	IGG	No output load	-	400	µA	VGG
Power supply current (2)	IDD	V_{DD}-V_{SS}=3.3 V	-	400	µA	V_{DD} *2, *4
		V_{DD}-V_{SS}=19 V	-	1000		

NOTES:

1. VX = V_{DD} - VLO
2. DI/O, DO/I, CPV, OE1 to 3, U/D, and 120/$\overline{128}$
3. When these pins are used as an output pin
4. Input swing voltage is V_{DD} to V_{DD}-3.3 V

AC CHARACTERISTICS

(Ta = −20 to +75°C, VGG-V_{SS} = 22 to 40V, V_{DD}-V_{SS} = 3.0 to 20.5V, VOFF-V_{SS} = 0V, V_{DD}-VLO = 3.0 to 5.5V)

Characteristic	Symbol	Condition	Value		Unit
			Min.	Max.	
Operation frequency	tCPV	−	10	−	µs
Clock pulse width	tCPVH, tCPVL	duty = 50%	4	−	
Output enable width	twOE	−	1	−	
Data setup time	tsDI	−	700	−	ns
Data hold time	thDI	−	700	−	
Output delay time (1)	tpdDO	CL = 30 pF	-	800	
Output delay time (2)	tpdG	CL = 300 pF	-	800	
Output delay time (3)	tpdOE	CL =3 00 pF	-	800	

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AC TIMING DIAGRAM