INTRODUCTION

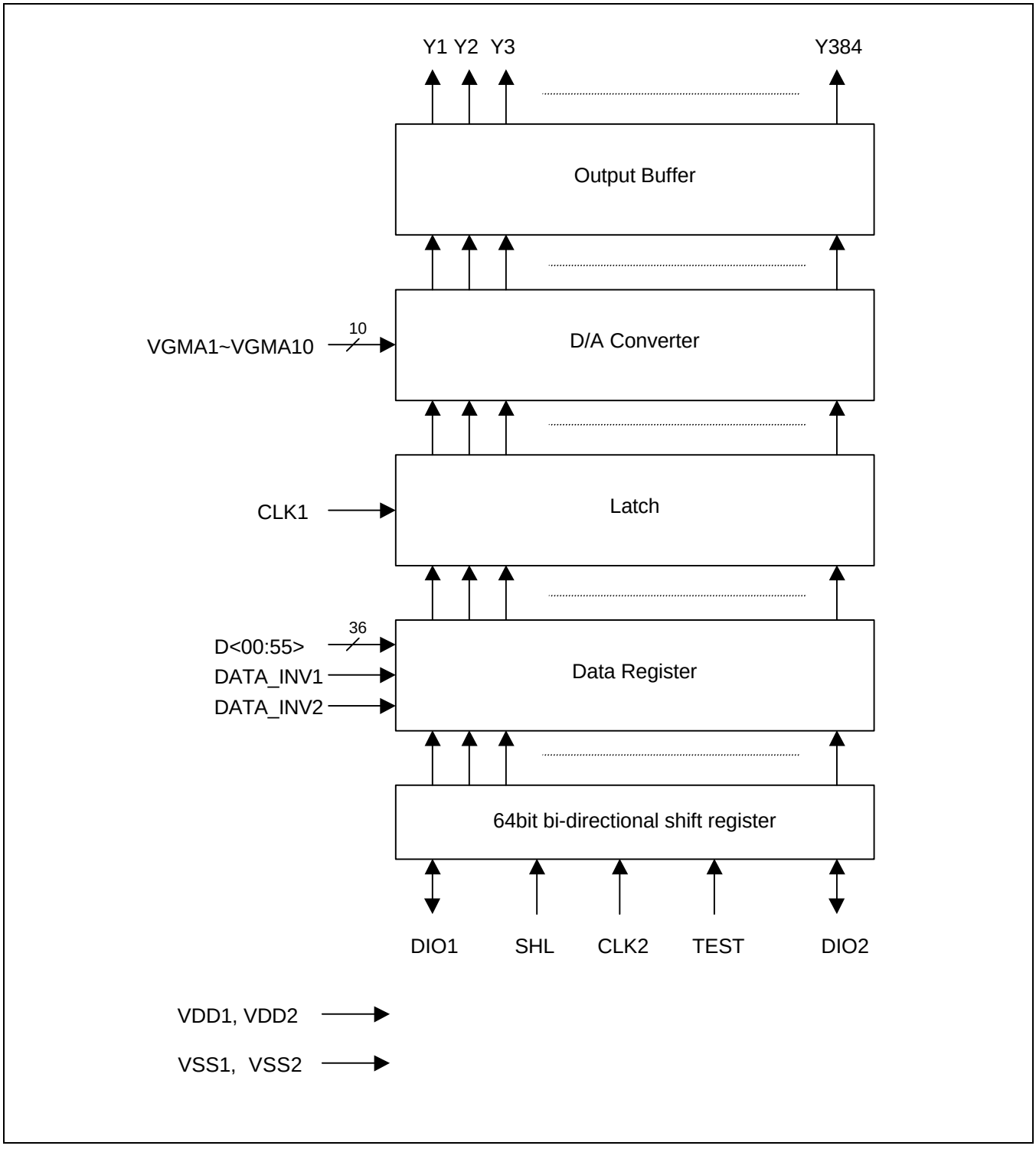
64G/S 384CH. SOURCE DRIVER

The KS0658 is a 384-channel output, TFT-LCD source driver for 64 gray scale displays.
Data input is a digital input consisting of 6 bits by 6 dots, while can realize a full-color display of 260,000 colors by output of 64 values γ - corrected.
This device has an internal D/A (digital-to-analog) converter for each output and utilizes 10 external power supplies.
The KS0658 can be adjusted to larger panel, and SHL (Shift direction selection) pin makes use of the LCD panel connection convenient. Maximum operation clock frequency is 55MHz at a 2.5V logic operation and it can be applied to the TFT LCD panel of XGA standards.

FEATURES

- ❑ TFT active matrix LCD source driver LSI.
- ❑ 64 outputs are possible through 10 external power supply and D/A converter
- ❑ CMOS level input
- ❑ 6 bits (G/S data) $\times$ 6 dots (RGB) input
- ❑ Input data inversion function. (DATA_INV1, DATA_INV2)
- ❑ Logic supply voltage: 2.5 to 3.6V
- ❑ LCD drive supply voltage: 3.0 to 5.5 Vp-p
- ❑ Maximum operation clock frequency:
  fmax = 55 MHz (internal data transmission rate at 2.5V operation)
- ❑ Output: 384 outputs.
- ❑ Slim TCP.

BLOCK DIAGRAM

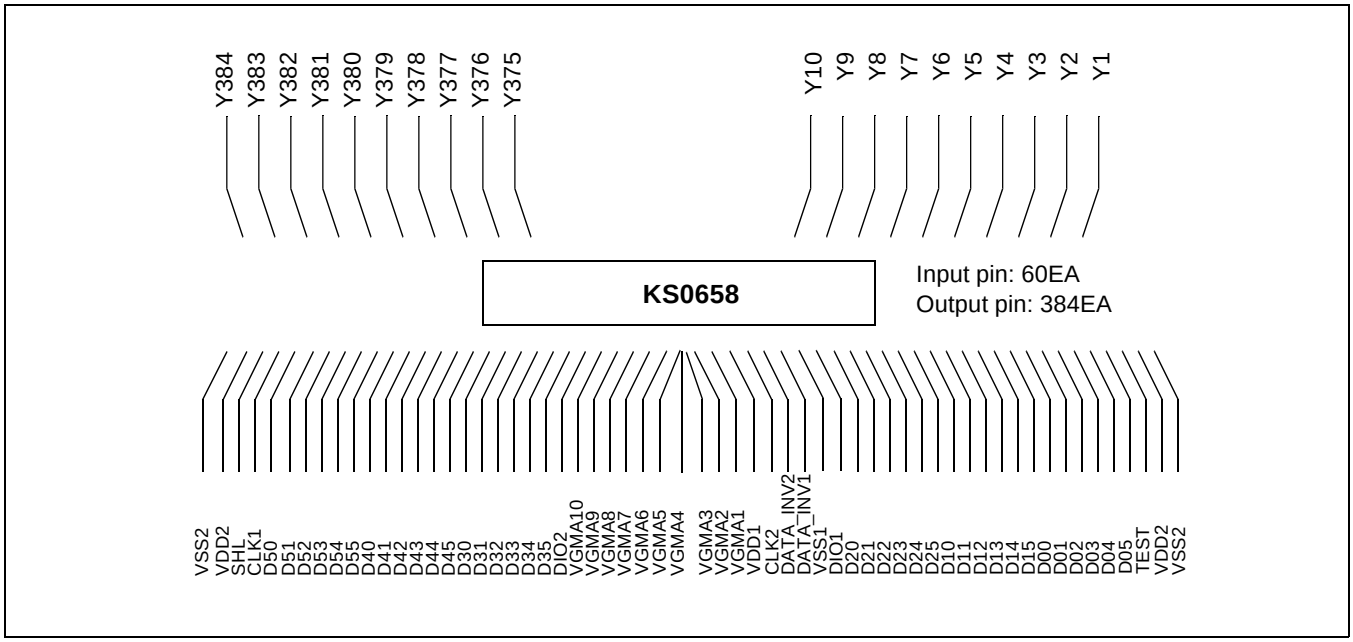


PIN DESCRIPTION

<table>
<tr><th>Pin Symbol</th><th>Pin Name</th><th>Description</th></tr>
<tr><td>VDD1</td><td>Logic power supply</td><td>2.7V to 3.6V</td></tr>
<tr><td>VDD2</td><td>Driver power supply</td><td>3.0V to 5.0V</td></tr>
<tr><td>VSS1</td><td>Logic ground</td><td>Ground (0V)</td></tr>
<tr><td>VSS2</td><td>Driver ground</td><td>Ground (0V)</td></tr>
<tr><td>Y1 to Y384</td><td>Driver Output</td><td>The D/A converted 64 G/S analog voltage is output</td></tr>
<tr><td>D0<0:5>
D1<0:5>
D2<0:5>
D3<0:5>
D4<0:5>
D5<0:5></td><td>Display data input</td><td>The display data is input with a width of 36 bits, gray scale data (6 bits) × 6 dots (R,G,B)
DX0: LSB, DX5: MSB</td></tr>
<tr><td>SHL</td><td>Shift direction control input</td><td>This pin controls the direction of shift register in cascade connection. The shift direction of the shift register is as follows.
SHL = H: DIO1 input (Y1 → Y384), DIO2 output
SHL = L: DIO2 input (Y384 → Y1), DIO1 output</td></tr>
<tr><td>DIO1</td><td>Right shift start pulse input/output</td><td>SHL = H: Used as the start pulse input pin
SHL = L: Used as the start pulse output pin</td></tr>
<tr><td>DIO2</td><td>Left shift start pulse input/output</td><td>SHL = H: Used as the start pulse output pin
SHL = L: Used as the start pulse input pin</td></tr>
<tr><td>CLK2</td><td>Shift clock input</td><td>Refer to shift clock input of the shift register. The display data is loaded to the data register at the rising edge of CLK2.</td></tr>
<tr><td>CLK1</td><td>Latch input</td><td>Latches the data register contents as rising edge and transfers it to the D/A converter. Also, after CLK1 input, clears the internal shift register contents. After 1 pulse input on start, operates normally. CLK1 input timing refers to the Relationship between CLK1 start pulse (DIO1,DIO2) and blanking period of the switching characteristic waveform. (page 9)</td></tr>
<tr><td>VGMA1 to VGMA10</td><td>γ-corrected power supplies</td><td>Input the γ-corrected power supplies from external source.
VDD2 > VGMA1 to VGMA10 > VSS2
Keep gray scale power supply unchanged during the gray scale voltage output.</td></tr>
<tr><td>DATA_INV1

DATA_INV2</td><td>Data inversion input</td><td>The input digital video signal is inverted by two data inversion input, DATA_INV1 and DATA_INV2.
<table>
<tr><td></td><td></td><td>DOX to 2X</td><td>DOX to 2X</td></tr>
<tr><td rowspan="2">DATA-INV1</td><td>H</td><td>Inversion</td><td>X</td></tr>
<tr><td>L</td><td>Not Inversion</td><td>X</td></tr>
<tr><td rowspan="2">DATA-INV2</td><td>H</td><td>X</td><td>Inversion</td></tr>
<tr><td>L</td><td>X</td><td>Not Inversion</td></tr>
</table>
</td></tr>
<tr><td>TEST</td><td>Test pin</td><td>TEST = L: Normal operation.TEST = H : TEST mode → OP AMP cut-off
This pin is internally pulled-down. < Rpd ≅ 30kΩ ></td></tr>
</table>

TCP PIN CONFIGURATION



NOTES:

1. This figure does not specify the dimensions of the TCP package.
2. In actual panel application, the power should be supplied through all the VDD2 and VSS2 pins simultaneously.

ABSOLUTE MAXIMUM RATINGS (VSS1 = VSS2 = 0V)

Characteristic	Symbol	Rating	Unit
Digital supply voltage	VDD1	–0.3 to +7.0	V
Analog supply voltage	VDD2	–0.3 to +7.0	V
Input voltage	VGMA1 to VGMA10	–0.3 to VDD2+0.3	V
	Other	–0.3 to VDD1+0.3	
Output voltage	DIO1, DIO2	–0.3 to VDD1+0.3	V
	Y1 to Y384	–0.3 to VDD2+0.3	
Operation Temperature	Topr	–20 to +75	°C
Storage Temperature	Tstg	–40 to +110	°C

If LSIs are stressed beyond the above absolute maximum ratings, they may be permanently destroyed.
These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the below recommended operating range is not implied.
Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

NOTE: Power on sequence VDD1 → input voltage → VDD2 → VGMA1 to VGMA10

RECOMMENDED OPERATION RANGE (Ta = –20 to +75°C, VSS1 = VSS2 = 0V)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital supply voltage	VDD1	fmax = 55MHz	2.5	–	3.6	V
Analog supply voltage	VDD2	–	3.0	–	5.5	V
γ-corrected voltage	VGMA1 to VGMA10	–	VSS2	–	VDD2	V
Max. clock frequency	*Note1. fmax	–	–	–	55	MHz
Output Load capacitance	CL	–	–	–	150	pF

NOTE: VDD1 = 2.5V

DC CHARACTERISTICS

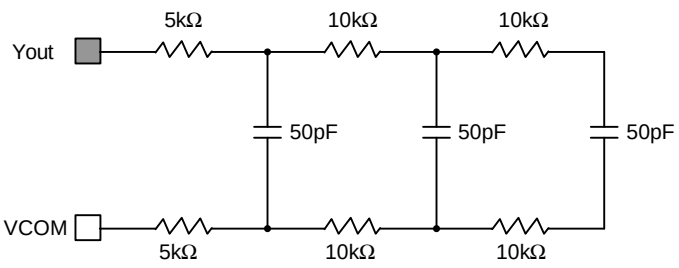
(Ta = -20 to +75°C, VDD1=2.5 to 3.6V, VDD2 = 3.0 to 5.5V, VSS1 = VSS2 = 0V)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
High level input voltage	VIH	SHL, CLK2, D00 to 55, CLK1, DIO1(DIO2), DATA_INV1, DATA_INV2	0.7VDD1	–	VDD1	V
Low level input voltage	VIL		0	–	0.3VDD1	
Input leak current	IL	D00 to D55, SHL, CLK2, CLK1, DATA_INV1, DATA_INV2	–0.5	–	5	µA
High level output voltage	VOH	DIO1(DIO2), VDD1 = 3.3V, IO = –2.0	VDD1-0.6	–	–	V
Low level output voltage	VOL	DIO1(DIO2), VDD1 = 3.3V, IO = +2.0	–	–	0.6	
Resistance between γ-corrected voltage	RGMA1 to RGMA9	*refer to page 13 resistance ladder circuit	0.7×Rtyp	*refer to page13	1.3×Rtyp	Ω
Driver output current	IVOH	VDD1 = 3.3V, VDD2 = 5.0V, Vx = 4.5V, VyO = 3.5V	–	–0.5	-0.3	mA
	IVOL	VDD1 = 3.3V, VDD2 = 5.0V, Vx = 0.5V, VyO = 1.5V	0.3	0.5	–	
Output voltage deviation	VO	VSS2+0.2 = YOUT = VDD2-0.2	–	±10	±20	mV
		YOUT < VSS2+0.2, YOUT > VDD2-0.2	–	±20	–	mV
Output voltage range	VYO	INPUT DATA: 00 to 3FH	VSS2+0.1	–	VDD2-0.1	V
Logic part dynamic current consumption	IDD1	*Note1, Note2.VDD1 = 3.3V No load.	–	3.5	5.5	mA
Driver part dynamic current consumption	IDD2	VDD1 = 3.3V, VDD2 = 5.0V VGMA1 = 4.0V, VGMA10 = 1.0V *Note1, Note2, Note3	–	10.0	13.0	

(Vyo is the output voltage of analog output pins Y1 to Y384.)
(Vx is the applied voltage of analog output pins Y1 to Y384.)

NOTES:

1. CLK1 cycle=20µs, fCLK2 = 33MHz, input data is alternated between 00 and 3F every last period 25µs.
2. The current consumption per driver when XGA single-sided mounting (8units) are connected in cascade.
3. Yout load condition.



AC CHARACTERISTICS

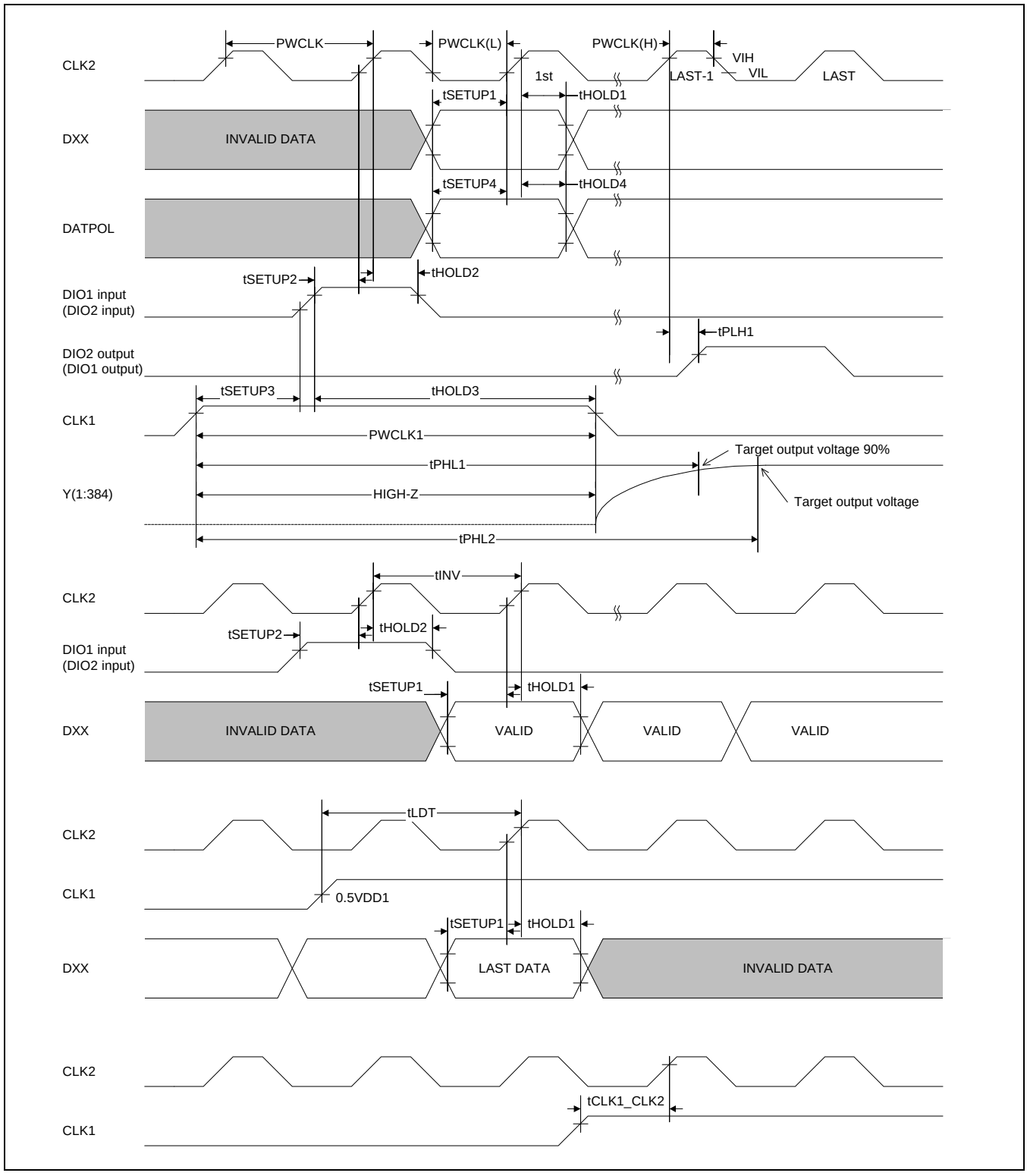
(Ta = –20 to +75°C, VDD1 = 2.5 to 3.6V, VDD2 = 3.0 to 5.5V, VSS1 = VSS2 = 0V)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Clock pulse width	PWCLK	–	18	–	–	ns
Clock pulse low period	PWCLK(L)	–	4	–	–	
Clock pulse high period	PWCLK(H)	–	4	–	–	
Data setup time	tSETUP1	–	4	–	–	
Data hold time	tHOLD1	–	2	–	–	
DATA_INV1 setup time	tSETUP11	–	4	–	–	
DATA_INV2 hold time	tHOLD11	–	2	–	–	
Start pulse setup time	tSETUP2	–	4	–	–	
Start pulse hold time	tHOLD2	–	2	–	–	
Start pulse delay time	tPLH1	VDD1=3.3V, CL=15pF	–	–	14	
CLK1 setup time	tSETUP3	–	1	–	–	CLK2 cycle
CLK1 hold time	tHOLD3	–	4	–	–	ns
CLK1 high pulse width	PWCLK1	–	2	–	–	CLK2 cycle
Driver output delay time(1)	tPHL1	refer to Note3 (page6), Note4.	–	–	5	s
Driver output delay time(2)	tPHL2	refer to Note3 (page6), Note5.	–	–	10	
Data invalid time	tINV	Note 6	1	–	–	CLK2 cycle
Last data timing	tLDT	–	1	–	–	
CLK1-CLK2 time	tCLK1-CLK2	CLK1 ↑ or ↓ → CLK2 ↑	4	–	–	ns

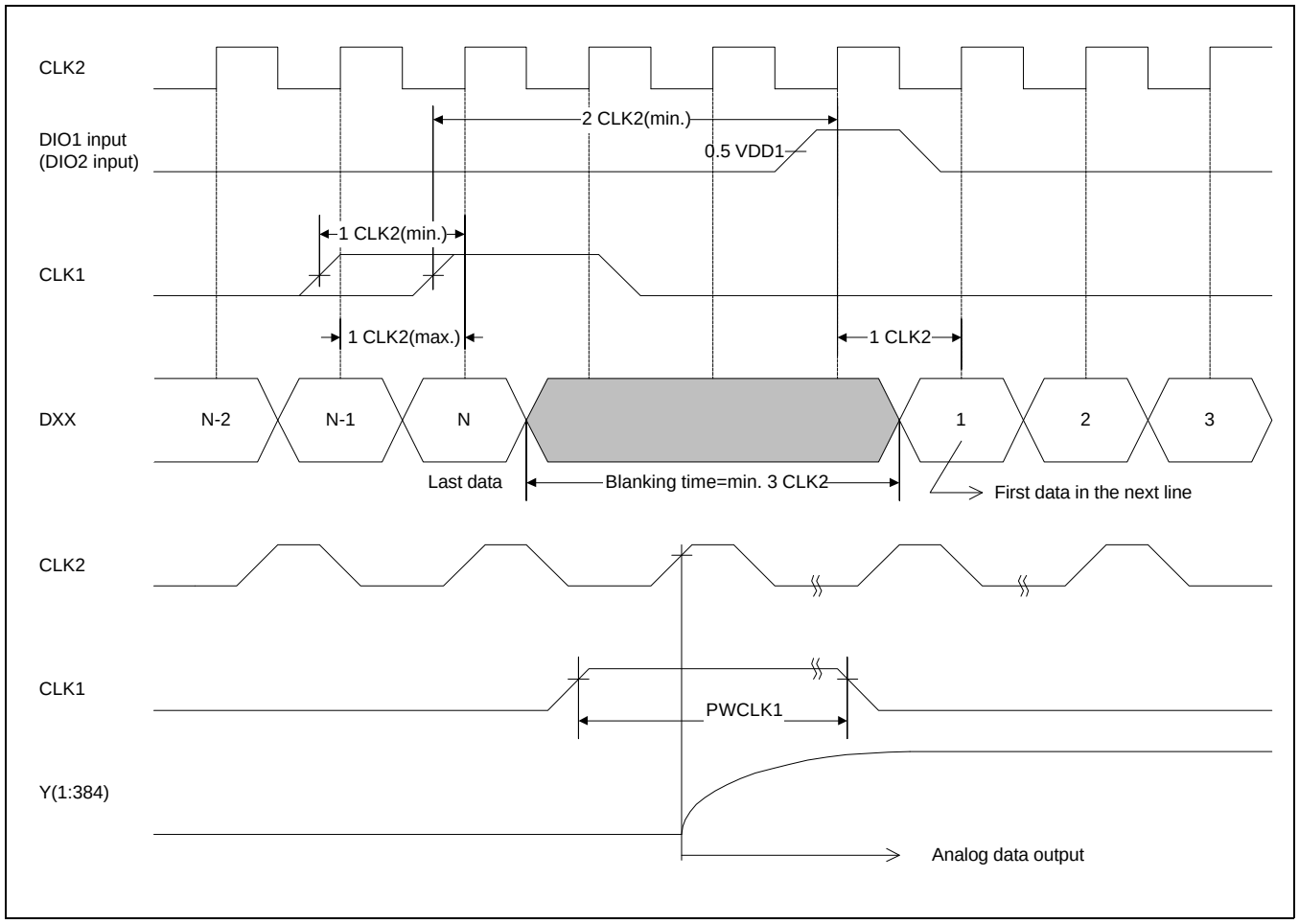
NOTES:

4. The value is specified when the drive voltage value reaches the target output voltage level of 90%
5. The value is specified when the drive voltage value reaches the target output voltage level of 6-bit accuracy.
6. Set the rising edge of the first CLK2 after the rising edge of DIO1(or DIO2).

AC Waveform (VIH = 0.7VDD1, VIL= 0.3VDD1)



Relationship between CLK1/start pulse (DIO1, DIO2) and blanking period.



DISPLAY DATA TRANSFER

DIO1 (or DIO2) = H is loaded into internal latch at the rising edge of CCLK2, which starts the data transfer operation, and after the falling edge of DIO1 (or DIO2), display data is valid at the rising edge of CLK2.
Once all the data of 384 channels is loaded into internal latch, it goes into standby state automatically, and any new data is not accepted even though CLK2 is provided until next DIO1(or DIO2) input.
When DIO1 (or DIO2) is provided, new display data is valid at the next rising edge of CLK2 after the falling edge of DIO1 (or DIO2).

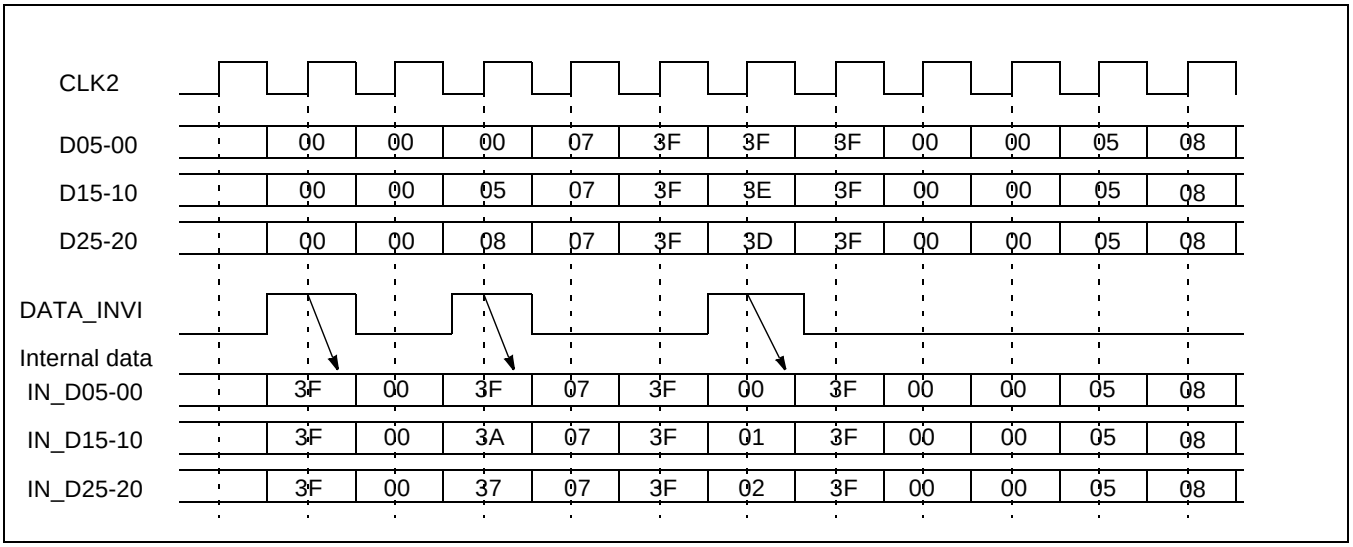
EXTENSION OF OUTPUT

Output pin can be adjusted to an extended screen by cascade connection.

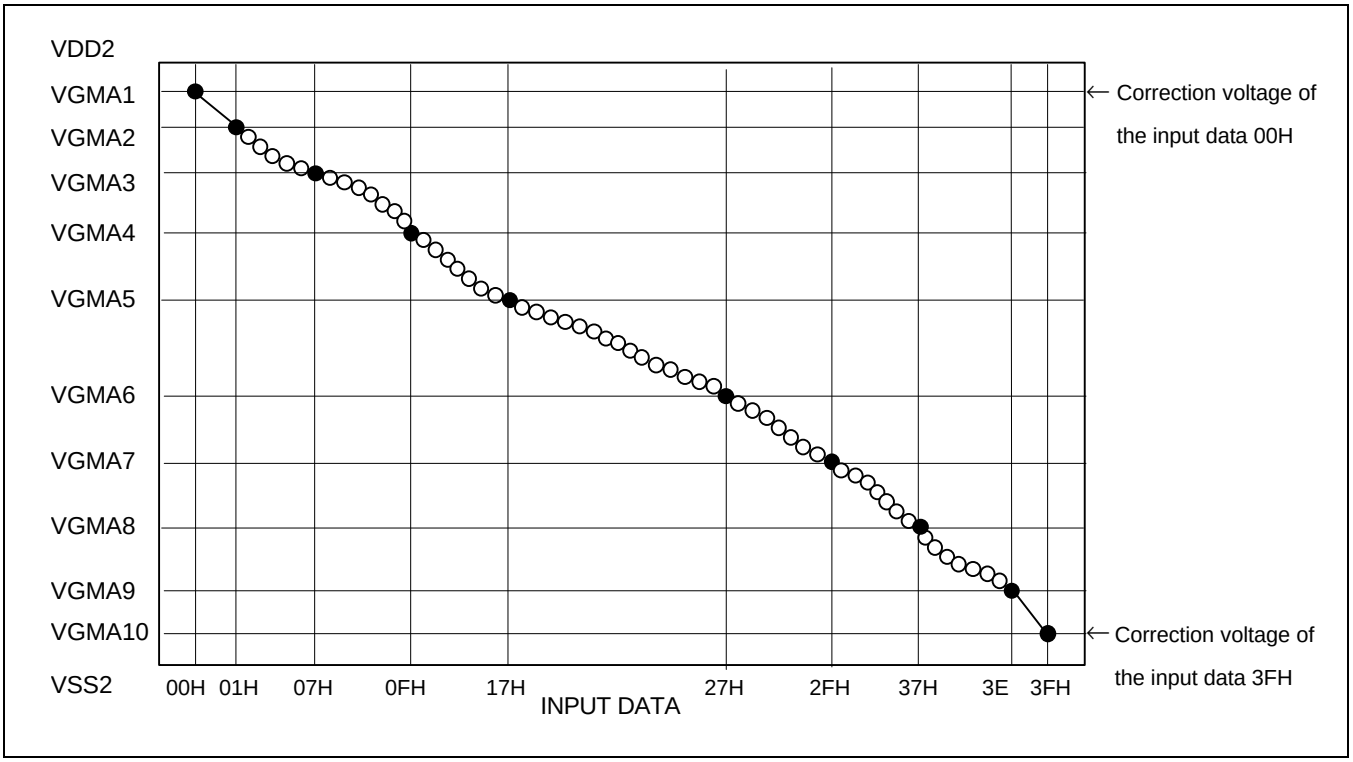
- SHL = L
  Connect DIO1 pin of previous stage to the DIO2 pin of next stage and all the input pins except DIO1 and DIO2 are connected together in each device.
- SHL = H
  Connect DIO2 pin of previous stage to the DIO1 pin of next stage and all the input pins except DIO1 and DIO2 are connected together in each device.

THE FUNCTION OF THE DATA INVERSION

The input digital video signal is inverted by two data inversion input, DATA_INV1 and DATA_INV2. When data inversion input is high, the digital video signal can be inverted.
Each data inversion input inverts 18 data, respectively DATA_INV1 inverts D00 to D25 and DATA_INV2 does D35 to D55. The below timing diagram shows how data is inverted. DATA_INV2 inverts data the same way.



γ - Correction Characteristic Curve



RELATIONSHIP BETWEEN THE INPUT DATA AND OUTPUT VOLTAGE

Relationship #1 Between The Input Data and Output Voltage

Outputs 64-level gray scale voltage generated by level 10 of γ-corrected power supplies (VGMA1 to VGMA10) and 6-bit digital data.
data format : 1PIXEL data (6 bits) × 2RGB(6 dots)
input width : 36 bits.

- Details on display data

DX5	DX4	DX3	DX2	DX1	DX0
Upper bits					Lower bits

- Relationship between shift direction and output data

SHL = H (Right shift)

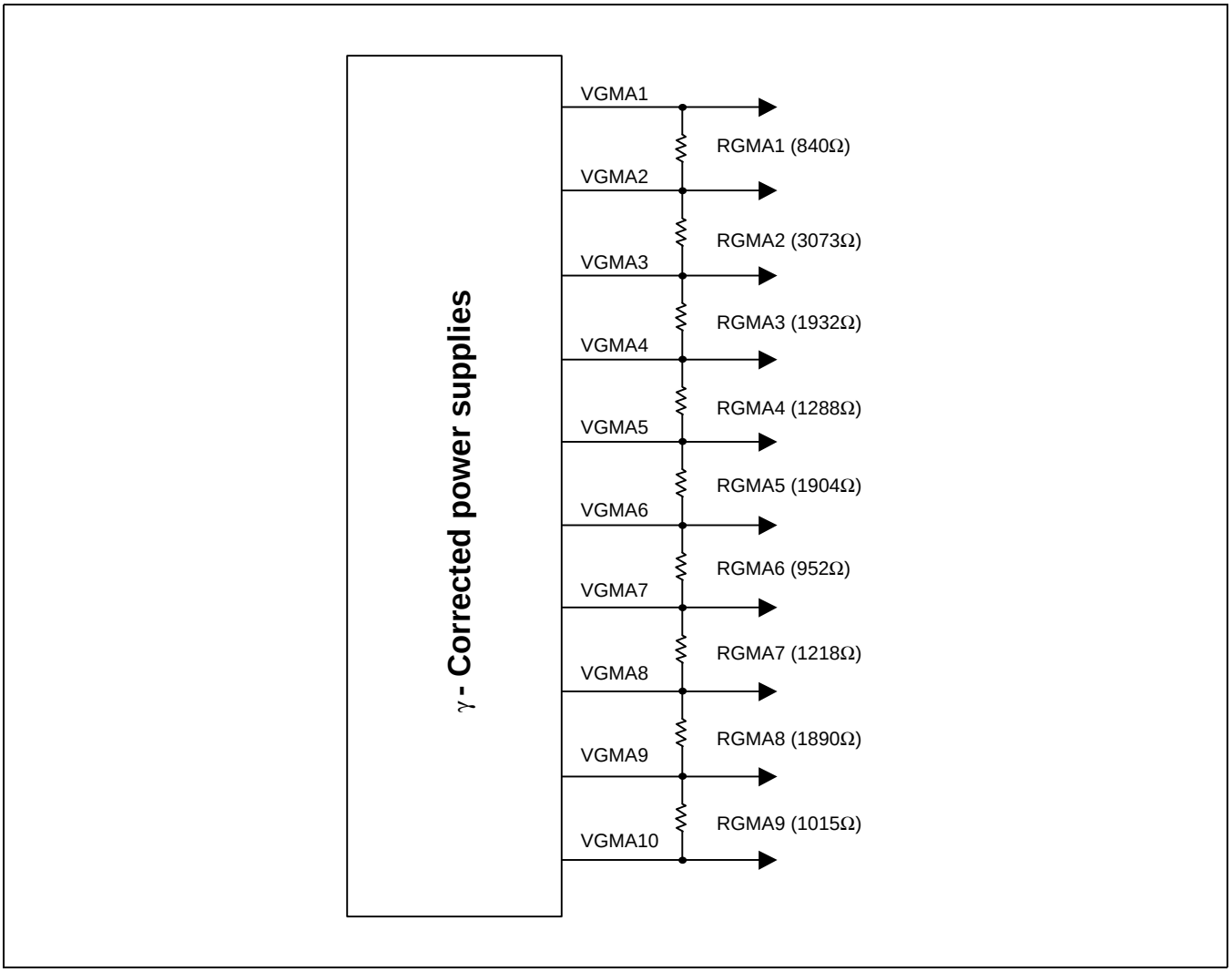
Output	Y1	Y2	Y3	-------	Y382	Y383	Y384
–	First			→	Last		
DATA	D00 to D05	D10 to D15	D20 to D25	-------	D30 to D35	D40 to D45	D50 to D55

SHL = L (Left shift)

Output	Y1	Y2	Y3	-------	Y382	Y383	Y384
–	Last			→	First		
DATA	D00 to D05	D10 to D15	D20 to D25	-------	D30 to D35	D40 to D45	D50 to D55

RELATIONSHIP #1 BETWEEN THE INPUT DATA AND OUTPUT VOLTAGE

All 384outputs of the KS0658 are driven by separate 6-bit D/A converters. The output voltage of each D/A converter, 64-level gray scale voltage, is determined by the reference voltages VGMA1 to VGMA10. The D/A converter consists of ladder resistors of which R0 to R63 are so designed that the ratios between the LCD panels γ-corrected voltages and V0 to V63.



RGMA1 + RGMA2 + ... + RGMA8 + RGMA9 ≅ 14.1kΩ

RELATIONSHIP #2 BETWEEN THE INPUT DATA AND OUTPUT VOLTAGE

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
00	0	0	0	0	0	0	V0	VGMA1
01	0	0	0	0	0	1	V1	VGMA2
02	0	0	0	0	1	0	V2	VGMA3+(VGMA2-VGMA3)×2352/3073
03	0	0	0	0	1	1	V3	VGMA3+(VGMA2-VGMA3)×1806/3073
04	0	0	0	1	0	0	V4	VGMA3+(VGMA2-VGMA3)×1260/3073
05	0	0	0	1	0	1	V5	VGMA3+(VGMA2-VGMA3)× 840/3073
06	0	0	0	1	1	0	V6	VGMA3+(VGMA2-VGMA3)× 420/3073
07	0	0	0	1	1	1	V7	VGMA3
08	0	0	1	0	0	0	V8	VGMA4+(VGMA3-VGMA4)×1624/1932
09	0	0	1	0	0	1	V9	VGMA4+(VGMA3-VGMA4)×1316/1932
0A	0	0	1	0	1	0	V10	VGMA4+(VGMA3-VGMA4)×1078/1932
0B	0	0	1	0	1	1	V11	VGMA4+(VGMA3-VGMA4)× 840/1932
0C	0	0	1	1	0	0	V12	VGMA4+(VGMA3-VGMA4)× 602/1932
0D	0	0	1	1	0	1	V13	VGMA4+(VGMA3-VGMA4)× 364/1932
0E	0	0	1	1	1	0	V14	VGMA4+(VGMA3-VGMA4)× 182/1932
0F	0	0	1	1	1	1	V15	VGMA4
10	0	1	0	0	0	0	V16	VGMA5+(VGMA4-VGMA5) × 7/8
11	0	1	0	0	0	1	V17	VGMA5+(VGMA4-VGMA5) × 6/8
12	0	1	0	0	1	0	V18	VGMA5+(VGMA4-VGMA5) × 5/8
13	0	1	0	0	1	1	V19	VGMA5+(VGMA4-VGMA5) × 4/8
14	0	1	0	1	0	0	V20	VGMA5+(VGMA4-VGMA5) × 3/8
15	0	1	0	1	0	1	V21	VGMA5+(VGMA4-VGMA5) × 2/8
16	0	1	0	1	1	0	V22	VGMA5+(VGMA4-VGMA5) × 1/8
17	0	1	0	1	1	1	V23	VGMA5
18	0	1	1	0	0	0	V24	VGMA6+(VGMA5-VGMA6) × 15/16
19	0	1	1	0	0	1	V25	VGMA6+(VGMA5-VGMA6) × 14/16
1A	0	1	1	0	1	0	V26	VGMA6+(VGMA5-VGMA6) × 13/16
1B	0	1	1	0	1	1	V27	VGMA6+(VGMA5-VGMA6) × 12/16
1C	0	1	1	1	0	0	V28	VGMA6+(VGMA5-VGMA6) × 11/16
1D	0	1	1	1	0	1	V29	VGMA6+(VGMA5-VGMA6) × 10/16
1E	0	1	1	1	1	0	V30	VGMA6+(VGMA5-VGMA6) × 9/16
1F	0	1	1	1	1	1	V31	VGMA6+(VGMA5-VGMA6) × 8/16

g - Corrected Voltage Vaule

VGMA1	4.00V	VGMA6	2.09V
VGMA2	3.82V	VGMA7	1.89V
VGMA3	3.15V	VGMA8	1.63V
VGMA4	2.74V	VGMA9	1.22V
VGMA5	2.00V	VGMA10	1.00V

RELATIONSHIP #2 BETWEEN THE INPUT DATA AND OUTPUT VOLTAGE

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
20	1	0	0	0	0	0	V32	VGMA6+(VGMA5-VGMA6) × 7/16
21	1	0	0	0	0	1	V33	VGMA6+(VGMA5-VGMA6) × 6/16
22	1	0	0	0	1	0	V34	VGMA6+(VGMA5-VGMA6) × 5/16
23	1	0	0	0	1	1	V35	VGMA6+(VGMA5-VGMA6) × 4/16
24	1	0	0	1	0	0	V36	VGMA6+(VGMA5-VGMA6) × 3/16
25	1	0	0	1	0	1	V37	VGMA6+(VGMA5-VGMA6) × 2/16
26	1	0	0	1	1	0	V38	VGMA6+(VGMA5-VGMA6) × 1/16
27	1	0	0	1	1	1	V39	VGMA6
28	1	0	1	0	0	0	V40	VGMA7+(VGMA6-VGMA7) × 7/8
29	1	0	1	0	0	1	V41	VGMA7+(VGMA6-VGMA7) × 6/8
2A	1	0	1	0	1	0	V42	VGMA7+(VGMA6-VGMA7) × 5/8
2B	1	0	1	0	1	1	V43	VGMA7+(VGMA6-VGMA7) × 4/8
2C	1	0	1	1	0	0	V44	VGMA7+(VGMA6-VGMA7) × 3/8
2D	1	0	1	1	0	1	V45	VGMA7+(VGMA6-VGMA7) × 2/8
2E	1	0	1	1	1	0	V46	VGMA7+(VGMA6-VGMA7) × 1/8
2F	1	0	1	1	1	1	V47	VGMA7
30	1	1	0	0	0	0	V48	VGMA8+(VGMA7-VGMA8) ×1092/1218
31	1	1	0	0	0	1	V49	VGMA8+(VGMA7-VGMA8) × 966/1218
32	1	1	0	0	1	0	V50	VGMA8+(VGMA7-VGMA8) × 840/1218
33	1	1	0	0	1	1	V51	VGMA8+(VGMA7-VGMA8) × 686/1218
34	1	1	0	1	0	0	V52	VGMA8+(VGMA7-VGMA8) × 532/1218
35	1	1	0	1	0	1	V53	VGMA8+(VGMA7-VGMA8) × 378/1218
36	1	1	0	1	1	0	V54	VGMA8+(VGMA7-VGMA8) × 189/1218
37	1	1	0	1	1	1	V55	VGMA8
38	1	1	1	0	0	0	V56	VGMA9+(VGMA8-VGMA9) ×1701/1890
39	1	1	1	0	0	1	V57	VGMA9+(VGMA8-VGMA9) ×1512/1890
3A	1	1	1	0	1	0	V58	VGMA9+(VGMA8-VGMA9) ×1323/1890
3B	1	1	1	0	1	1	V59	VGMA9+(VGMA8-VGMA9) ×1134/1890
3C	1	1	1	1	0	0	V60	VGMA9+(VGMA8-VGMA9) × 868/1890
3D	1	1	1	1	0	1	V61	VGMA9+(VGMA8-VGMA9) × 504/1890
3E	1	1	1	1	1	0	V62	VGMA9
3F	1	1	1	1	1	1	V63	VGMA10

RGMA (g-Corrected Resistance) RATIO. (If the RGMA1 equals 1)

RGMA1	1.000	RGMA6	1.133
RGMA2	3.658	RGMA7	1.450
RGMA3	2.300	RGMA8	2.250
RGMA4	1.533	RGMA9	1.208
RGMA5	2.267		

* RGMA1 = 840Ω