# INTRODUCTION

The KS16118 is a facsimile controller that provides major functions on a single chip. It contains a fax modem with an Analog Front-End (AFE), a CPU, an image processor with a codec accelerator, CPU peripheral circuits, and general purpose I/O ports. The peripheral circuits include an 8-bit timer, 2-channel Serial I/O (SIO), 3-channel direct memory access (DMA), a real time clock, and a tone generator. The fax modem, which is functionally the same as the KS16116, is a synchronous, half-duplex modem capable of speeds up to 9600 bps. The image processor includes a 6-bit half-flash A/D converter, a scanner controller, THP interfaces, and a codec accelerator.
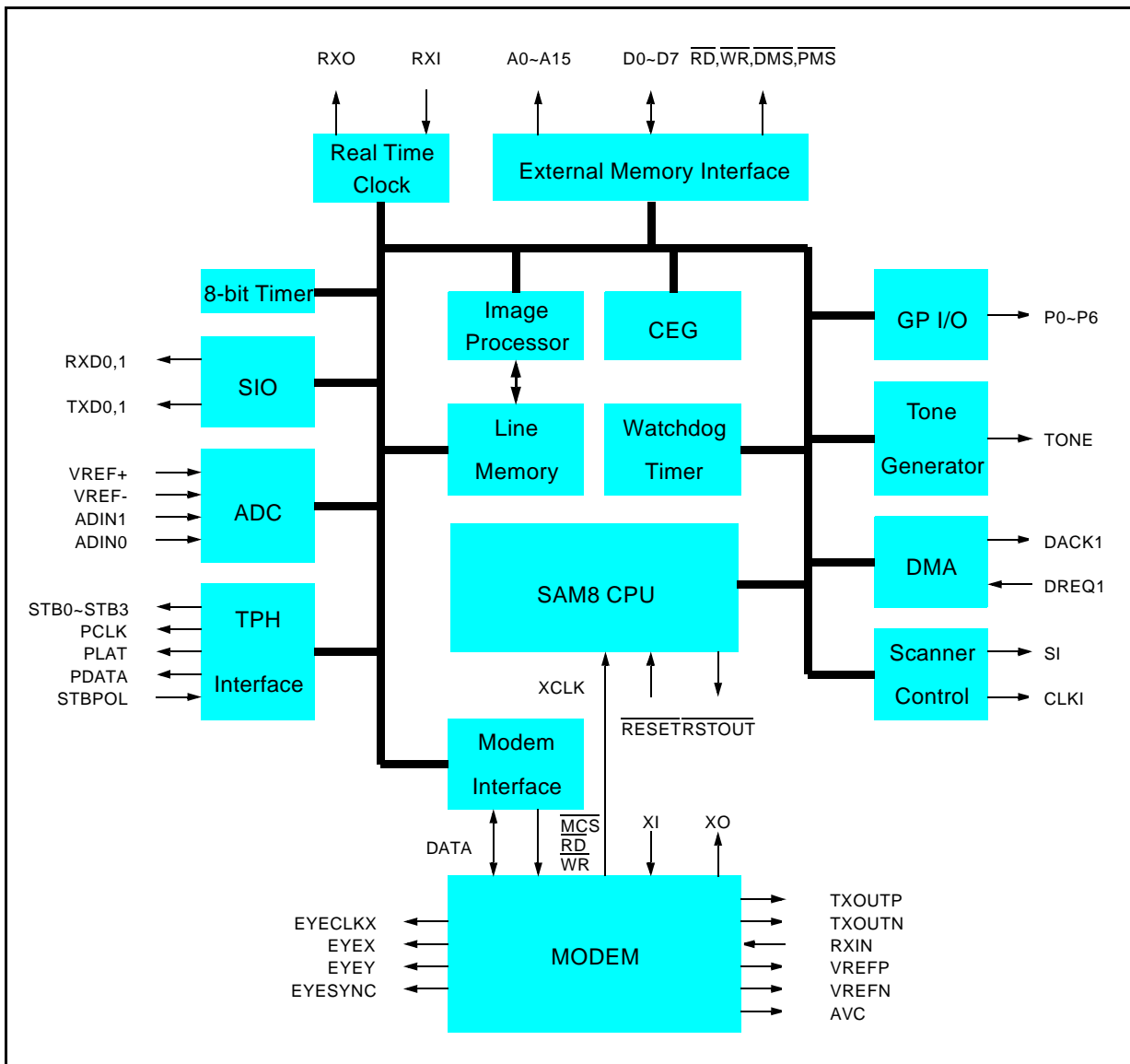
Each functional block is equipped with many versatile functions. All functions necessary for home facsimile machine as well as small business facsimile machine are intergrated in a single chip. The KS16118 is housed in 144-QFP and operates with +5V single power.

144-QFP-2828-AN

KS16118
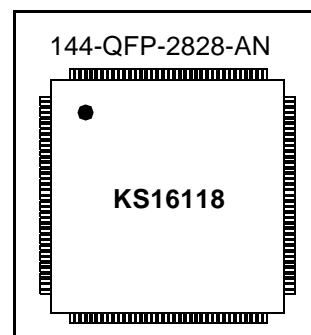
FEATURES

- CPU
  - SAM8 CPU core
- Memory
  - 64-Kbyte external data or peripheral memory
  - 64-Kbyte external program memory
  - 128 general purpose registers
  - 16 working registers
  - 104 system and peripheral registers
- Interrupts
  - 5 interrupt levels
  - 10 interrupt sources with 9 vectors
  - Fast interrupt processing
- Watchdog Timer
  - 8-bit timer for noise protection or interrupts
- I/O Ports
  - Five output ports (32 pins)
  - One input port (4 pins)
  - Three bidirectional ports (20 pins)
- Serial Ports
  - 2 channel serial I/O for serial communication to an operational panel, etc.
- 8-bit Timer
  - An 8-bit timer for timing schedule
  - Auto-reload method
- External Interface
  - Programmable waits for external memory and peripheral chip selection
  - Three DMA channels
- Tone Generator
  - 366 Hz to 93.75 KHz at 12 MHz CPU clock

- Real Time Clock
  - Operate with 3V backup battery
  - Low power consumption
- A/D Converter
  - Two channels for TPH and scanner input
  - Half-flash, 6-bit resolution
  - 8 CPU-clocks peak conversion time
- Scanner Control Block
  - 1728 or 2048-pixel scan width
  - Minimum scanning time: 5ms
- Image Processing Unit
  - Decimation by 1% (up to 50%)
  - Shading correction for A4 and B4 size
  - 64-gray level half-tone processing
  - 2048X6 bits line memory for error diffusion
  - 2048X6 bits line memory for shading correction
  - 64X6 bits line memory for gamma-correction
  - Edge emphasis and edge strength
  - Programmable threshold generation
  - Peak value detection
- TPH Interface Block
  - Up to 4 TPH strobes
- Changing Element Generator (CEG)
  - For T.4 MH/MR compression and decompression
- Modem
  - Group 3 facsimile transmission/reception according to ITU-T V.29, V.27ter short and long train, V.21 Ch2, T.30, and T.4
  - Half-duplex operation
  - Receiver dynamic range: 0 dBm to -43 dBm
  - Programmable transmit level: 0 dBm to -15 dBm

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- Programmable transmit attenuation: 0 dB to 14 dB in 2 dB step
- Programmable DTMF generation/detection
- Programmable tone generation/detection
- Programmable interface memory interrupt
- Programmable turn-on and turn-off threshold
- Automatic T/2 adaptive equalizer
- HDLC capability at all speeds
- Diagnostic capability allowing telephone line quality monitoring
- ITU-T V.24 compatible interface
- Caller ID reception and detection

- Software compatible with KS16116
- Miscellanies
  - 24.00014 MHz
  - Crystal, ceramic, or external clock sources
  - Operating Temperature Range: 0°C to 70°C
  - Operating Voltage Range: +4.75 to +5.25V
  - Package Type: 144-pin QFP
- ESD Mode
  - HBM(Human Body Model): ± 2,000V
  - MM(Machine Model): ± 300V
  - CDM(Charged Device Model): ± 800V

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KS16118 Pin Assignments

Top pins (144–109): VDDR, RXI, RXO, TEST, TONE, P5<7>, P5<6>, P5<5>, P5<4>, P2<3>, P2<2>, P2<1>, P2<0>, VSS, VDD, XO, XI, VSS, P5<0>, P1<7>, P1<6>, P1<5>, P1<4>, P1<3>, P1<2>, P1<1>, P1<0>, P6<7>, P6<6>, ADOUT, EYECLKX, EYEX, EYEY, EYESYNC, VSS, VDD

Left pin	Signal		Signal	Right pin
1	RESET		VREFP	108
2	D7		AVC	107
3	D6		VSSA	106
4	D5		VDDA	105
5	D4		RXIN	104
6	D3		TXOUTP	103
7	D2		TXOUTN	102
8	D1		VSSA	101
9	D0		VREFN	100
10	VDD		VSS	99
11	VSS		VDD	98
12	PMS		VSS	97
13	DMS		P5<3>	96
14	RD		P5<1>	95
15	WR		P4<0>	94
16	A15		P4<1>	93
17	A14		P4<2>	92
18	A13		P4<3>	91
19	A12		P4<4>	90
20	A11		P4<5>	89
21	A10		P4<7>	88
22	A9		P4<6>	87
23	A8		P0<5>	86
24	VDD		P0<6>	85
25	VSS		P0<7>	84
26	A7		CLKI	83
27	A6		SI	82
28	A5		VDD	81
29	A4		VSS	80
30	A3		VREFO	79
31	A2		VSSADC	78
32	A1		VREF+	77
33	A0		VREF-	76
34	P0<0>		ADIN1	75
35	P0<1>		VDDADC	74
36	GIDIS		ADIN0	73

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Bottom pins (37–72): XCLK, RSTOUT, P0<2>, P0<3>, P0<4>, VSS, VDD, SCK1, P2<4>, P2<5>, P2<6>, P2<7>, P3<0>, P3<1>, P3<2>, P3<3>, P3<4>, P3<5>, P3<6>, P3<7>, P5<2>, P6<0>, P6<1>, P6<2>, P6<3>, P6<4>, P6<5>, VSS, STBPOL, STB3, STB2, STB1, STB0, PLAT, PCLK, PDATA