KS57C2202
4-BIT CMOS Microcontroller

Product Specification

PRODUCT OVERVIEW

The KS57C2202 single-chip CMOS microcontroller has been designed for very high performance using Samsung's newest 4-bit CPU core. With an up-to-16-digit LCD direct drive capability, a melody generator with 256-word melody ROM, and 8-bit timer/counter, the KS57C2202 offers you an excellent design solution for a wide variety of applications that require LCD and melody generator functions.

Up to 25 pins of the 64-pin QFP package can be dedicated to I/O. Six vectored interrupts provide fast response to internal and external events. In addition, the KS57C2202's advanced CMOS technology ensures low power consumption and a wide operating voltage range.

FEATURES

Memory

- 256 × 4-bit RAM
- 2048 × 8-bit ROM

25 I/O Pins

- Input only: 2 pins
- Output only: 8 pins (if not used for segment output)
- I/O: 15 pins

LCD Controller/Driver

- 32 segments × 4 commons: static, 1/2 duty (1/2 bias), 1/3 duty (1/2 bias)
- 1/3 duty (1/3 bias), 1/4 duty (1/3 bias)

Melody Generator

- Single tone and sound effect generation
- 16 notes, 63 tones
- 16 tempos
- 256 × 12-bit melody ROM

8-Bit Basic Timer

- Four interval timer functions

8-Bit Timer/Counter

- Programmable 8-bit timer
- Arbitrary clock output

Watch Timer

- Time interval generation: 0.5s, 3.9 ms at 32768 Hz
- Clock generation for LCD

Interrupts

- 3 internal interrupt vectors
- 3 external interrupt vectors
- 1 quasi-interrupt

Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary format

Memory-Mapped I/O Structure

- Data memory bank 15

Two Power-Down Modes

- Idle (only CPU clock stops)
- Stop (system clock stops)

Oscillation Sources

- Crystal oscillator for system clock
- System clock frequency of 32.768 kHz (typical)

Instruction Execution Times

- 122 μs at 32.768kHz

Power Consumption

- Operating mode: 14 μA (typical) at 3 V, 32.768 kHz
- Idle mode: 7 μA (typical) at 3V, 32.768 kHz
- Stop mode: 0.8 μA (typical) at 3V, 32.768 kHz

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 2.7 V to 6.0 V

Package Type

- 64-pin QFP

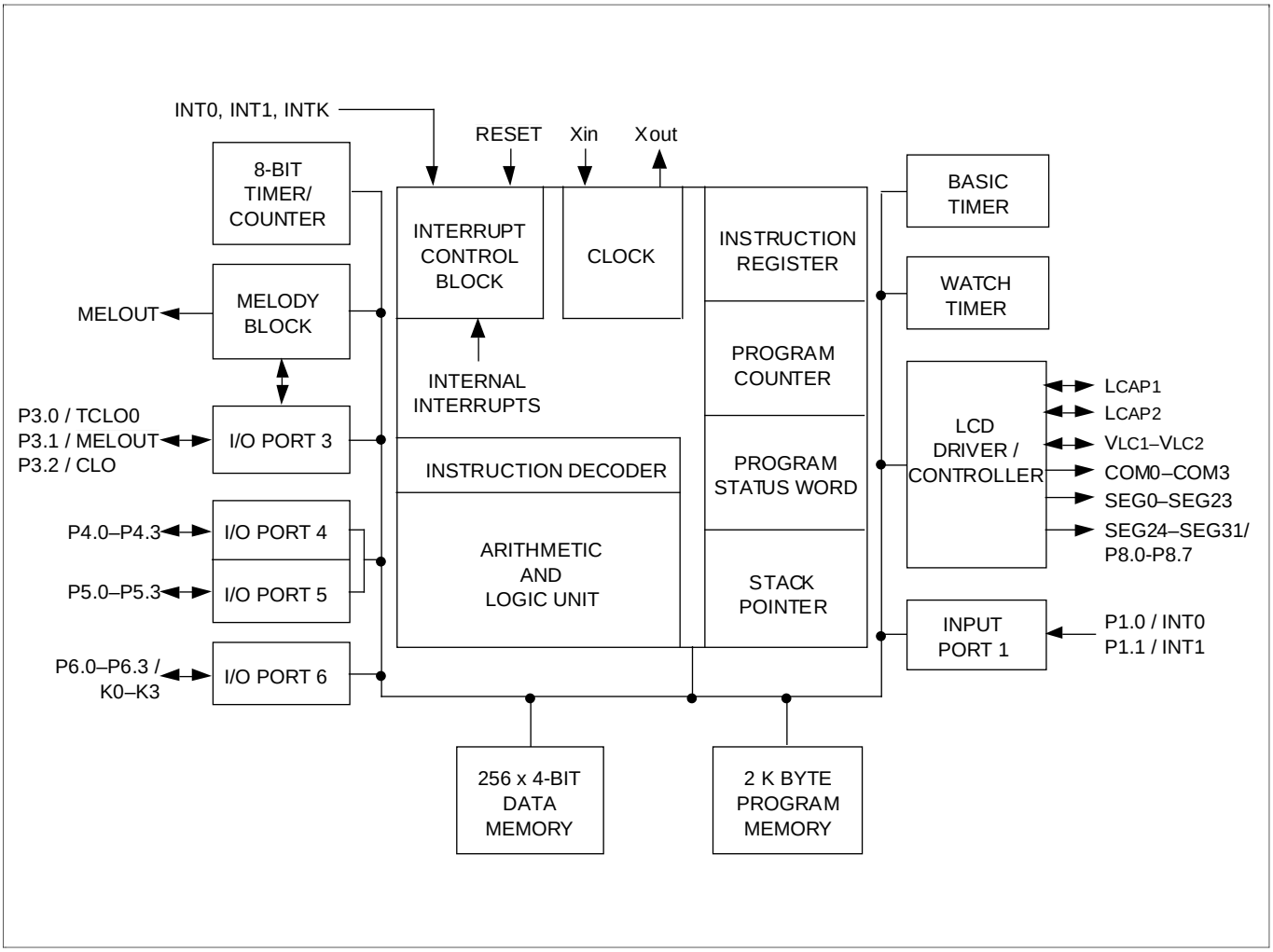

Figure 1. KS57C2202 Block Diagram

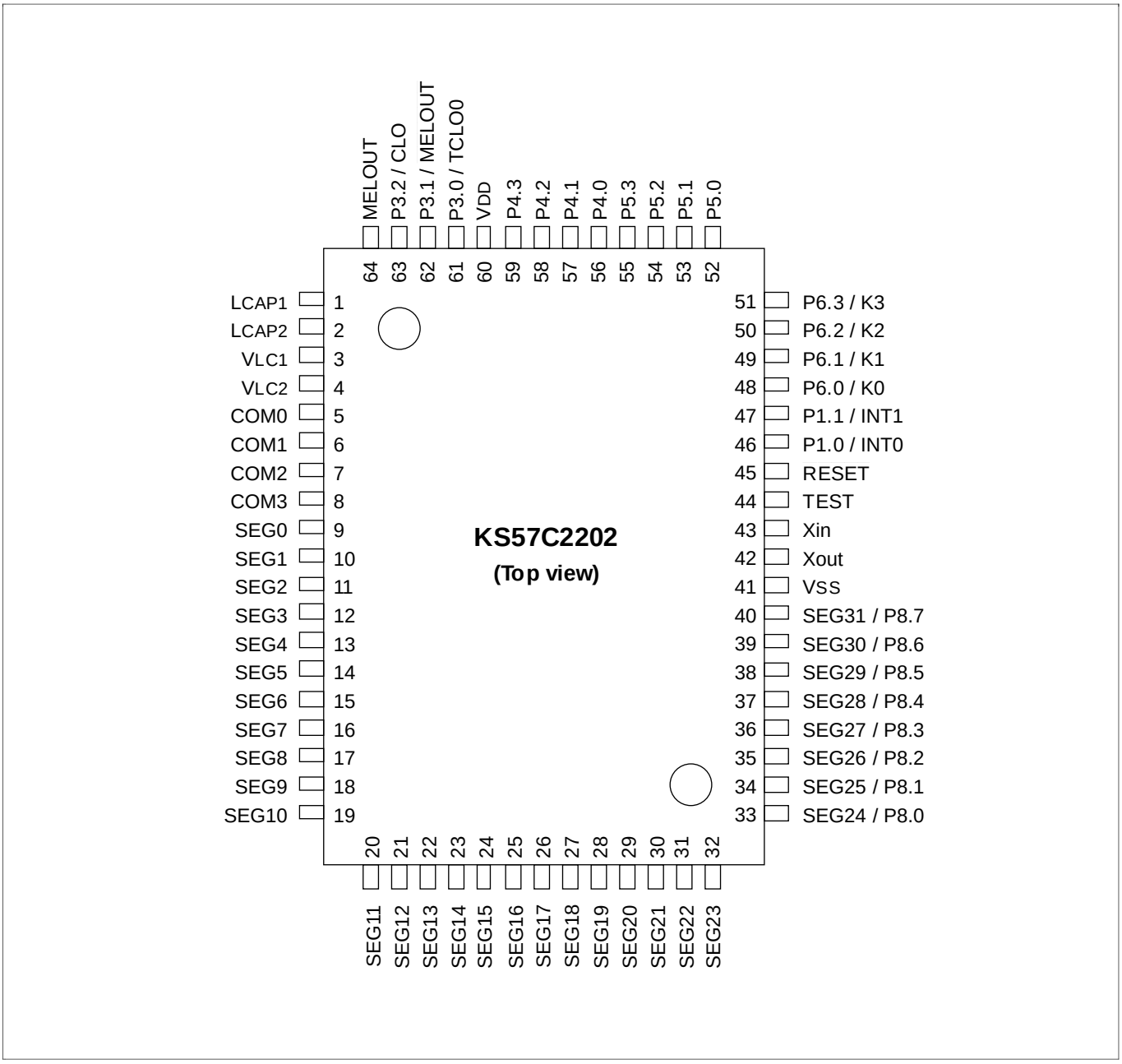

Figure 2. KS57C2202 Pin Assignments (64-QFP)

Table 1. KS57C2202 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P1.0 P1.1	I	2-bit input port. 1-bit and 2-bit read and test is possible. 2-bit pull-up resistors are software assignable.	46 47	INT0 INT1
P3.0 P3.1 P3.2	I/O	3-bit I/O port. 1-bit or 3-bit read/write and test is possible. Pins are individually software configurable as input or output. 3-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	61 62 63	TCLO0 MELOUT CLO
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. Ports 4 and 5 can be configured individually as n-channel open-drain or as CMOS push-pull output by software. 1-bit and 4-bit read/write and test is possible. Ports 4 and 5 can be paired to enable 8-bit data transfer. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	56–59 52–55	—
P6.0–P6.3	I/O	4-bit I/O ports. 1-bit and 4-bit read/write and test is possible. Pins are individually software configurable as input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	48–51	K0–K3
P8.0–8.7	O	Output port for 1-bit data (if segment outputs are not used)	33–40	SEG24–SEG31
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable.	46, 47	P1.0, P1.1
TCLO0	I/O	Timer/counter clock output	61	P3.0
MELOUT	I/O	Complement of melody output	62	P3.1
CLO	I/O	Clock output	63	P3.2
K0–K3	I/O	External interrupt inputs with falling edge detection	48–51	P6.0–P6.3
SEG0–SEG23	O	LCD segment output	9–32	—
SEG24–SEG31	O	LCD segment output	33–40	P8.0–P8.7
COM0–COM3	O	LCD common signal output	5–8	—
L_{CAP1}, L_{CAP2}	—	Switching pins for supplying LCD driving voltage to the V_{LC1} and V_{LC2}	1, 2	—
V_{LC1}–V_{LC2}	—	LCD power supply	3, 4	—
MELOUT	O	Melody output	64	—
V_{DD}	—	Main power supply	60	—
V_{SS}	—	Ground	41	—

Table 1. KS57C2202 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
RESET	I	Reset signal	45	—
X_{in}, X_{out}	—	Crystal oscillator signal for system clock 32.768 kHz	43, 42	—
TEST	I	Test signal input (must be connected to V_{SS})	44	—

Table 2. Supplemental KS57C2202 Pin Data

Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
P1.0–P1.1	INT0, INT1	I	Input	3
P3.0–P3.2	TCLO0, MELOUT, CLO	I/O	Input	5
P4.0–P4.3 P5.0–P5.3	—	I/O	Input	7
P6.0–P6.3	K0–K3	I/O	Input	6
P8.0–P8.7	SEG24–SEG31	O	Low	10
SEG0–SEG23	—	O	Low	8
COM0–COM3	—	O	Low	9
MELOUT	—	O	High	11
L_{CAP1}, L_{CAP2}	—	—	—	—
V_{LC1}, V_{LC2}	—	—	—	—
V_{DD}, V_{SS}	—	—	—	—
X_{in}, X_{out}	—	—	—	—
RESET	—	I	—	2
TEST	—	I	—	—