1 PRODUCT OVERVIEW

OVERVIEW

The KS57C2302/C2304 single-chip CMOS microcontroller has been designed for high performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

With features such as, LCD direct drive capability, 8-bit timer/counter, and watch timer, the KS57C2302/C2304 offers an excellent design solution for a wide variety of applications that require LCD functions.

Up to 16 pins of the 64-pin QFP package, it can be dedicated to I/O. Four vectored interrupts provide fast response to internal and external events. In addition, the KS57C2302/C2304 's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

OTP

The KS57C2302/C2304 microcontroller is also available in OTP (One Time Programmable) version, KS57P2304 . The KS57P2304 microcontroller has an on-chip 4-Kbyte one-time-programmable EPROM instead of masked ROM. The KS57P2304 is comparable to KS57C2302/C2304, both in function and in pin configuration.

FEATURES

Memory

— 288 × 4-bit RAM
— 2048 × 8-bit ROM (KS57C2302)
— 4096 × 8-bit ROM (KS57C2304)

I/O Pins

— Input only: 4 pins
— I/O: 12 pins
— Output: 8 pins sharing with segment driver outputs

LCD Controller/Driver

— Maximum 16-digit LCD direct drive capability
— 32 segment, 4 common pins
— Display modes: Static, 1/2 duty (1/2 bias)
1/3 duty (1/2 or 1/3 bias), 1/4 duty (1/3 bias)

8-Bit Basic Timer

— Programmable interval timer
— Watchdog timer

8-Bit Timer/Counter

— Programmable 8-bit timer
— External event counter
— Arbitrary clock frequency output

Watch Timer

— Real-time and interval time measurement
— Four frequency outputs to BUZ pin
— Clock source generation for LCD

Interrupts

— Two internal vectored interrupts
— Two external vectored interrupts
— Two quasi-interrupts

Memory-Mapped I/O Structure

— Data memory bank 15

Two Power-Down Modes

— Idle mode (only CPU clock stops)
— Stop mode (main or sub system oscillation stops)

Oscillation Sources

— Crystal, ceramic, or RC for main system clock
— Crystal or external oscillator for subsystem clock
— Main system clock frequency: 4.19 MHz (typical)
— Subsystem clock frequency: 32.768 kHz
— CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

— 0.95, 1.91, 15.3 µs at 4.19 MHz (main)
— 122 µs at 32.768 kHz (subsystem)

Operating Temperature

— – 40 °C to 85 °C

Operating Voltage Range

— 2.0 V to 5.5 V at 4.19 MHz
— 1.8 V to 5.5 V at 3 MHz

Package Type

— 64-pin QFP

BLOCK DIAGRAM

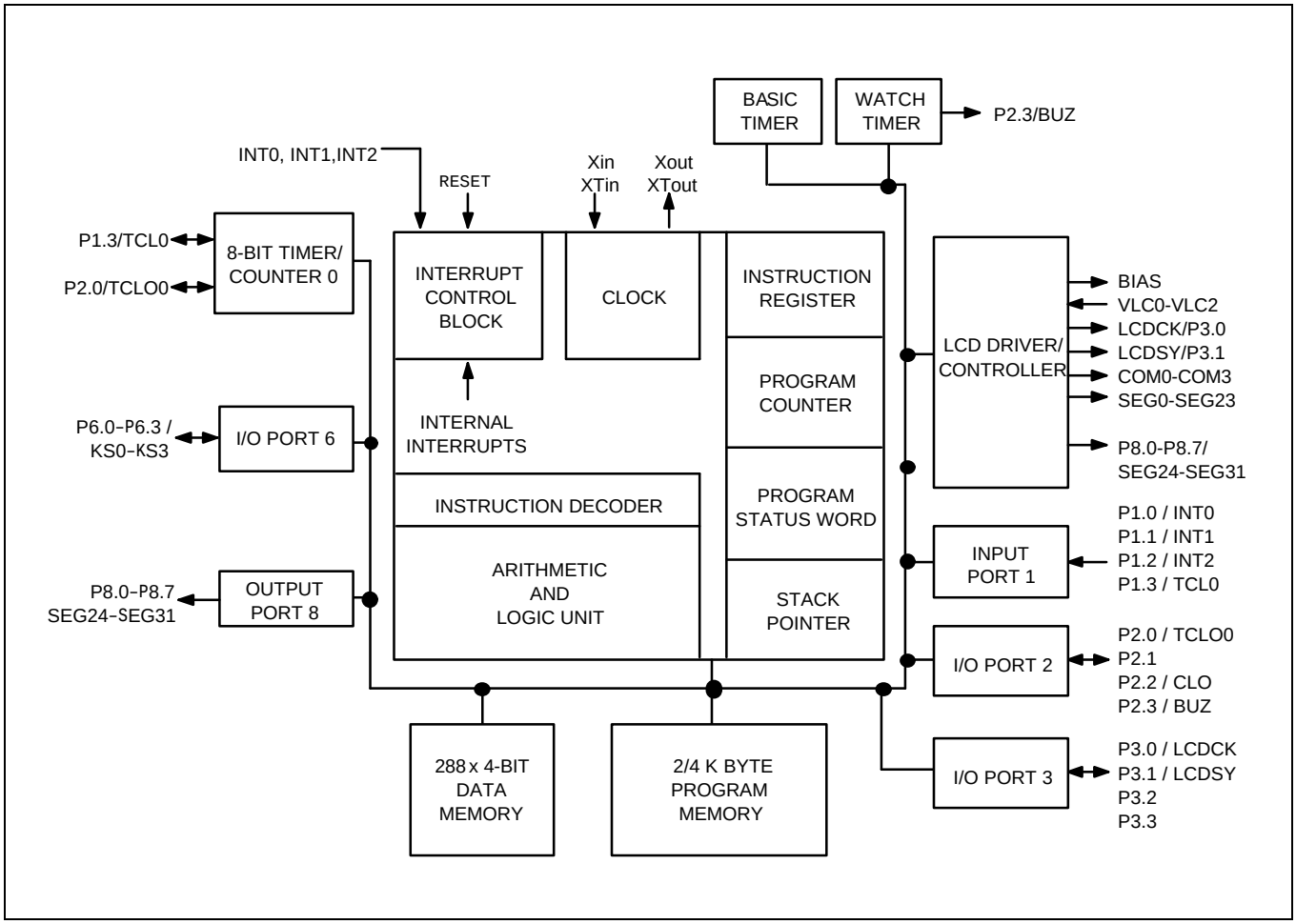

Figure 1-1. KS57C2302/C2304 Simplified Block Diagram

PIN ASSIGNMENTS

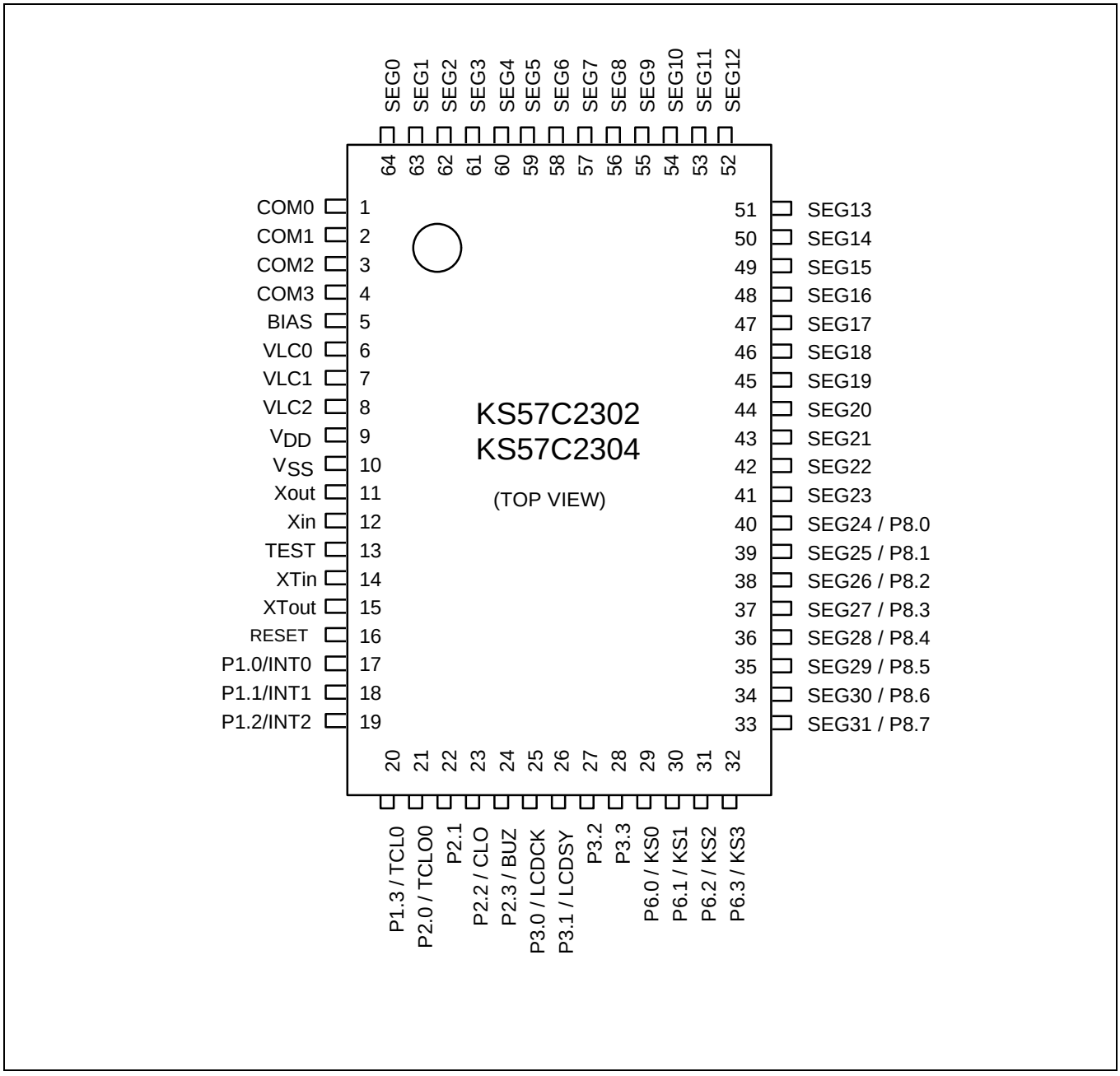

Figure 1-2. KS57C2302/C2304 64-QFP Pin Assignment

PIN DESCRIPTIONS

Table 1-1. KS57C2302/C2304 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin	Reset Value	Circuit Type
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit or 4-bit read and test is possible. 4-bit pull-up resistors are software assignable.	17 18 19 20	INT0 INT1 INT2 TCL0	Input	A-4
P2.0 P2.1 P2.2 P2.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. 4-bit pull-up resistors are software assignable.	21 22 23 24	TCLO0 – CLO BUZ	Input	D
P3.0 P3.1 P3.2 P3.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. Each individual pin can be specified as input or output. 4-bit pull-up resistors are software assignable.	25 26 27 28	LCDCK LCDSY	Input	D
P6.0–P6.3	I/O	4-bit I/O ports. Pins are individually software configurable as input or output. 1-bit and 4-bit read/write and test is possible. 4-bit pull-up resistors are software assignable.	29–32	KS0–KS3	Input	D
P8.0–P8.7	O	Output port for 1-bit data (for use as CMOS driver only)	40–33	SEG24–SEG31	Output	H-1
SEG0–SEG23	O	LCD segment signal output	64–41	–	Output	H
SEG24–SEG31	O	LCD segment signal output	40–33	P8.0–P8.7	Output	H-1
COM0–COM3	O	LCD common signal output	1–4	–	Output	H
V_{LC0}–V_{LC2}	–	LCD power supply. Built-in voltage dividing resistors	6–8	–	–	–
BIAS	–	LCD power control	5	–	–	–
LCDCK	I/O	LCD clock output for display expansion	25	P3.0	Input	D

Table 1-1. KS57P2304 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin	Reset Value	Circuit Type
LCDSY	I/O	LCD synchronization clock output for LCD display expansion	26	P3.1	Input	D
TCL0	I	External clock input for timer/counter 0	20	P1.3	Input	A-4
TCLO0	I/O	Timer/counter 0 clock output	21	P2.0	Input	D
INT0 INT1	I	External interrupt. The triggering edge for INT0 and INT1 is selectable. Only INT0 is synchronized with the system clock.	17 18	P1.0 P1.1	Input	A-4
INT2	I	Quasi-interrupt with detection of rising edge signals.	19	P1.2	Input	A-4
KS0–KS3	I/O	Quasi-interrupt input with falling edge detection.	29–32	P6.0–P6.3	Input	D
CLO	I/O	CPU clock output	23	P2.2	Input	D
BUZ	I/O	2, 4, 8 or 16 kHz frequency output for buzzer sound with 4.19 MHz main system clock or 32.768 kHz subsystem clock.	24	P2.3	Input	D
X_{IN}, X_{OUT}	–	Crystal, ceramic or RC oscillator pins for main system clock. (For external clock input, use X_{IN} and input X_{IN}' s reverse phase to X_{OUT})	12,11	–	–	–
XT_{IN}, XT_{OUT}	–	Crystal oscillator pins for subsystem clock. (For external clock input, use XT_{IN} and input XT_{IN}' s reverse phase to XT_{OUT})	14,15	–	–	–
V_{DD}	–	Main power supply	9	–	–	–
V_{SS}	–	Ground	10	–	–	–
RESET	–	Reset signal	16	–	Input	B
TEST	–	Test signal input (must be connected to V_{SS})	13	–	–	–

NOTE: Pull-up resistors for all I/O ports automatically disabled if they are configured to output mode.