KS8809 PLL Frequency Synthesizer for Pager

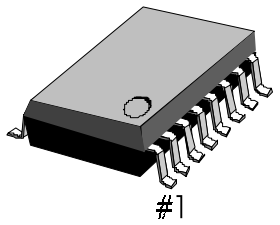
INTRODUCTION

KS8809 is a superior low-power-programmable PLL frequency synthesizer which can be used in high performance / Simple application for a Wide Area Pager system.

KS8809 consists of 2 kinds of divider block including a 19-bit Shift register, 16/18-bit Latch, 13/15 and 16/18-bit Counter, Prescaler, and a phase detector block including a Phase detector, Lock detector and a Charge pump.

KS8809 also has a battery saving mode which can control each register block by serial control data from the μ-controller (MICOM) and a Boost-up signal output for fast Locking .

16 - TSSOP



(Magnifications = 1 : 4)

ORDERING INFORMATION

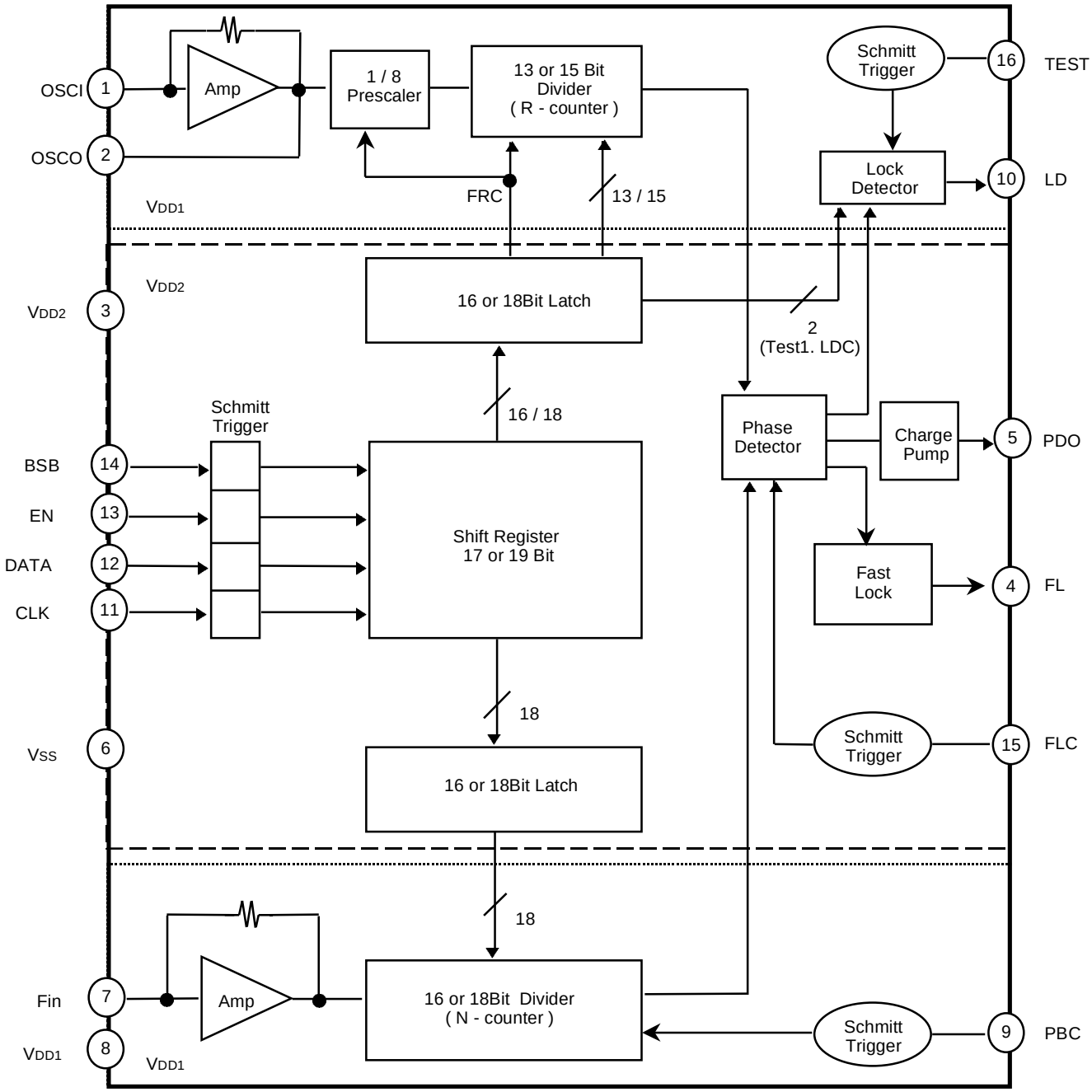
Device	Package	Operating Temperature
++ KS8809D	16 - TSSOP	- 25 ℃ ~ + 75℃

++ : Under development

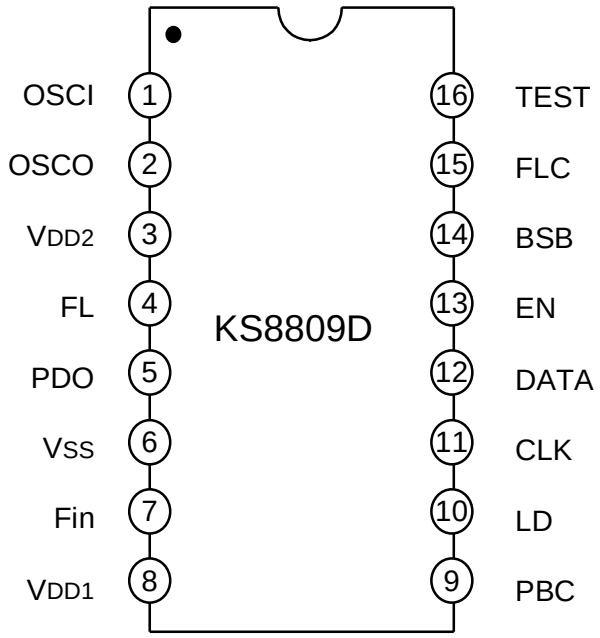
FEATURES

- Maximum operating frequency : 330 MHz @ 300mVp-p, V_{DD1}=1.0 V, V_{DD2}=3.0 V
- On-chip reference oscillator supports external crystal which oscillates up to 23 MHz.
- Superior supply current :
  - f_{IN} =310 MHz , I_{DD1} = 0.8 mA (Typ.) @ V_{DD1}=1.0 V, V_{DD2}=3.0 V
- Operating voltage : V_{DD1} = 0.95V ~ 1.5V and V_{DD2} = 2.0V ~ 3.3 V.
- Excellent Divider range
  - Ref. Divider : FRC (0) : 1/40 ~ 1/ 65528 (Multiple 8) : *Default*
    FRC (1) : 1/ 5 ~ 1/32767
  - Rx Divider : PBC (0) : 1/1056 ~ 1/ 65535 : *Default*
    PBC (1) : 1/1056 ~ 1/262143
- Boost-up signal output for Fast Locking
- In the Standby mode, V_{DD1} block can be controlled by BS Pin status
  - Standby current consumption : 10μA (Max.)
- Programmable control the output of LD to reduce internal noise
- Programmable 17/19-bit Shift Register value to reduce current consumption
- Phase Detector Output circuit for Passive filter
- Package type : 16 - TSSOP (0.65 mm)

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Symbol	Description
1	OSCI	These input / output pins generate the reference frequency. In case of OSCI Pin, external reference frequency can be input through the AC coupling.
2	OSCO	
3	VDD2	The highest potential supply terminal that can be supplied up to 2.0 V ~ 3.3 V.
4	FL	Booster signal output for fast Locking
5	PDO	The Output of RX Phase detector terminal for passive loop filter . There are 3 - kinds of output signal states according to Rx Loop Error.
6	Vss	Ground terminal

PIN DESCRIPTION (*Continued*)

Pin No.	Symbol	Description
7	Fin	Input terminal for 16 or 18-bit N - Divider from VCO. VCO Frequency can be input through AC coupling
8	V_{DD1}	Voltage supply terminal for Oscillator and Fin block. This pin can be supplied up to 0.95 ~ 1.5 V from Vss.
9	PBC	This is an input for Programmable Bit Control which has Schimitt Trigger architecture , Pull-up. High = 16 Bits N - Divider (Default : ND0 ~ ND15) Low = 18 Bits N - Divider (ND0 ~ ND17) cf) R-divider Bits will be changed by the FRC bit of Program
10	LD	The output of Phase Detector can be controlled by R - counter register When the LDC bit of R - counter set to Low, the output will be disabled to reduce a noise problem, but if it is set to High, the output will be enabled to show an lock / unlock status that is the error width between the Ref. signal and the VCO output signal.
11	CLK	These pins are controlled by the µ-controller which has Schmitt Trigger architecture , Pull-down The features of these pins are as follows ; Clock input for 17 or 19-bit Shift Register, Serial data input (it include TEST1, FRC and LDC), and Latch enable input .
12	DATA	
13	EN	
14	BSB	In the BS mode (set to Low) , the V_{DD1} block will be powered off, but the internal latch data is still valid because the V_{DD2} is supplied continuously. This input has Schmitt Trigger architecture.
15	FLC	This is the input pin for Fast Locking Control (FLC) which has Schmitt Trigger architecture , Pull-down. Low = The Current of PDO Charge pump output is Normal (Default : x1) High = The Current of PDO Charge pump output is Double (x 2)
16	TEST	This is the input pin for TEST which has Schmitt Trigger architecture , Pull-down. Low = All block wil be operated as normal state (Default) High = LD and FL state will be TEST mode

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply voltage	V_{DD1}~V_{DD2}	- 0.3 ~ 4.0	V
Input voltage	V_I	V_{SS} - 0.3 ~ V_{DD} + 0.3	V
Power dissipation	P_D	350	mW
Operating temperature	T_{OPR}	- 25 ~ 75	℃
Storage temperature	T_{STG}	- 40 ~ 125	℃

ELECTRICAL CHARACTERISTICS

(Ta = 25℃ , V_{DD1}= 1.0 V , V_{DD2}=3.0 V , unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating voltage	V_{DD1}	-	0.95	1.0	1.5	V
	V_{DD2}	-	2.0	3.0	3.3	
Operating current	I_{DD}	F_{OSCI} = 12.8 MHz F_{FIN} =310 MHz @ 0.3V_{P-P} V_{DD1} =1.0 V, V_{DD2}=3.0 V, BSB=High	-	0.8	-	mA
Standby current	I_{SB1}	V_{DD1}=0.0 V , V_{DD2}=3.0 V, BSB=Low	-	0.01	10	㎂
Input voltage (DATA,CLK,EN,BS)	V_{IL}	-	-	-	0.3	V
	V_{IH}	-	V_{DD2}-0.3	-	-	
Input voltage (TEST , PBC)	V_{IL}	-	-	-	0.2	V
	V_{IH}	-	V_{DD2}-0.2	-	-	
Input Current (Fin,Xin)	I_{IH}	V_{IH}=V_{DD1}, BSB = High	-	-	20	㎂
	I_{IL}	V_{IL}=0 V, BSB = High	-	-	20	
Input frequency	F_{FIN}	V_{FIN} = 0.3Vp-p, V_{DD1} = 1.0V	40	-	330	MHz
	F_{OSCI}	V_{OSCI} = 0.3Vp-p, V_{DD1} = 1.0V	7	12.8	23	
Output Current (PDO, FL)	I_{OH1}	V_{OH} = 0.4 V	1.0	-	-	mA
	I_{OL1}	V_{OL} = V_{DD2} - 0.4 V	1.0	-	-	
Output current (LD)	I_{OH2}	V_{OH} = 0.4 V	0.1	-	-	mA
	I_{OL2}	V_{OL} = V_{DD2} - 0.4 V	0.1		-	
Setup-Time (DATA-CLK,CLK-EN)	t_s	-	2	-	-	uS
Hold Time	t_H	-	2	-	-	uS

▶ Program Scheme (μ-controller)

- **N - Counter Register (19 bits)**

Bit	Bit 18 (ND 17) ~ Bit 1 (ND 0)	Bit 0 (LSB)
Name	ND	PMC
Description	N-Counter Data (ND 17 ~ ND 0)	Program Mode Control
Function	18 Bit Program Data • PBC = 1 : 16 bits (ND15 ~ ND0) will be valid • PBC = 0 : 18 bits (ND17 ~ ND0) will be valid	0 : N-Counter Program 1 : Ref. R-Counter Program

- **R - Counter Register (19 bits)**

Bit	Bit 18 ~ Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Name	RD	LDC	FRC	TEST1	PMC
Description	Ref. R-Counter Data (RD 14 ~ RD 0)	Lock Detector Control	Frequency of Reference Control	TEST Mode Control	Program Mode Control
Function	15 Bit Programmable Ref. R-Counter • FRC = 0 : 13 bits (RD12~ RD0) •FRC = 1 : 15 bits (RD14~ RD0)	0 : Disable LD out 1 : Enable LD out	0 : R_CNT div. = 8 x RD 1 : R_CNT div. = RD(15bit)	Mainly for the product Test	0 :ND Program 1 :RD Program

※ CONTROL MODE ※

LDC	LDC Pin State	Description
0	Low	LDC function is independent of the other Control Bit
1	Normal Operation	

FRC	R - Counter Value	Description
0	8 x R_cnt value (OSCI / 8 x R) , Use 13 bits R- Counter	FRC function is independent of the other Control Bit
1	R_cnt value (OSCI / R) , Use 15 bits R- Counter	

- **Rx. N - Counter Register Programming Timing (PMC=0 → 16 / 18-Bit N_Counter)**

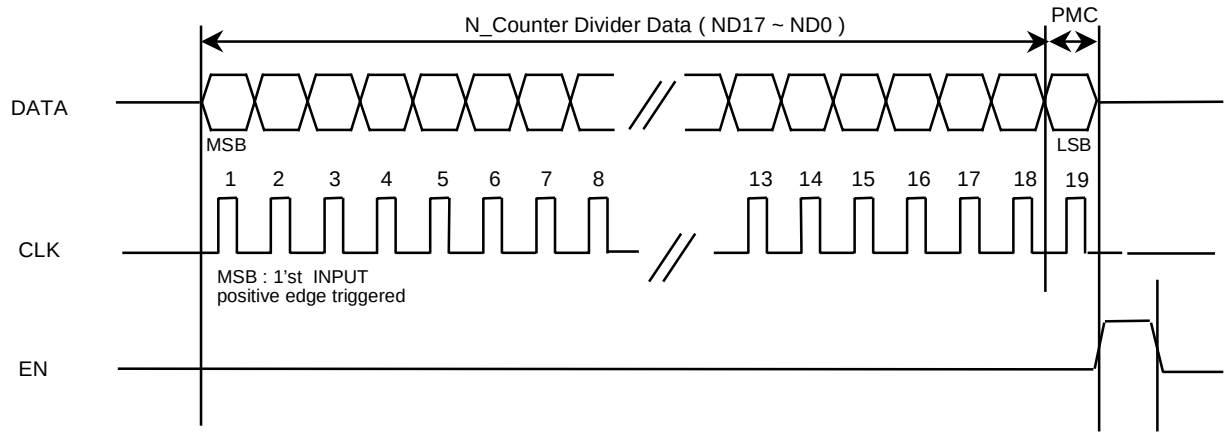


Figure 1

- **Ref. R - Counter Register Programming Timing (PMC= 1 → 13 / 15 Bit R_Counter, LDC , FRC , TEST1)**

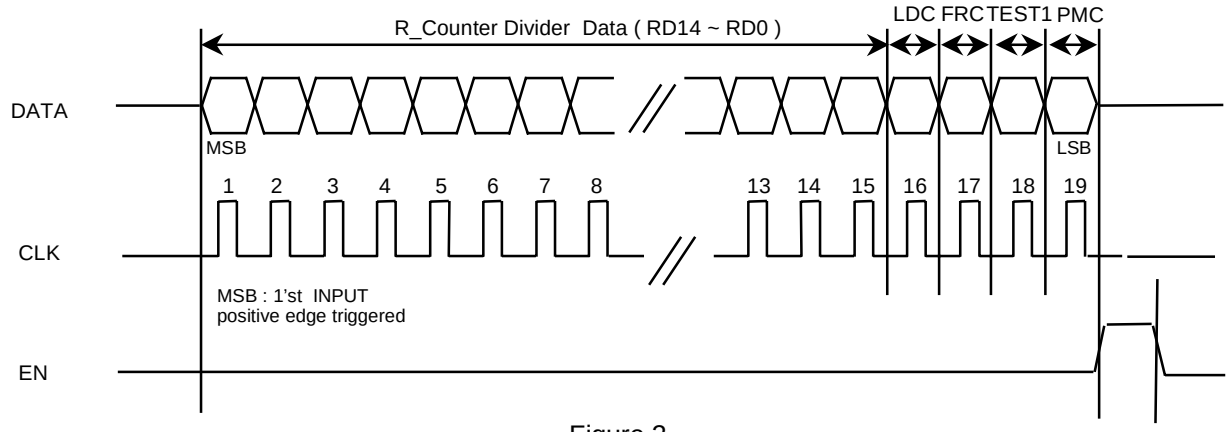


Figure 2

- **Serial DATA Input Timing**

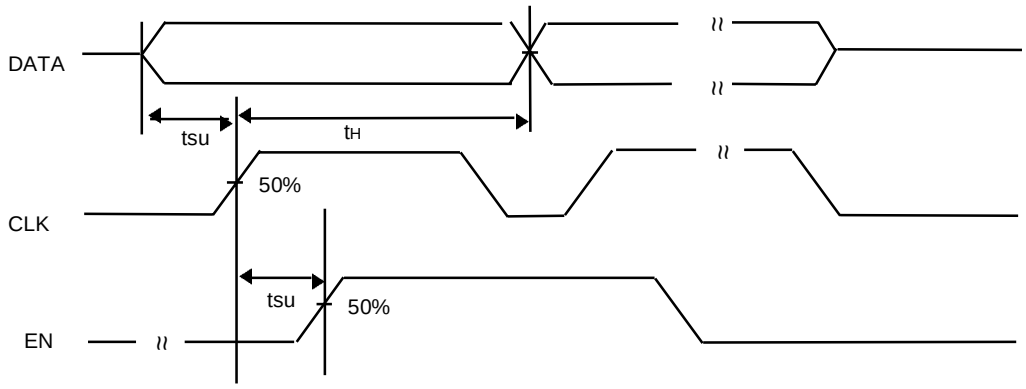


Figure 3.

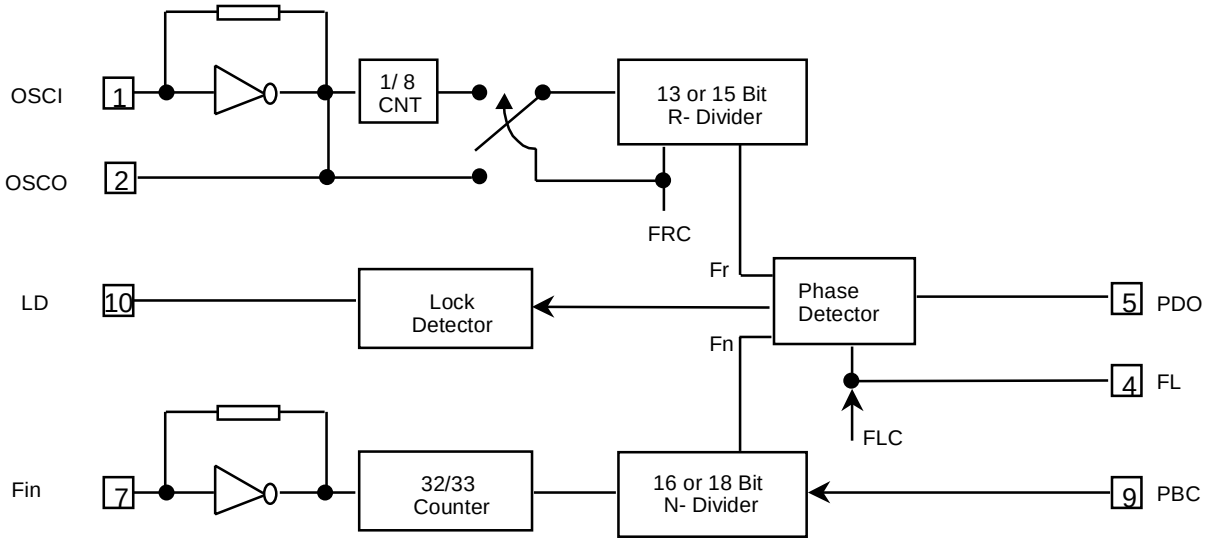


Figure 4-1. Phase Detector / Lock Detector / Fast Lock Block Diagram

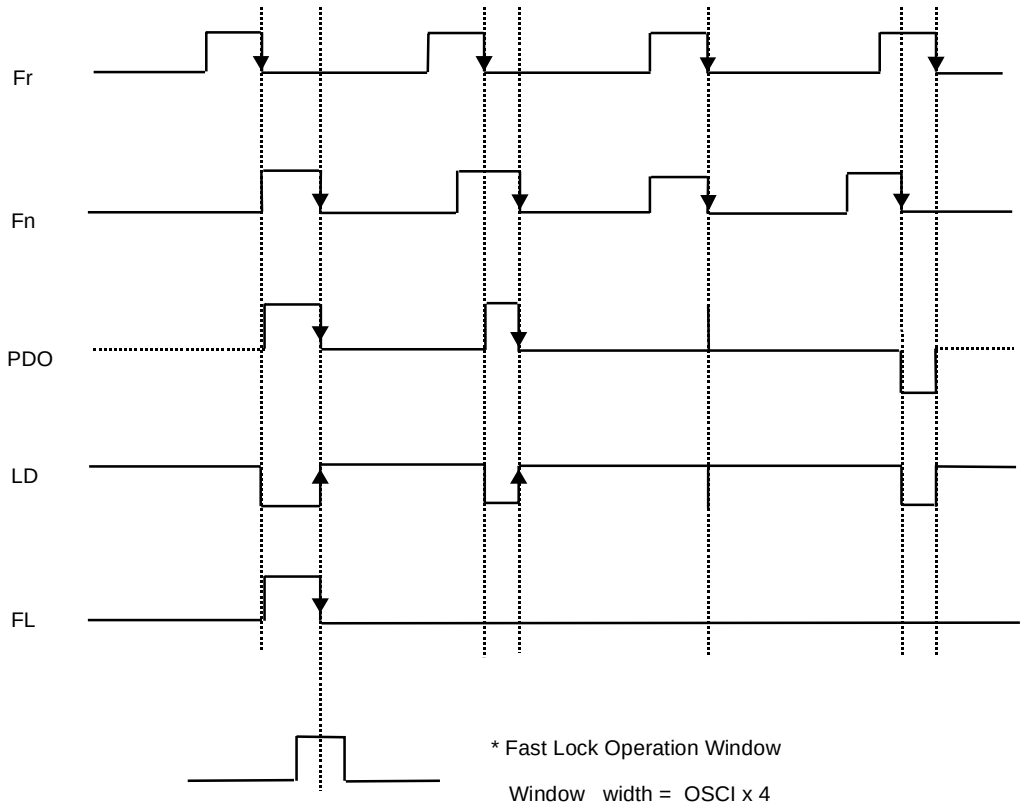


Figure 4-2. Phase Detector / Lock Detector / Fast Lock Output Waveforms

▶ PACKAGE DIMENSIONS

Dimensions in Milimeters

16 - TSSOP