SAMSUNG ELECTRONICS

KS88C0116
8-Bit CMOS Microcontroller

Product Specification

OVERVIEW

The KS88C0116 single-chip 8-bit microcontroller is fabricated using a highly advanced CMOS process. Its fast and reliable CPU is based on Zilog's Super8® architecture. With two 8-bit and two 16-bit timer/counters, a large number of general I/O pins, full-duplex serial port, and 16-bit backup timer, the KS88C0116 is an excellent choice for a wide range of general-purpose electronics applications.

FEATURES

CPU

- SAM8 CPU core

Memory

- 272-byte general purpose register area
- 16-Kbyte internal program memory
- ROM-less operating mode

External Interface

- 64-Kbyte external data memory area
- 64-Kbyte external program memory area (ROM-less mode)

Instruction Set

- 79 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 600 ns at 20 MHz f_{OSC} (min.)

Interrupts

- 18 interrupt sources
- 18 interrupt vectors
- Eight interrupt levels
- Fast interrupt processing

General I/O

- Seven I/O ports (54 pins):
- Three nibble-programmable ports
- One bit-programmable port
- Two bit-programmable ports for external interrupts
- One n-channel, open-drain output port

Timer/Counters

- Two 8-bit timers with interval timer and PWM modes
- Two 16-bit general-purpose timer/counters

Backup Timer

- 16-bit backup timer

Serial Port

- One synchronous operating mode and three full-duplex asynchronous UART modes

Operating Temperature Range

- – 20°C to + 85°C

Operating Voltage Range

- 4.5 V to 5.5 V

Package Types

- 64-pin SDIP, 64-pin QFP

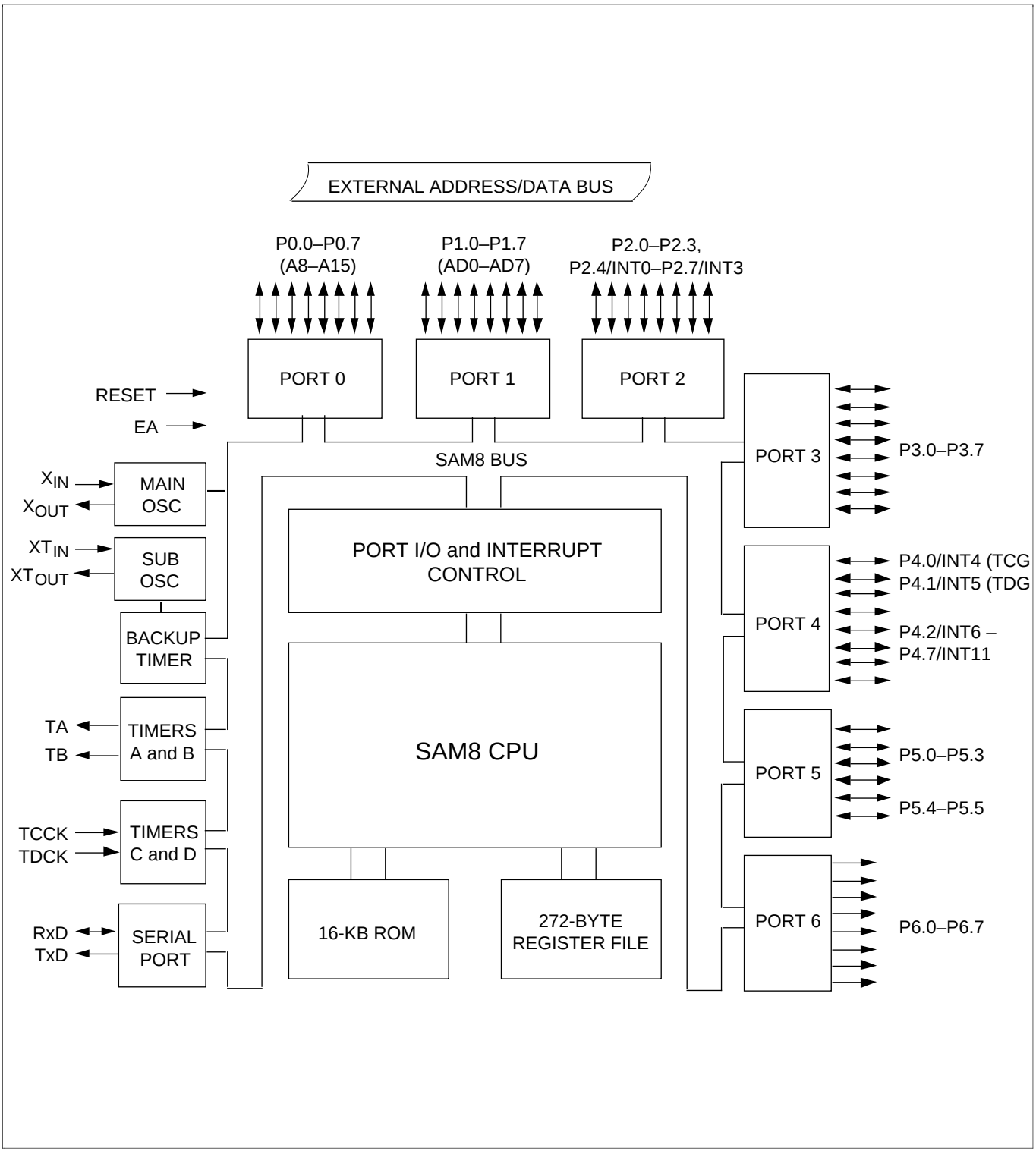

Figure 1. KS88C0116 Block Diagram

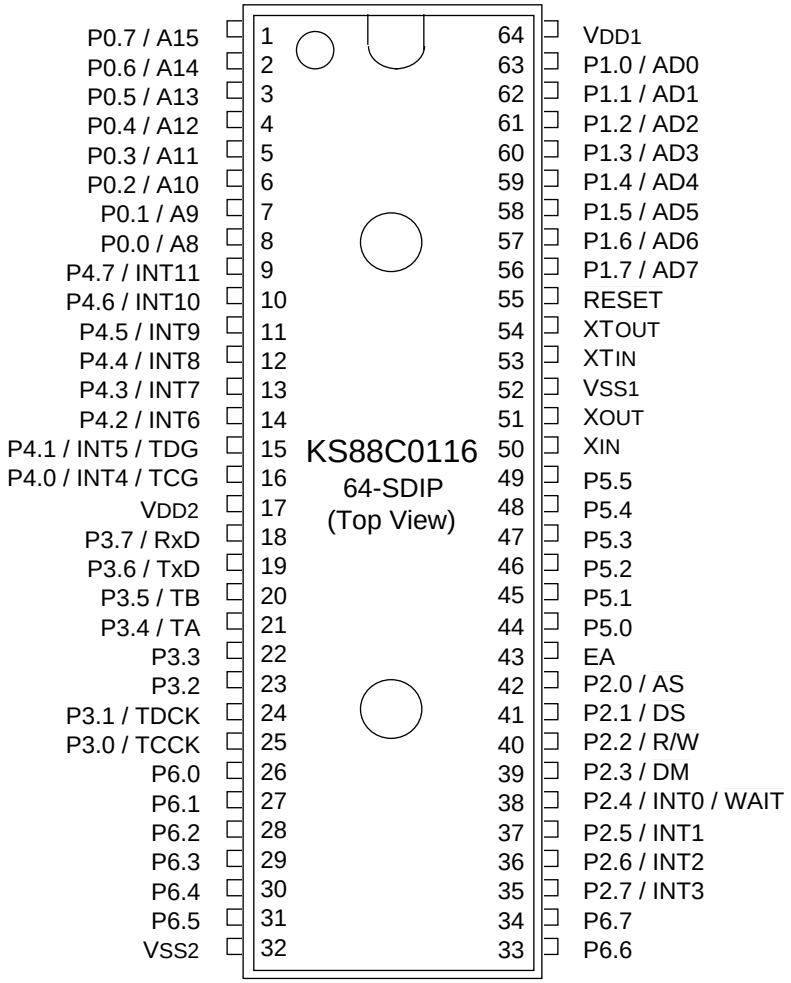

Figure 2. KS88C0116 Pin Assignments (64-SDIP)

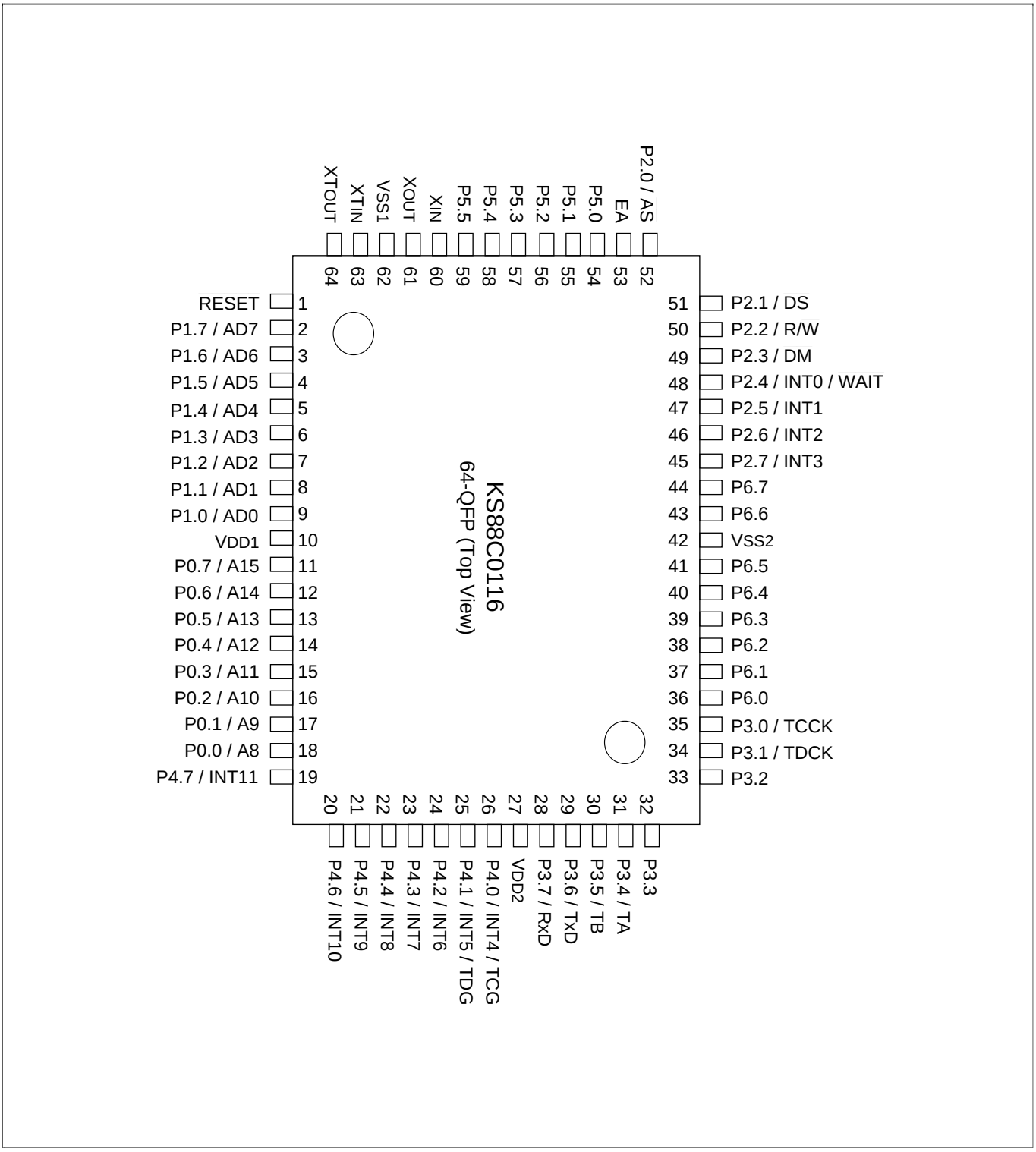

Figure 3. KS88C0116 Pin Assignments (64-QFP)

Table 1. KS88C0116 Pin Descriptions

Pin Name	Pin Type	Pin Description	Circuit Number	SDIP Pin Number	Share Pins
P0.0–P0.7	I/O	I/O port with nibble-programmable pins; Schmitt trigger input or push-pull, open-drain output and software assignable pull-ups; also configurable as external interface address lines A8–A15.	1	8–1	A8–A15
P1.0–P1.7	I/O	Same general characteristics as port 0; also configurable as external interface address/data lines AD0–AD7.	1	63–56	AD0–AD7
P2.0–P2.3 P2.4–P2.7	I/O	I/O port with Schmitt trigger input (P2.0–P2.3 only) or push-pull output. Lower nibble pins 0–3 are configurable for external interface signals; upper nibble pins 4–7 are bit-programmable for external interrupts INT0–INT3. P2.4 can also be used for external WAIT input.	2 (lower nibble); 3 (upper nibble; with noise filter)	42–39; 38–35	AS, DS, DM, R/W; INT0–INT3, WAIT
P3.0–P3.7	I/O	I/O port with bit-programmable pins; Schmitt trigger input or push-pull output. Alternate functions include software-selectable UART transmit and receive on pins 3.7 and 3.6, timer B and timer A outputs at pins 3.5 and 3.4, and timer D and C clock inputs at pins 3.1 and 3.0.	4	25–18	TCCK, TDCK, TA, TB, TxD, RxD
P4.0–P4.7	I/O	I/O port with bit-programmable pins; Schmitt trigger input or push-pull output; software-assignable pull-ups. Alternate functions include external interrupt inputs INT4–INT11 (with interrupt enable and pending control) and timer C and D gate input at P4.0 and P4.1.	5 (with noise filter)	16–9	INT4–INT11; TCG, TDG
P5.0–P5.5	I/O	I/O port with nibble-programmable pins; Schmitt trigger input or push-pull, open-drain output; software-assignable pull-ups.	1	44–49	–
P6.0–P6.7	O	N-channel, open-drain output pins; up to 9-volt capacity	6	26–31, 33–34	–
RxD	I/O	Bi-directional serial data input pin	–	18	P3.7
TxD	I/O	Serial data output pin	–	19	P3.6
TA, TB	I/O	Timer A and B output pins	4	21, 20	P3.4, P3.5
TCCK, TDCK	I/O	Timer C and D external clock input pins	4	25, 24	P3.0, P3.1
INT0–INT3	I/O	External interrupts. I/O pin 2.4 (share pin with INT0) is also configurable as a WAIT signal input pin for the external interface.	3 (with noise filter)	38–35	P2.4–P2.7

Table 1. KS88C0116 Pin Descriptions (Continued)

Pin Name	Pin Type	Pin Description	Circuit Number	SDIP Pin Number	Share Pins
INT4–INT11	I/O	Bit-programmable external interrupt input pins with interrupt pending and enable /disable control	5 (with noise filter)	16–9	P4.0–P4.7
X_{IN}, X_{OUT}	–	System clock input and output pins	–	50, 51	–
XT_{IN}, XT_{OUT}	–	Suboscillator clock pins for backup timer	–	53, 54	–
RESET	I	System reset pin (internal pull-up: 280 kΩ)	7	55	–
EA	I	External access (EA) pin with three modes: 0 V: Normal operation (internal ROM) 5 V: ROM-less operation (external interface)	–	43	–
V_{DD2}, V_{SS2}	–	Power input pins for port output (external)	–	17, 32	–
V_{DD1}, V_{SS1}	–	Power input pins for CPU (internal)	–	64, 52	–

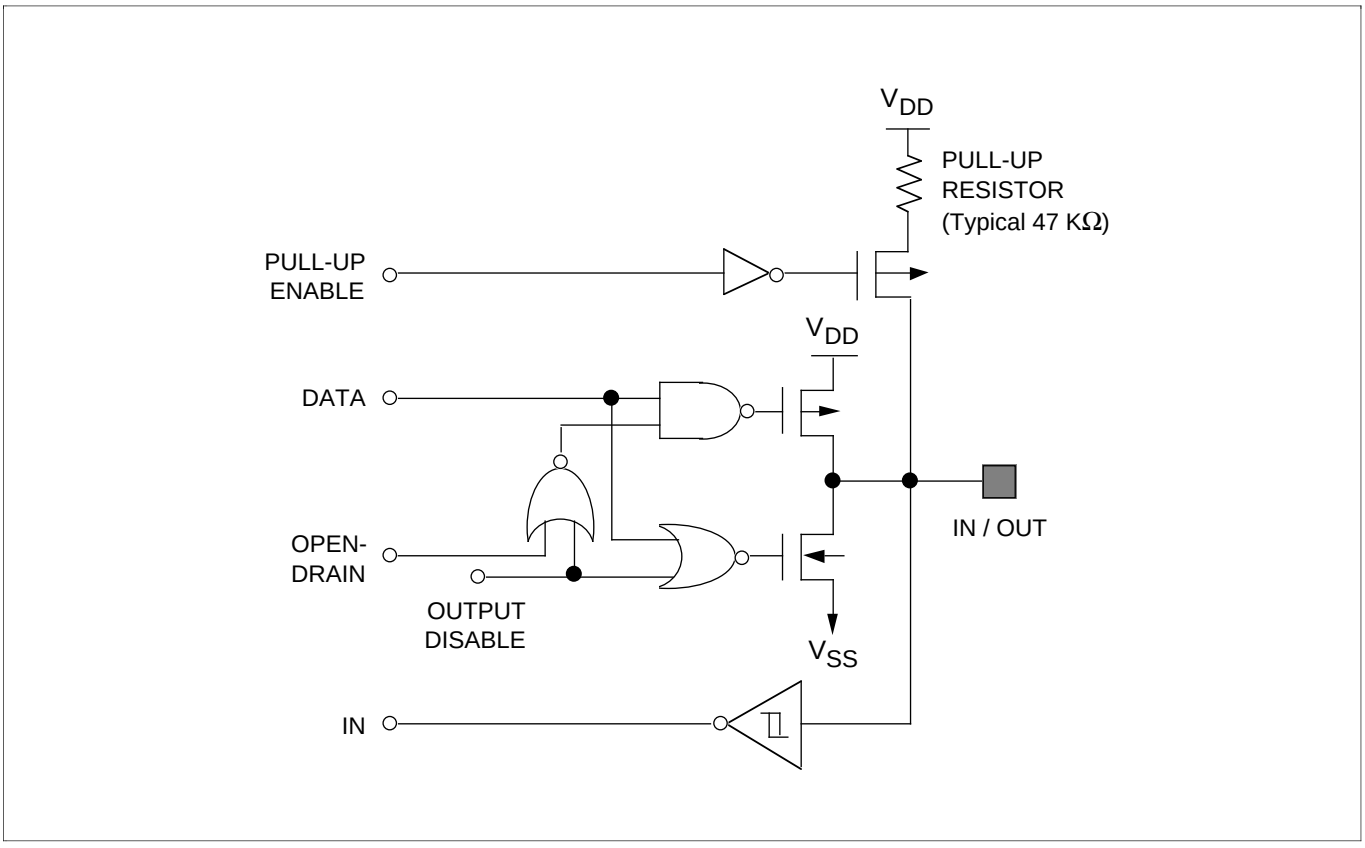

Figure 4. Pin Circuit Type 1 (Ports 0, 1, and 5)