1 PRODUCT OVERVIEW

KS88-SERIES MICROCONTROLLERS

Samsung s KS88 series of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Important CPU features include:

— Efficient register-oriented architecture

— Selectable CPU clock sources

— Idle and Stop power-down mode release by interrupt

— Built-in basic timer with watchdog function

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum six CPU clocks) can be assigned to specific interrupt levels.

KS88C2064 MICROCONTROLLER

The KS88C2064 single-chip CMOS microcontroller is fabricated using a highly advanced CMOS process and is based on Samsung s newest CPU architecture.

The KS88C2064 is the microcontroller which has 64-Kbyte mask-programmable ROM and 192-Kbyte mask ROM for font data.

Using a proven modular design approach, Samsung engineers developed the KS88C2064 by integrating the following peripheral modules with the powerful SAM87 core:

— Four programmable I/O ports, excluding one BUZ pin, for a total of 32 pins.

— Eight bit-programmable pins for external interrupts.

— One 8-bit basic timer for oscillation stabilization and watchdog functions (system reset).

One 8-bit timer/counter and one 16-bit timer/counter with selectable operating modes.

— Watch timer for real time.

The KS88C2064 is a versatile microcontroller for data bank or dictionary. It is currently available in a 128-pin QFP package.

FEATURES

CPU

- SAM87 CPU core

Memory

- 64-Kbyte internal program memory (ROM)
- 192-Kbyte internal memory (ROM) for font data
- 272-byte internal register file (Excluding LCD RAM)
- 6144-byte data RAM

Instruction Set

- 78 instructions

  IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 1.5 μs at 4 MHz fx (minimum)
- 183 μs at 32,768 Hz fxt

Interrupts

- Five interrupt levels and 15 interrupt sources
- 15 vectors (15 sources have a dedicated vector address)
- Fast interrupt processing feature (for one selected interrupt level)

I/O Ports

- Four 8-bit I/O ports (P0 P3) for a total of 32-bit programmable pins

  Eight input pins for external interrupts

  One output only pin for BUZ

Watch Timer

- Interval time: 3.91 ms, 1s at 32,768 Hz
- Four frequency outputs to BUZ pin and BUZ pin
- Clock source generation for LCD

LCD Controller/Driver

- 65 segments and 18 common terminals
- Internal resistor circuit for LCD bias
- Voltage doubler
- All dot can be switched on/off

Timers and Timer/Counters

- One programmable 8-bit basic timer (BT) for oscillation stabilization control or watchdog timer (software reset) function
- One 8-bit timer/counter (Timer 0) with three operating modes; Interval, Capture and PWM

  One 16-bit timer/counter (Timer 1) with two 8-bit timer/counter modes; Interval

Power-Down Modes

- Idle mode (CPU clock stops)
- Stop mode (main oscillation and CPU clock stops)

Operating Temperature Range

- – 40°C to + 85°C

Operating Voltage Range

- 2.2 V to 3.4 V
- 2.7 V to 3.4 V at 4 MHz fx

Package Type

- 128-pin QFP

BLOCK DIAGRAM

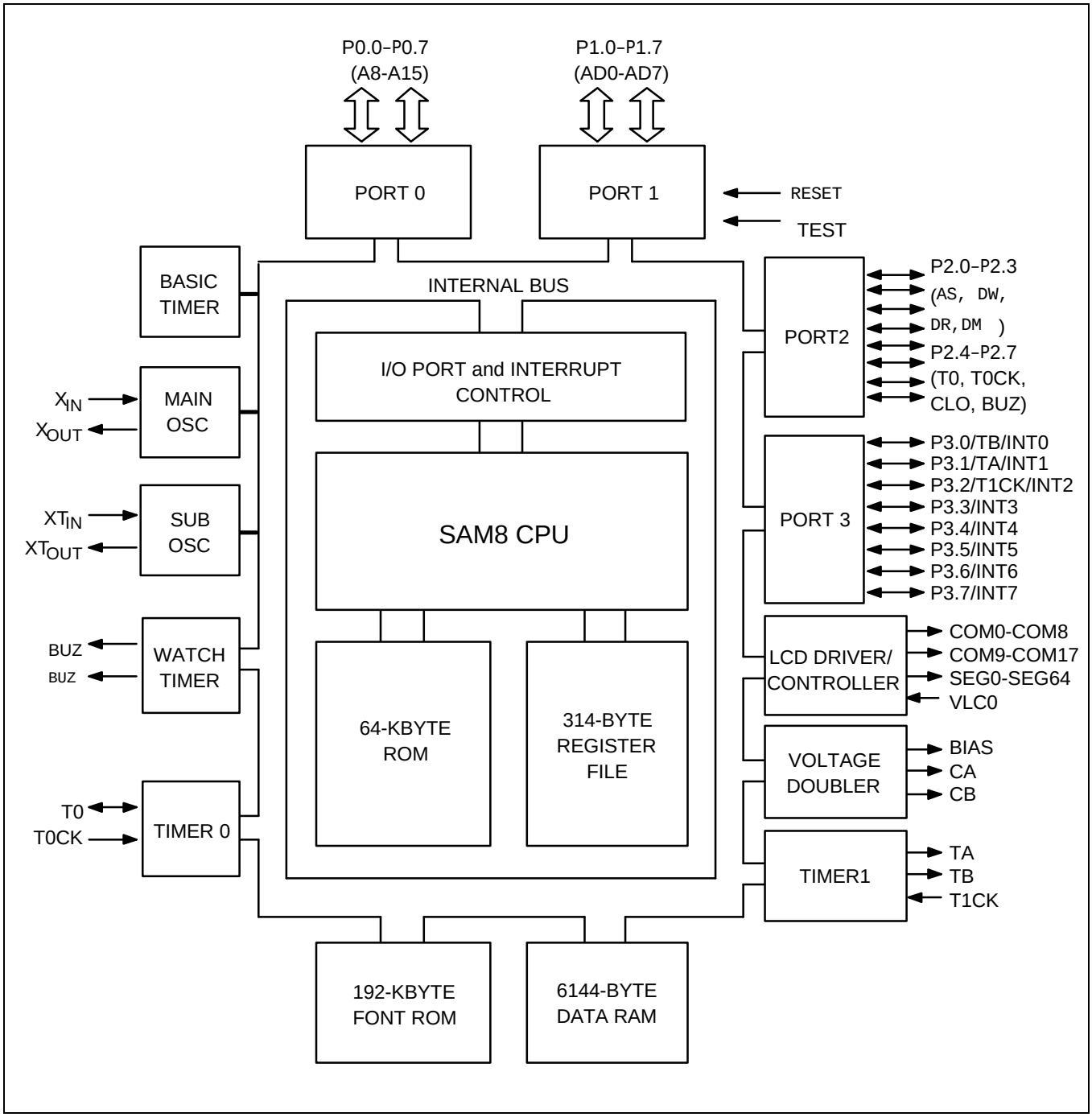

Figure 1-1. Block Diagram

PIN ASSIGNMENTS

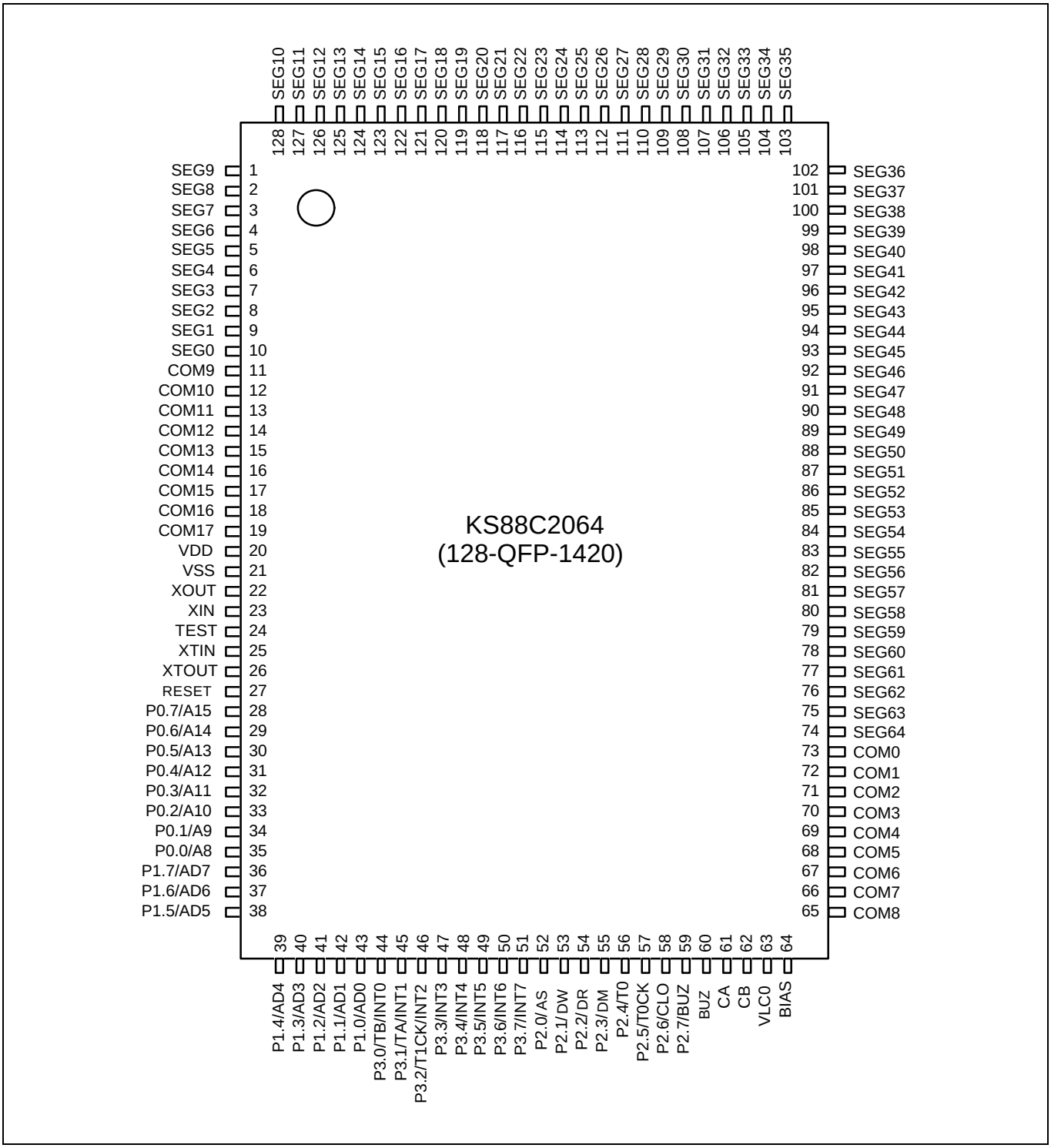

Figure 1-2. Pin Assignment (128-Pin QFP Package)

SAMSUNG ELECTRONICS

PIN DESCRIPTIONS

Table 1-1. Pin Descriptions

Pin Names	Pin Type	Pin Description	Circuit Type	Pin No.	Shared Functions
P0.0-P0.7	I/O	I/O port with nibble-programmable pins; schmitt trigger input or push-pull, open-drain output and software assignable pull-up; also configurable as external interface address lines A8-A15.	3	35-28	A8-A15
P1.0-P1.7	I/O	Same general characteristics as port 0; also configurable as external interface address/data lines AD0-AD7.	3	43-36	AD0-AD7
P2.0-P2.3	I/O	I/O port with bit-programmable pins; schmitt trigger input or push-pull output and software assignable pull-ups. Lower nibble pins 0 3 are configurable for external interface signals.	5	52-55	AS, DW, DR, DM
P2.4-P2.7	I/O	P2.4/Capture input, interval/PWM output (T0) P2.5/timer 0 clock input (T0CK) P2.6/system clock output (CLO) P2.7/buzzer signal output (BUZ)	6	56-59	T0, T0CK, CLO, BUZ
P3.0-P3.7	I/O	I/O port with bit-programmable pins; schmitt trigger input or push-pull output and software assignable pull-up; P3.0 P3.7 are alternately used for external interrupt input (noise filters, interrupt enable and pending control); P3.0/timer B clock output (TB)/INT0 P3.1/timer 1/A clock output (TA)/INT1 P3.2/timer 1/A clock input (T1CK)/INT2	4	44-51	TB/INT0, TA/INT1, T1CK/INT2, INT3 INT7
T1CK	I/O	Timer A external clock input pins.	4	46	P3.2/INT2
TB TA	I/O	Timer B and 1/A clock output pins.	4	44 45	P3.0/INT0 P3.1/INT1
AS, DW, DR, DM	I/O	Output pins for external interface control signals. AS: address strobe DW: data memory write DR: data memory read DM: data memory select	5	52 55	P2.0 P2.3
T0	I/O	Capture input or interval/PWM output.	6	56	P2.4
T0CK	I/O	Timer 0 clock input.	6	57	P2.5

Table 1-1. Pin Descriptions (Continued)

Pin Names	Pin Type	Pin Description	Circuit Type	Pin No.	Shared Functions
CLO	I/O	Clock output	6	58	P2.6
BUZ	I/O	Output pin for buzzer signal.	6	59	P2.7
$\overline{BUZ}$	O	Inverted buzzer signal output.	-	60	-
INT0-INT7	I/O	External interrupt input pins.	4	44 51	P3.0/TB, P3.1/TA, P3.2/T1CK, P3.3-P3.7
AD0-AD7	I/O	Address low and data ports.	3	43-36	P1.0-P1.7
A8-A15	I/O	Address high output ports.	3	35-28	P0.0-P0.7
COM0-COM8	O	LCD common signal output.	7	73-65	-
COM9-COM17	O	LCD common signal output.	7	11-19	-
SEG0-SEG64	O	LCD seg signal output.	8	10-1 128-74	-
CA, CB		Capacitor terminal for voltage doubling.	-	61, 62	-
VLC0		LCD power supply.	-	63	-
BIAS	O	Bias voltage level for LCD driving.	-	64	-
$\overline{RESET}$	I	System reset pin	2	27	-
XT_{IN}, XT_{OUT}		Crystal oscillator pins for sub clock.	-	25, 26	-
TEST	I	Test signal input (must be connected to V_{SS}).	-	24	-
X_{IN}, X_{OUT}		Main oscillator pins	-	23, 22	-
V_{DD}, V_{SS}		Power input pins	-	20, 21	-