1 PRODUCT OVERVIEW

KS88-SERIES MICROCONTROLLERS

Samsung's KS88 series of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Among the major CPU features are:

— Efficient register-oriented architecture

— Selectable CPU clock sources

— Idle and Stop power-down mode release by interrupt

— Built-in basic timer with watchdog function

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum of six CPU clocks) can be assigned to specific interrupt levels.

KS88C2148/P2148 MICROCONTROLLER

The KS88C2148/P2148 single-chip CMOS microcontroller is fabricated using the highly advanced CMOS process, based on Samsung' s newest CPU architecture.

The KS88C2148 is a microcontroller with a 48-Kbyte mask-programmable ROM embedded.

The KS88P2148 is a microcontroller with a 48-Kbyte one-time-programmable ROM embedded.

Using a proven modular design approach, Samsung engineers have successfully developed the KS88C2148/P2148 by integrating the following peripheral modules with the powerful SAM8 core:

— Six programmable I/O ports, including five 8-bit ports and one 7-bit port, for a total of 47 pins.

— Twelve bit-programmable pins for external interrupts.

— One 8-bit basic timer for oscillation stabilization and watchdog functions (system reset).

— One 8-bit timer/counter and one 16-bit timer/counter with selectable operating modes.

— Watch timer for real time.

— 4-input A/D converter

— Serial I/O interface

The KS88C2148/P2148 is versatile microcontroller for cordless phone, pager, etc. They are currently available in 80-pin TQFP and 80-pin QFP package.

OTP

The KS88P2148 is an OTP (One Time Programmable) version of the KS88C2148 microcontroller. The KS88P2148 microcontroller has an on-chip 48-Kbyte one-time-programmable EPROM instead of a masked ROM. The KS88P2148 is comparable to the KS88C2148, both in function and in pin configuration.

FEATURES

CPU

- SAM8 CPU core

Memory

- Data memory: 1040-byte of internal register file (Excluding LCD RAM)
- Program memory: 48-Kbyte internal program memory (ROM)

External Interface

- 64-Kbyte external data memory area

Instruction Execution Time

- 750 ns at 8 MHz (minimum, Main oscillator)
- 183 μs at 32,768 Hz (minimum, Sub oscillator)

Interrupts

- 7 interrupt levels and 19 interrupt sources
- 19 vectors
- Fast interrupt processing feature (for one selected interrupt level)

I/O Ports

- Five 8-bit I/O ports (P0–P4) and one 7-bit I/O port for a total of 47 bit-programmable pins

8-Bit Basic Timer

- One programmable 8-bit basic timer (BT) for oscillation stabilization control or watchdog timer (software reset) function

Watch Timer

- Time internal generation: 3.91 ms, 0.5 s at 32,768 Hz
- Four frequency outputs to BUZ pin
- Clock source generation for LCD

Timers and Timer/Counters

- One 8-bit timer/counter (Timer 0) with three operating modes: Interval, Capture, and PWM
- One 16-bit timer/counter (Timer 1) with two 8-bit timer/counter modes

LCD Controller/Driver

- UP to 32 segment pins
- 3, 4, and 8 common selectable
- Choice of duty cycle
- All dots can be switched on/off
- Internal resistor circuit for LCD bias

Serial Port

- One synchronous SIO

A/D Converter

- 8-bit conversion resolution × 4 channel
- 34 μs conversion time(4 MHz CPU clock, fxx/4)

Oscillation Sources

- Crystal, ceramic, or RC for main system clock
- Crystal or external oscillator for subsystem clock
- Main system clock frequency: 8 MHz
- Subsystem clock frequency: 32.768 kHz

Power-Down Modes

- Main Idle mode (only CPU clock stops)
- Sub idle mode
- Stop mode (main/sub system oscillation stops)

Operating Temperature Range

- – 40°C to + 85°C

Operating Voltage Range

- 2.0 V to 5.5 V at 32 kHz (sub clock)–6 MHz (main clock)
- 2.2 V to 5.5 V at 8 MHz

Package Type

- 80-pin TQFP, 80-pin QFP

BLOCK DIAGRAM

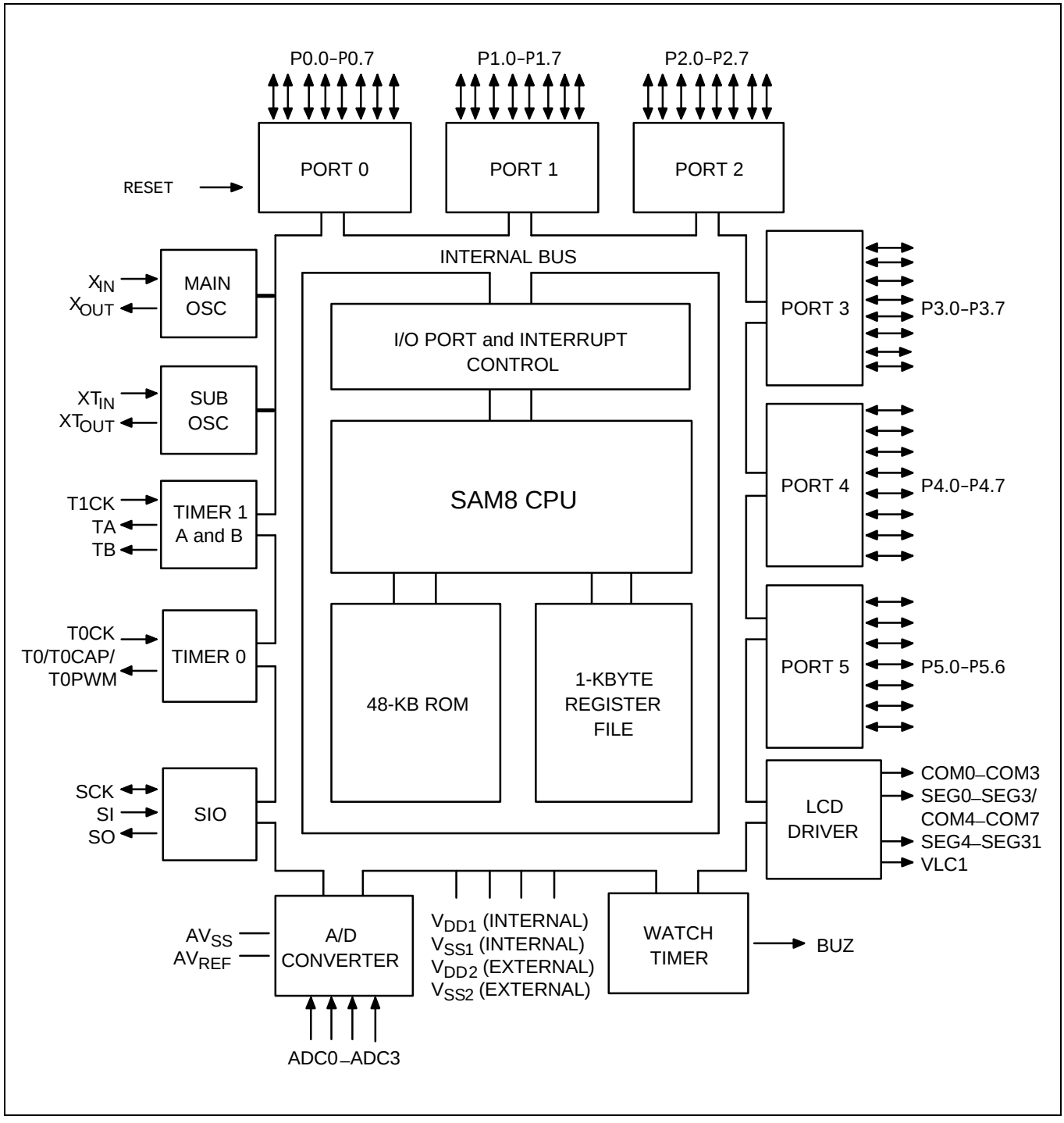

Figure 1-1. Block Diagram

PIN ASSIGNMENTS

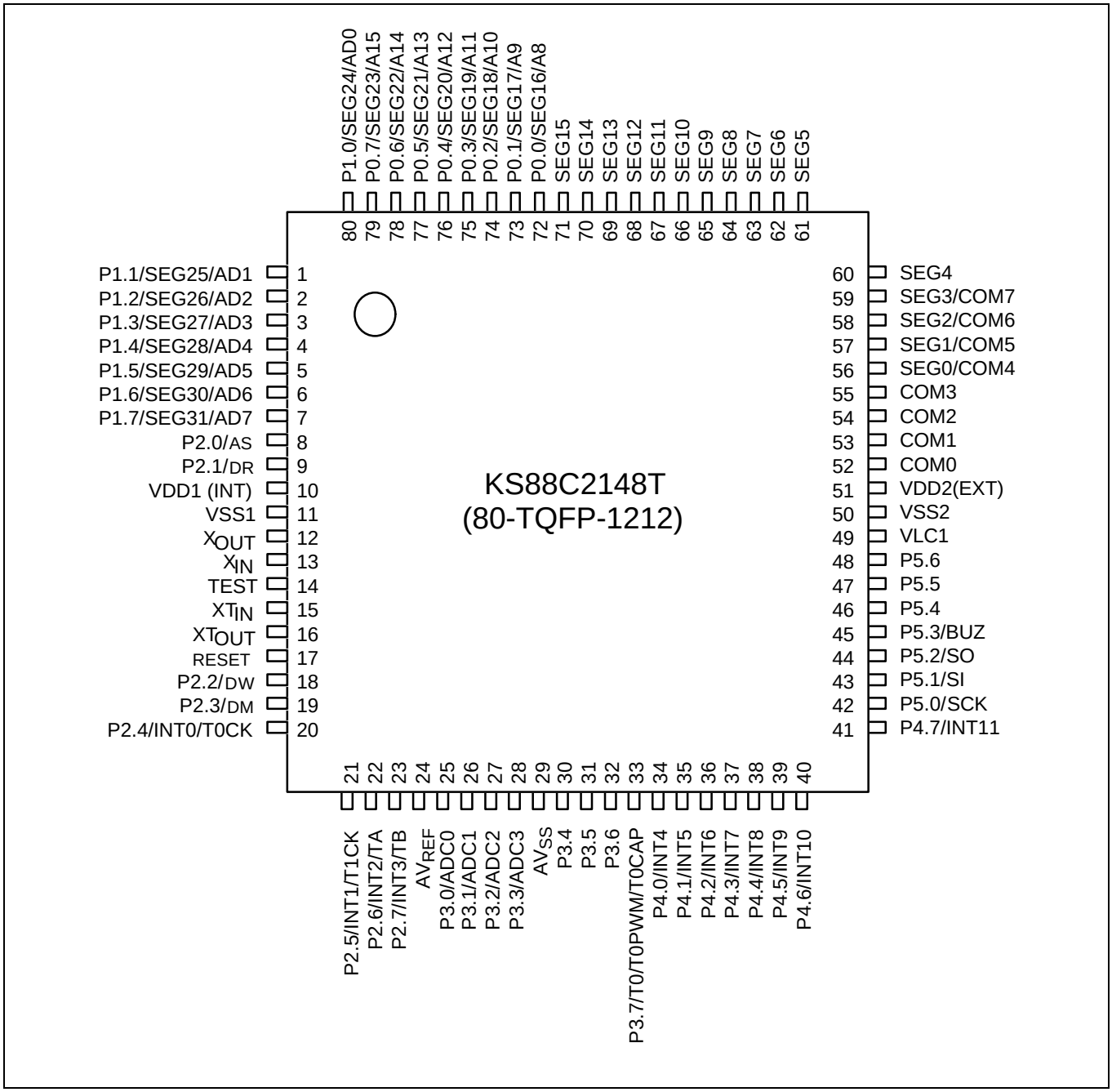

Figure 1-2. KS88C2148 Pin Assignments (80TQFP)

PIN ASSIGNMENT (Continued)

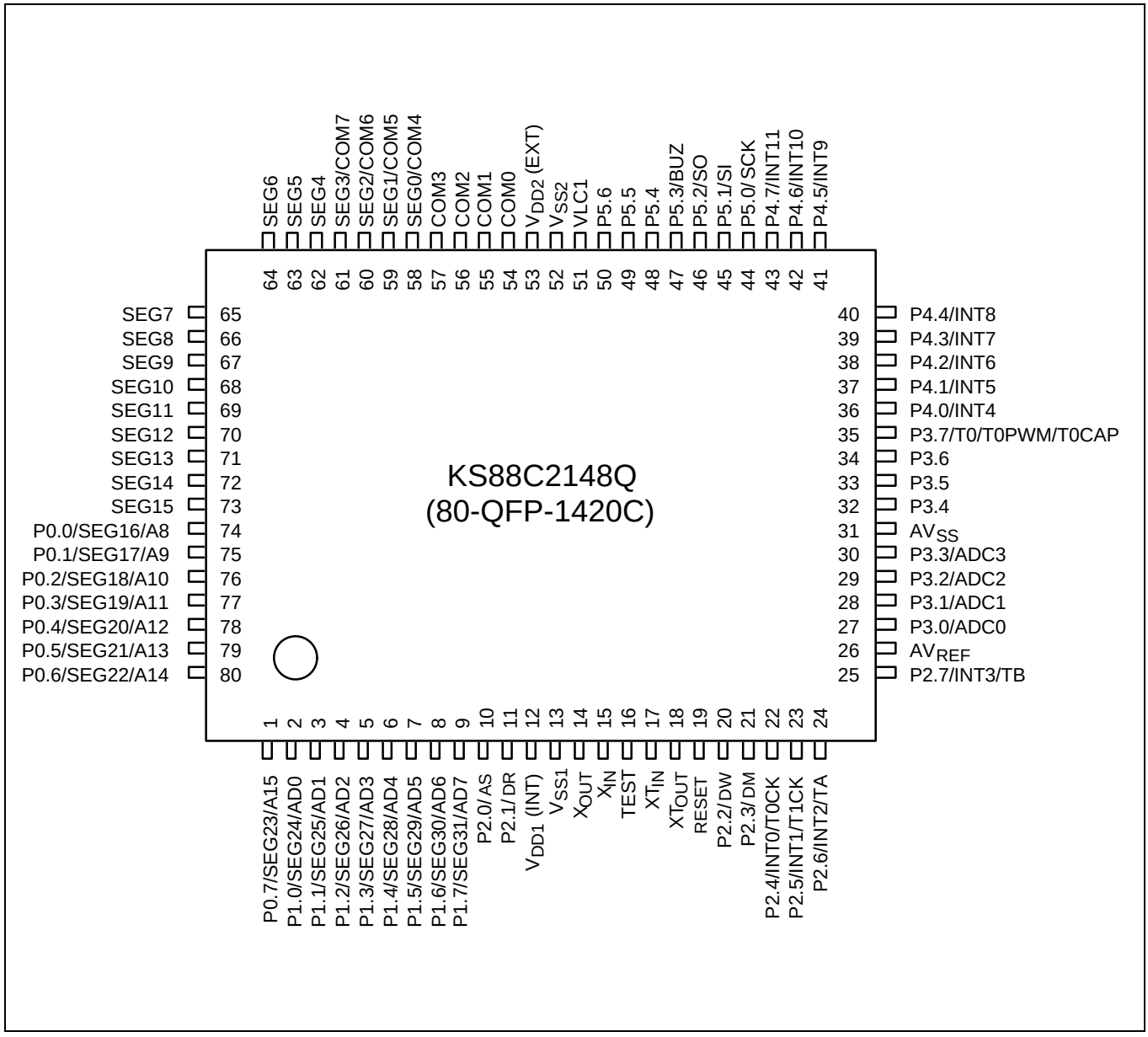

Figure 1-3. KS88C2148 Pin Assignments (80QFP)

PIN DESCRIPTIONS

Table 1-1. KS88C2148 Pin Descriptions

Pin Names	Pin Type	Pin Description	Circuit Type	Pin Numbers	Share Pins
P0.0–P0.7	I/O	4-bit-programmable I/O port. Pull-up resistors and open-drain outputs are software assignable. Pull-up resistors are automatically disabled for out pins. Configurable as LCD segments/external interface address lines	H-32	72–79 (74–80, 1)	SEG16/A8 – SEG23/A15
P1.0–1.7	I/O	4-bit-programmable I/O port. Pull-up resistors and open-drain outputs are software assignable. Pull-up resistors are automatically disabled for out pins. Configurable as LCD segments external interface address and data lines	H-32	80, 1–7 (2–9)	SEG24/AD0 – SEG31/AD7
P2.0 P2.1 P2.2 P2.3 P2.4 P2.5 P2.6 P2.7	I/O	1-bit-programmable I/O port. Pull-up resistors are software assignable, and automatically disabled for out pins. P2.0–P2.3 can alternately be used as external interface lines. P2.4–P2.7 are configurable as alternate functions or external interrupts at falling edge with noise filters.	D-4	8 (10) 9 (11) 18 (20) 19 (21) 20 (22) 21 (23) 22 (24) 23 (25)	AS DR DW DM INT0/T0CK INT1/T1CK INT2/TA INT3/TB
P3.0–P3.3 P3.4–P3.6 P3.7	I/O	1-bit-programmable I/O port. Pull-up resistors are software assignable, and automatically disabled for out pins. P3.0–P3.3 can alternately be used as ADC. P3.7 is configurable as an alternate function.	F-16 D-4 D-4	25–28 (27–30) 30–32 (32–34) 33 (35)	ADC0–ADC3 T0/T0PWM/ T0CAP
P4.0–P4.7	I/O	1-bit-programmable I/O port. Pull-up resistors and open-drain outputs are software assignable. Pull-up resistors are automatically disabled for out pins. P4.0–P4.7 are configurable as external interrupts at the selectable edge with noise filters.	E-4	34–41 (36–43)	INT4–INT11
P5.0 P5.1 P5.2 P5.3 P5.4–P5.6	I/O	1-bit-programmable I/O port. Pull-up resistors are software assignable, and automatically disabled for out pins. P5.0–P5.3 are configurable as alternate functions. If SCK and SI are used as input, these pins have noise filters.	D-4	42 (44) 43 (45) 44 (46) 45 (47) 46–48 (48–50)	SCK SI SO BUZ

Table 1-1. KS88C2148 Pin Descriptions (Continued)

Pin Names	Pin Type	Pin Description	Circuit Type	Pin Numbers	Share Pins
V_{SS1}, V_{DD1}	–	Power input pins for internal power block	–	10, 11 (12, 13)	–
X_{OUT}, X_{IN}	–	Main oscillator pins	–	12, 13 (14, 15)	–
TEST	–	Chip test input pin Hold GND when the device is operating	–	14 (16)	–
XT_{IN}, XT_{OUT}	–	Sub oscillator pins for sub-system clock	–	15,16 (17,18)	–
RESET	I	RESET signal input pin. Schmitt trigger input with internal pull-up resistor.	B	17 (19)	–
INT0–INT3	I/O	External interrupts input with noise filter.	D-4	20–23 (22–24)	P2.4–P2.7
T0CK	I/O	8Bit Timer 0 external clock input.	D-4	20 (22)	P2.4
T1CK	I/O	Timer A external clock input.	D-4	21 (23)	P2.5
TA	I/O	Timer 1A clock output	D-4	22 (24)	P2.6
TB	I/O	Timer 1B clock output	D-4	23 (25)	P2.7
T0	I/O	Timer 0 clock output	D-4	33 (35)	P3.7
T0PWM	I/O	Timer 0 PWM output	D-4	33 (35)	P3.7
T0CAP	I/O	Timer 0 capture input	D-4	33 (35)	P3.7
ADC0–ADC3	I/O	Analog input pins for A/D converts module	F-16	25–28 (27–30)	P3.0–P3.3
AV_{REF}, AV_{SS}	–	A/D converter reference voltage and ground	–	24, 29 (26, 31)	–
INT4–INT11	I/O	External interrupts input with noise filter.	E-4	34–41 (36–43)	P4.0–P4.7
BUZ	I/O	Buzzer signal output	D-4	45(47)	P5.3
SCK, SI, SO	I/O	Serial clock, serial data input, serial data output	D-4	42–44 (44–46)	P5.0–P5.2
V_{LC1}	–	LCD bias voltage input pins	–	49 (51)	–
V_{SS2}, V_{DD2}	–	Power input pins for external power block	–	50, 51 (52, 53)	–
COM0–COM3	O	LCD Common signal output	H-30	52–55 (54–57)	–
SEG0–SEG3 (COM4–COM7)	O	LCD Common or Segment signal output	H-31	56–59 (58–60)	–
SEG4–SEG15	O	LCD segment signal output	H-29	60–71 (62–73)	–

Table 1-1. KS88C2148 Pin Descriptions (Concluded)

Pin Names	Pin Type	Pin Description	Circuit Type	Pin Numbers	Share Pins
SEG16–SEG23	I/O	LCD segment signal output	H-32	72–79 (74–80, 1)	P0.0–P0.7
SEG24–SEG31	I/O	LCD segment signal output	H-32	80, 1–7 (2–9)	P1.0–P1.7
A8–A15	I/O	External interface address lines	H-32	72–79 (74–80, 1)	P0.0–P0.7
AD0–AD7	I/O	External interface address/data lines	H-32	80, 1–7 (2–9)	P1.0–P1.7
AS	I/O	Address strobe	D-4	8 (10)	P2.0
DR	I/O	Data read	D-4	9 (11)	P2.1
DW	I/O	Data write	D-4	18 (20)	P2.2
DM	I/O	Data memory select	D-4	19 (21)	P2.3