SAMSUNG ELECTRONICS

KS88C4400/4404
8-Bit CMOS Microcontroller

Data Sheet

DESCRIPTION

The KS88C4400/4404 single-chip 8-bit microcontroller is fabricated using a highly advanced CMOS process. With 42 I/O ports, UART, two 8-bit timers, two 16-bit timer/counters, PWM with data capture, A/D converter. KS88C4400 has no internal mask ROM, but KS88C4404 has a 4-Kbyte internal mask ROM. The KS88C4400/4404 offers an excellent design solution for a wide range of consumer electronics applications.

FEATURES

CPU

- SAM8 CPU core

Memory

- 1040-byte internal register file
- 64-Kbyte program memory
  (KS88C4404 internal ROM size: 4-Kbyte;
  KS88C4400 internal ROM size: 0 byte)
- 64-Kbyte external data memory area

Instruction Set

- 78 instructions, including IDLE and STOP instructions for power-down modes

Instruction Execution Time

- Minimum 33 ns at 18 MHz f_{OSC} (KS88C4400)
- Minimum 240 ns at 25 MHz f_{OSC} (KS88C4404)

Interrupts

- Fast interrupt processing (levels 0 and 3–7 only)

General I/O

- Six 8-bit general I/O ports
- One 8-bit n-channel, open-drain output port
- One 8-bit input port (ADC input or port7)

A/D Converter

- Eight analog input pins
- 8-bit A/D conversion resolution
- 10.66-µs conversion speed with 18-MHz

Timers

- Two 8-bit timers with interval or PWM mode

Timer/Counters

- Two 16-bit timer/counters with four selectable operating modes

Serial Port

- Full-duplex serial data port (UART)
- Four programmable operating modes:

Pulse width Modulation

- Two output channels (PWM0, PWM1)
- 8-bit resolution with 2-bit prescaler
- Frequency: 70.305 kHz (18 MHz CPU clock)
- Capture module with CAP input pin

Oscillator Frequency

- 1 MHz to 18 MHz (KS88C4400)
- 1 MHz to 25 MHz (KS88C4404)

Operating Temperature Range

- –20°C to +85°C

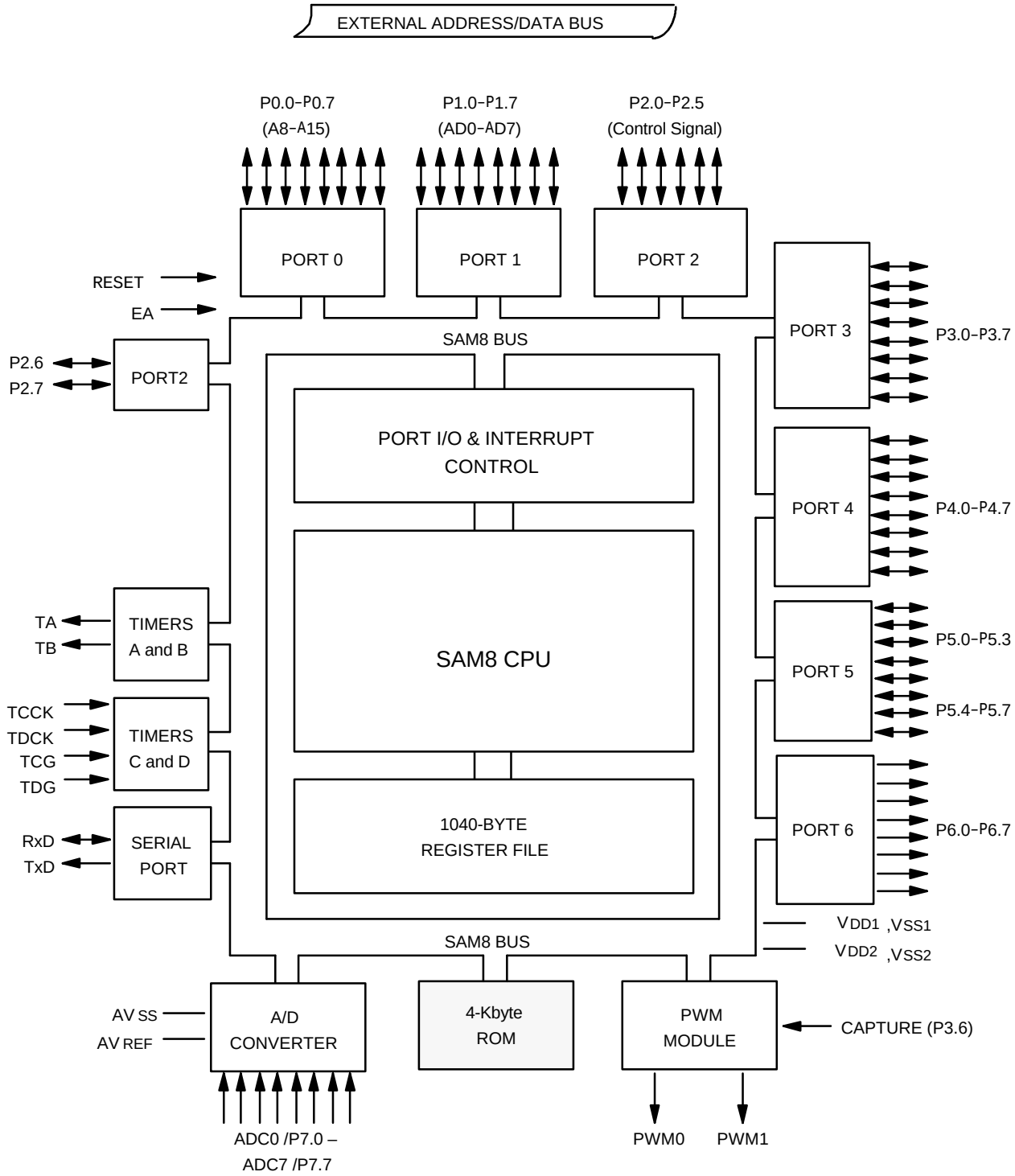
Operating Voltage Range

- 4.5 V to 6.0 V (KS88C4400)
- 4.5 V to 5.5 V (KS88C4404)

Package Type

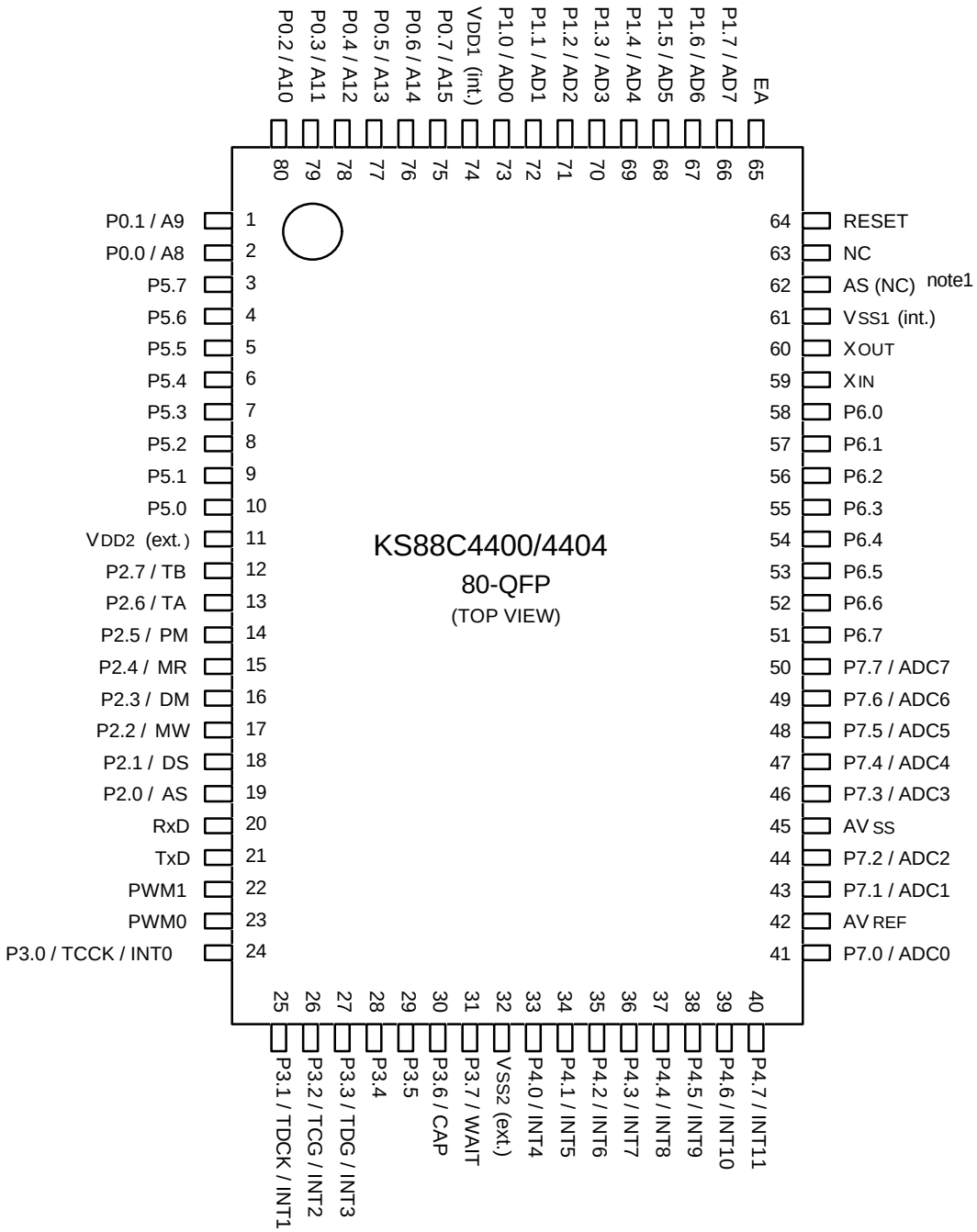
- 80-pin QFP, 80-pin TQFP

BLOCK DIAGRAM



NOTE: KS88C4404 has a 4-Kbyte internal program memory, but KS88C4400 has no internal program memory.

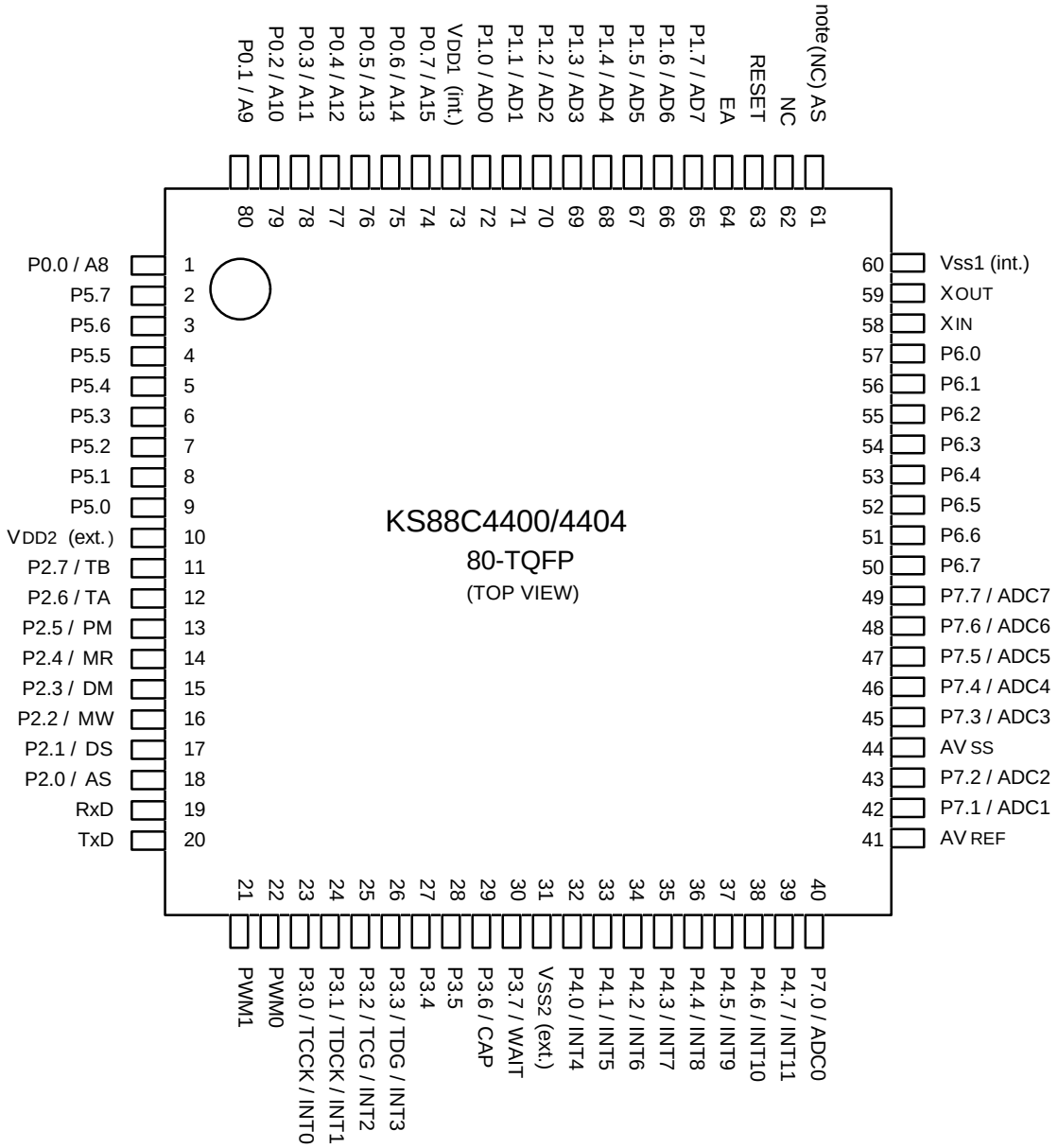
PIN ASSIGNMENTS



NOTES

1. Address Strobe (AS) is only available in the KS88C4404.
2. In the KS88C4400, P0, P1 and P2.0-2.5 are configured only for external interface because it has no internal program memory.

PIN ASSIGNMENTS (Continued)



NOTES

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PIN DESCRIPTIONS

Pin Name	Pin Type	Pin Description	QFP Pin Number	Share Pins
P0.0–P0.7	I/O	Nibble programmable port; input or output mode selected by software; Schmitt trigger input or push-pull, open-drain output with software assignable pull-ups; alternately configurable as external interface address lines A8–A15.	2–1, 80–75	A8–A15
P1.0–P1.7	I/O	Same general characteristics as port 0; alternately configurable as external interface address/data lines AD0–AD7.	73–66	AD0–AD7
P2.0–P2.7	I/O	General I/O port with Schmitt trigger input or push-pull output. bit programmable; P2.0/Address Strobe (AS) P2.1/Data Strobe (DS) P2.2/Memory Write (MW) P2.3/Data Memory select (DM) P2.4/Memory Read (MR) P2.5/Program Memory select (PM) P2.6/timer A output (TA) P2.7/timer B output (TB)	19–12	AS, DS, MW, DM, MR, PM, TA, TB
P3.0–P3.7	I/O	General I/O port with bit programmable pins; Schmitt trigger input or push-pull output with software assignable pull-ups; |input/output mode selectable by software; P3.0–P3.3 are alternately used for external interrupt input (noise filters, interrupt enable and pending control); P3.0/timer C clock input (TCCK)/INT0 P3.1/timer D clock input (TDCK)/INT1 P3.2/timer C gate input (TCG)/INT2 P3.3/timer D gate input (TDG)/INT3 P3.6/Capture data input (CAP) P3.7/WAIT for slow memory interface	24–31	TCCK / INT0, TDCK / INT1, TCG / INT2, TDG / INT3, CAP, WAIT
P4.0–P4.7	I/O	General I/O port with bit programmable pins; Schmitt trigger input or push-pull, open-drain output; software assignable pull-ups; input/output mode selectable by software; P4.0–P4.7 can alternately be used as inputs for external interrupts INT4–INT11; noise filters, interrupt control	33–40	INT4–INT11
P5.0–P5.7	I/O	General I/O port with nibble programmable pins; Schmitt trigger input or push-pull, open–drain output; software assignable pull-ups; input/output mode selectable by software;	10–3	–
P6.0–P6.7	O	Output port; n-channel open-drain output pins; up to 9-volt capacity	58–51	–

PIN DESCRIPTIONS (Continued)

Pin Name	Pin Type	Pin Description	QFP Pin Number	Share Pin
ADC0–ADC7	I	Analog input pins for A/D converter module; alternately, general-purpose input port 7	41, 43–44, 46–50	P7.0–P7.7
RESET	I	System reset pin (pull-up resistor: 280 kΩ)	64	–
EA	I	External access (EA) pin with three modes: 0 V: Not allowed in KS88C4400/4404. 5V: ROM–less operation (external interface)	65	–
RxD	I/O	Serial data RxD pin; receive input and transmit output (mode 0)	20	–
TxD	O	Serial data TxD pin; transmit output, shift clock (mode 0)	21	–
PWM0, PWM1	O	Pulse width modulation output pins	23, 22	–
V_{DD1}, V_{DD2}	–	Power supply	74, 11	–
V_{SS1}, V_{SS2}	–	Ground	61, 32	–
X_{IN}, X_{OUT}	–	Main oscillator pins	59, 60	–
NC	–	No connections (connect to V_{SS})	62, 63	–
AV_{REF}, AV_{SS}	–	A/D converter reference voltage and ground	42, 45	–

NOTE: $V_{DD1}$and V_{DD2} must be connected in external circuit (same to V_{SS1} and V_{SS2}).

FUNCTION OVERVIEW

ADDRESS SPACES

Overview

The KS88C4400/4404 has three kinds of address space:

— Internal register file
— External program memory
— External data memory
— Internal data memory (only for KS88C4404)

A 16-bit address/data bus supports both external program memory and external data memory operations. Special instructions and internal logic determine when the 16-bit bus carries addresses and data for the program memory or for external memory locations. A separate 8-bit register bus carries addresses and data between the CPU and the internal register file.

Program Memory

The KS88C4400 has no internal program memory (ROM), but KS88C4404 has a 4-Kbyte internal program memory (ROM).

The KS88 interrupt structure supports up to 126 vector addresses. Twenty vectors are used for the KS88C4400/4404 interrupt structure. The first 256 bytes of the ROM (0H–FFH) are reserved for the maximum number of vectors. Unused locations in this address range can be used as normal program memory. The reset address in the ROM is 0020H.

Using the external interface, 64-Kbyte of program memory *and* 64-Kbyte of data memory space can be accessed. These spaces can be combined or they can be kept separate. If separate program and data memory areas are configured, selective access is controlled by the DM (data memory) and PM (program memory) signal line.

Register File

The physical 256-byte space is logically extended into four 256-byte pages, giving a total of 1024 general-purpose registers. The upper 64-byte area of the register file is extended into two sets called *set 1* and *set 2*. Set 1 is further divided into two 32-byte register banks, called bank 0 and bank 1, and a 32-byte common area.

The total register file space is 1120 bytes (256 bytes × 4 pages) + set 1 (64 bytes + 32 bytes). However, because only locations FFH–F9H are mapped in set 1, bank 1, the KS88C4400/4404 register file has a total of 1095 8-bit registers. Of these 1088 registers, 13 bytes are CPU and system control registers, and 35 bytes are for peripheral control and data registers. There are 1040 general-purpose registers.

Register Addressing

The SAM8 register architecture provides an efficient method of working register addressing that takes full advantage of shorter instruction formats to reduce execution times. Registers can be addressed either as a single 8-bit register or a 16-bit register pair.

The SAM8 instruction set supports seven addressing modes. Not all of these addressing modes are available for each instruction. The seven addressing modes and their symbols are:

— Register (R)
— Indirect Register (IR)
— Indexed (X)
— Direct Address (DA)
— Indirect Address (IA)
— Relative Address (RA)
— Immediate (IM)

In Register (R) addressing mode, the operand value is the content of a specific register or register pair. You can use this mode to access all locations in the internal register file except for set 2. Working register addressing uses register pointers to select a specific register within a working register space.

To increase the speed of context switches during program execution, you use the register pointers to dynamically select movable 8-byte "slices" of the register file as active working register space.

System and User Stacks

KS88-series microcontrollers use the system stack to implement subroutine calls and returns, for interrupt processing, and for dynamic data storage. The PUSH and POP instructions support system stack operations. Hardware support is provided for stack operations in the internal register file as well as in external data memory. User stacks can be freely defined in the register file for dynamic data storage.

EXTERNAL INTERFACE

The KS88C4400/4404 architecture supports an external peripheral interface. Instruction code can be fetched, or data read/write, from external program memory. If the external program memory is implemented in a RAM-type device, program code and data can also be written to external program memory (by "LDCxx" instructions).

The KS88C4400/4404 microcontroller has a total of 80 pins. Up to 23 pins can be configured as external interface lines. Because memory addresses that are carried over the address and data bus are 16 bits, up to 64 K bytes of data memory and/ or program memory space can be addressed.

External data memory accesses can be handled separately from external program memory accesses by defining (DM and PM) signal line. DM output remains high level (PM is low level) when instructions are being fetched or when accessing the external program memory; DM output goes to low level whenever an external data memory location is addressed (by "LDExx" instructions).

INTERRUPTS

The SAM8 interrupt structure has three components: levels, vectors, and sources. Eight interrupt levels are recognized by the CPU. Up to 126 vector addresses are supported for each level. When a specific interrupt level is assigned more than one vector address, these vectors are prioritized in hardware. Each vector may, in turn, have one or more sources.

The KS88C4400/4404 microcontroller has 20 interrupt sources. Nineteen different vector addresses are used to support these interrupt sources. Only seven interrupt levels are used in the interrupt structure.

When multiple interrupt levels are active, the interrupt priority register (IPR) determines the order in which contending interrupts are to be serviced. If multiple interrupts occur within the same interrupt level, the interrupt with the lowest vector address is processed first. The relative priorities of multiple interrupts within a single level are set in hardware.

The instruction pointer (IP) is used to control optional high-speed interrupt processing called *fast interrupts*. With fast interrupt processing, specific interrupt service routines be completed in approximately six clock cycles instead of the usual 22 cycles. For the KS88C4400/4404, fast interrupt processing is not supported for interrupt levels 1 and 2.

INSTRUCTION SET

The SAM8 instruction set is designed to support a large register file. It includes 78 arithmetic and logical operations, including multiply and divide. Binary-coded decimal (BCD) operations include decimal adjustment of binary values.

Because I/O control and data registers are mapped directly into the register file, special I/O instructions are not necessary. Flexible instructions for bit addressing, and for rotate and shift operations complete the powerful data manipulation capabilities of the instruction set.

CLOCK CIRCUITS

An external crystal produces a maximum 18-MHz CPU clock in the KS88C4400 and 25–MHz in the KS88C4404. The X_{IN} and X_{OUT} pins connect the external oscillation source to the on-chip clock circuit. The main oscillator circuit generates the CPU clock signal. To increase processing speed and to reduce noise levels, non-divided logic is implemented for the main clock circuit.

RESET and POWER-DOWN MODES

A reset is initiated by holding the signal at the RESET pin to low level for at least 22 CPU clocks during power is supplied.. If the EA pin is held at high level (5-volt input) prior to a reset, ROM-less mode is initiated and the external interface is automatically configured by hardware.

The instruction IDLE invokes Idle mode. In Idle mode, the CPU "sleeps" while select peripherals remain active: For the KS88C4400/4404, these peripherals are the PWM module, serial I/O port, timers A and B, timers C and D, and external interrupt logic.

During Idle mode, the contents of system registers, control registers, and data registers are retained. Port pins retain the mode (input or output) they had at the time Idle mode was entered. There are two ways to release Idle mode: 1) activate an enabled interrupt, causing a hardware release of Idle mode, and 2) execute an external reset.

The instruction STOP invokes Stop mode. In Stop mode, the CPU and all peripherals "sleep" (that is, the on-chip main oscillator is halted). Data stored in the internal register file and the current values of peripheral registers are retained. The only way to release Stop mode is by executing a reset.

When RESET is released and goes high level, the processor restarts the program from ROM vector address 0020H.

I/O PORTS

Of the 80 pins in the KS88C4400/4404 package, 64 pins are used for I/O. There are six I/O ports, one Input port and one output port. Each I/O port can be configured by software to meet varied system configuration and design requirements. The CPU accesses an I/O port directly by writing or reading the port's data register. For this reason, no special I/O instructions are required.

Ports 0–2 are configured as address and data lines and bus signal lines for the external peripheral interface.

The 8-bit input port can receive analog data for the A/D converter module, or it can serve as a general input port (port 7).

TIMER MODULE 0

The KS88C4400/4404 timer module 0 (T0) has two 8-bit timers called timer A and timer B. Each timer has an 8-bit counter register, an 8-bit data register, an 8-bit comparator, and a corresponding output pin. Both timers run continuously.

Timer A and timer B operate in interval mode or in pulse width modulation (PWM) mode. The LSB of the T0CON register controls the timer A operating mode, and the LSB of the TBCON register controls the operating mode for timer B. Timer A and timer B are driven by the same clock input. There are two options for timer clock input: the non-scaled CPU clock or the CPU clock divided by 1024 (decimal).

TIMER MODULE 1

The KS88C4400/4404 has two 16-bit timer/counters, called timer C and timer D. Both can be configured to operate either as timers or as event counters. Timer module 1 can operate in four different modes:

Mode 0	13-bit timer/counter
Mode 1	16-bit timer/counter
Mode 2	8-bit auto-reload timer/counter
Mode 3	Two 8-bit timer/counters (timer D disabled)

When used as an interval timer, the corresponding count register is incremented based on the internal timer clock rate. The timer clock can be selected as either an external clock source, or a divided-by-six CPU clock. When used as an event counter, the timer's count register is incremented whenever a 1-to-0 transition occurs at its external input pin. The external input is sampled on every fifth cycle of a 6-cycle CPU clock.

UART

The KS88C4400/4404 has a full-duplex serial port with four programmable operating modes: There is one synchronous mode and three UART (Universal Asynchronous Receiver/Transmitter) modes:

— Serial I/O with baud rate of CPU clock /6
— 8-bit UART mode; variable baud rate
— 9-bit UART mode; CPU clock /32 or /16
— 9-bit UART mode, variable baud rate

Serial port receive and transmit buffers are both accessed through the shift register, SIO (E9H). Writing to the shift register loads the transmit buffer; reading the shift register accesses a physically separate receive buffer. The serial port is receive-buffered. The receive data buffer enables reception of the next byte to start before the previously received byte has been read from the receive register. If, however, the first byte has not been read by the time the next byte is completely received, the first byte is overwritten.

In all four operating modes, data transmission starts when any instruction uses the SIO register as its destination address.

PULSE WIDTH MODULATION

The pulse width modulation (PWM) module has the following components:

— 16-bit counter with 2-bit prescaler
— Two 8-bit comparators
— Two 8-bit PWM data registers (PWM0, PWM1)
— PWM control register (PWMCON)
— PWM counter overflow interrupt (IRQ1)
— Two PWM output pins (PWM0, PWM1)

An 8-bit capture unit is included in the PWM module. The capture unit is controlled by PWMCON register settings and has the following components:

— 8-bit capture register (PWMCAP)
— Capture input pin (P3.6 /CAP, pin 30)
— Capture input interrupt (IRQ1, vector BAH)

The two 8-bit PWM circuits function identically: Each has its own 8-bit data register and 8-bit comparator. Each circuit compares a unique data register value to the lower 8-bit value of the 16-bit PWM counter.

The PWM module includes an integrated 8-bit data capture unit. The capture unit captures the upper 8-bit value of the 16-bit counter when a signal edge transition is detected at the CAP pin. The captured value is then dumped into the PWMCAP register where it can be read. In this way, it can be used to measure the pulse width of the incoming signals.

A/D CONVERTER

The 8-bit A/D converter (ADC) module uses successive approximation logic to convert single-channel analog inputs to equivalent 8-bit digital values. The analog input level must lie between the AV_{REF} and AV_{SS} values.

To start an analog-to-digital conversion procedure, you write the SCH bits in the A/D converter control register ADCON to select one of the eight analog input pins (ADCn, n = 0–7).

The KS88C4400/4404 performs 8-bit conversions for one input channel at a time. You can dynamically select different channels by manipulating the SCH bit values (SCH0–SCH2) in the ADCON register.

The A/D conversion process requires 24 CPU clocks to convert each bit. Therefore, 192 clocks are required to complete a full 8-bit conversion. The digital result is dumped into the output register ADOUT and the ADC module enters an idle state.

Because the ADC does not generate an interrupt to signal a completed conversion, you must first read the content of ADOUT before another conversion starts. Otherwise, the previous result is overwritten.

D.C. ELECTRICAL CHARACTERISTICS

(T_A = –20°C to +85°C, V_{DD} = 4.5 V to 6.0 V note)

Parameter	Symbol	Conditions	Min	Typical	Max	Unit
Input High Voltage	V_{IH1}	All input pins except V_{IH2}	0.8 V_{DD}	–	V_{DD}	V
	V_{IH2}	X_{IN}	V_{DD} – 0.5			
Input Low Voltage	V_{IL1}	All input pins except V_{IL2}	–	–	0.2 V_{DD}	V
	V_{IL2}	X_{IN}			0.4	
Output High Voltage	V_{OH1}	V_{DD} = 4.5 V to 6.0 V I_{OH} = –1 mA; Ports AD only	V_{DD} – 1.0	–	–	V
	V_{OH2}	V_{DD} = 4.5 V to 6.0 V I_{OH} = –200 µA All output pins except port AD	V_{DD} – 1.0			
Output Low Voltage	V_{OL1}	V_{DD} = 4.5 V to 6.0 V I_{OL} = 2 mA All output pins except port 5	–	–	0.4	V
	V_{OL2}	V_{DD} = 4.5 V to 6.0 V I_{OL} = 1.5 mA Port 5			0.4	
Input High Leakage Current	I_{LIH1}	V_{IN} = V_{DD} All input pins except X_{IN}	–	–	3	µA
	I_{LIH2}	V_{IN} = V_{DD}; X_{IN}			20	
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{IN}, and RESET	–	–	–3	µA
	I_{LIL2}	V_{IN} = 0 V; X_{IN}			–20	
Output High Leakage Current	I_{LOH1}	V_{OUT} = V_{DD} All output pins except port 6	–	–	5	µA
	I_{LOH2}	Port 6 (open-drain) V_{OUT} = 9 V			20	
Output Low Leakage Current	I_{LOL}	V_{OUT} = 0 V	–	–	–5	µA
Pull-up Resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% Ports 4, 5, and RxD	30	56	80	kΩ
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% RESET only	120	220	320	

NOTE: The operating voltage range of KS88C4404 is from 4.5 V to 5.5 V.

SUPPLY CURRENT CHARACTERISTICS FOR KS88C4400 MICROCONTROLLER

(T_A = – 20°C to + 85°C, V_{DD} = 4.5 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typical	Max	Unit
Supply Current (note)	I_{DD1}	V_{DD} = 5 V ± 10% 18 MHz crystal oscillator	–	32	50	mA
		V_{DD} = 5 V ± 10% 12 MHz crystal oscillator		22		
	I_{DD2}	Idle mode; V_{DD} = 5 V ± 10% 18 MHz crystal oscillator		7.9	25	
		Idle mode; V_{DD} = 5 V ± 10% 12 MHz crystal oscillator		5.8		
	I_{DD3}	Stop mode; V_{DD} = 5 V ± 10%		18	50	µA

NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.

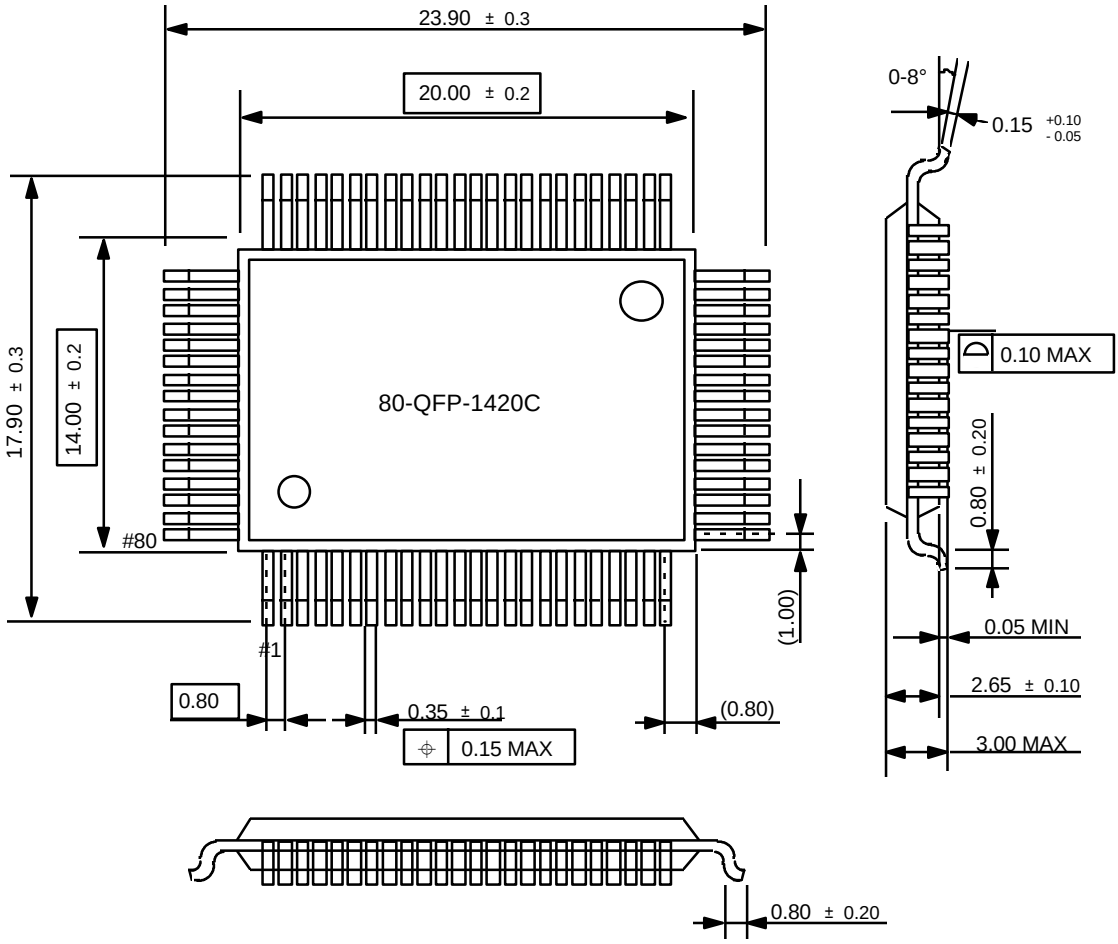
SUPPLY CURRENT CHARACTERISTICS FOR KS88C4404 MICROCONTROLLER

(T_A = – 20°C to + 85°C, V_{DD} = 4.5 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typical	Max	Unit
Supply Current (note)	I_{DD1}	V_{DD} = 5 V ± 10% 25 MHz crystal oscillator	–	35	50	mA
		V_{DD} = 5 V ± 10% 10 MHz crystal oscillator		30		
	I_{DD2}	Idle mode: V_{DD} = 5 V ± 10% 25 MHz crystal oscillator		11	25	
		Idle mode: V_{DD} = 5 V ± 10% 10 MHz crystal oscillator		5		
	I_{DD3}	Stop mode; V_{DD} = 5 V ± 10%		3	20	µA

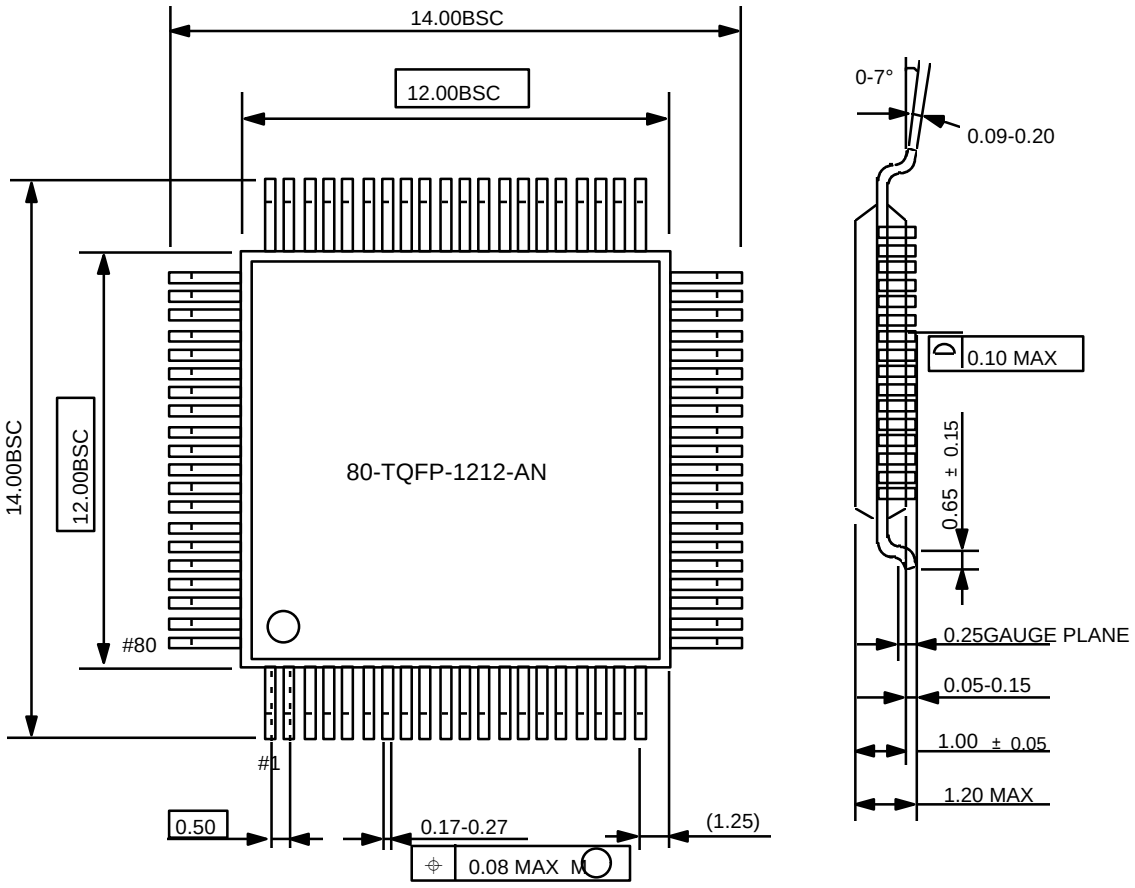
NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.

PACKAGE DIMENSIONS



NOTE : Dimensions are in millimeters.

PACKAGE DIMENSIONS (Continued)



NOTE : Dimensions are in millimeters.