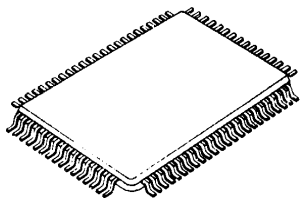
KS9283 DIGITAL SIGNAL PROCESSOR

INTRODUCTION

The KS9283 is a CMOS integrated circuit designed for the digital audio signal processor of the CDP (Compact Disc Player) application.
It is a monolithic IC that builts in 16K SRAM and DPLL.

80-QFP-1420C



ORDERING INFORMATION

Device	Package	Operating Temperature
KS9283	80-QFP-1420C	-20℃~ +75℃

FEATURES

- EFM data demodulation
- Built-in frame sync detection, protection and Insertion circuit
- Correction of C1, C2 error
- Interpolation
- Subcode data serial output
- CLV servo Controller
- Tracking counter
- Micom interface
- Built-in 16K SRAM
- Digital audio output
- Built-in digital PLL
- Single power supply: V_{DD} = 4.5 ~ 5.5V

BLOCK DIAGRAM

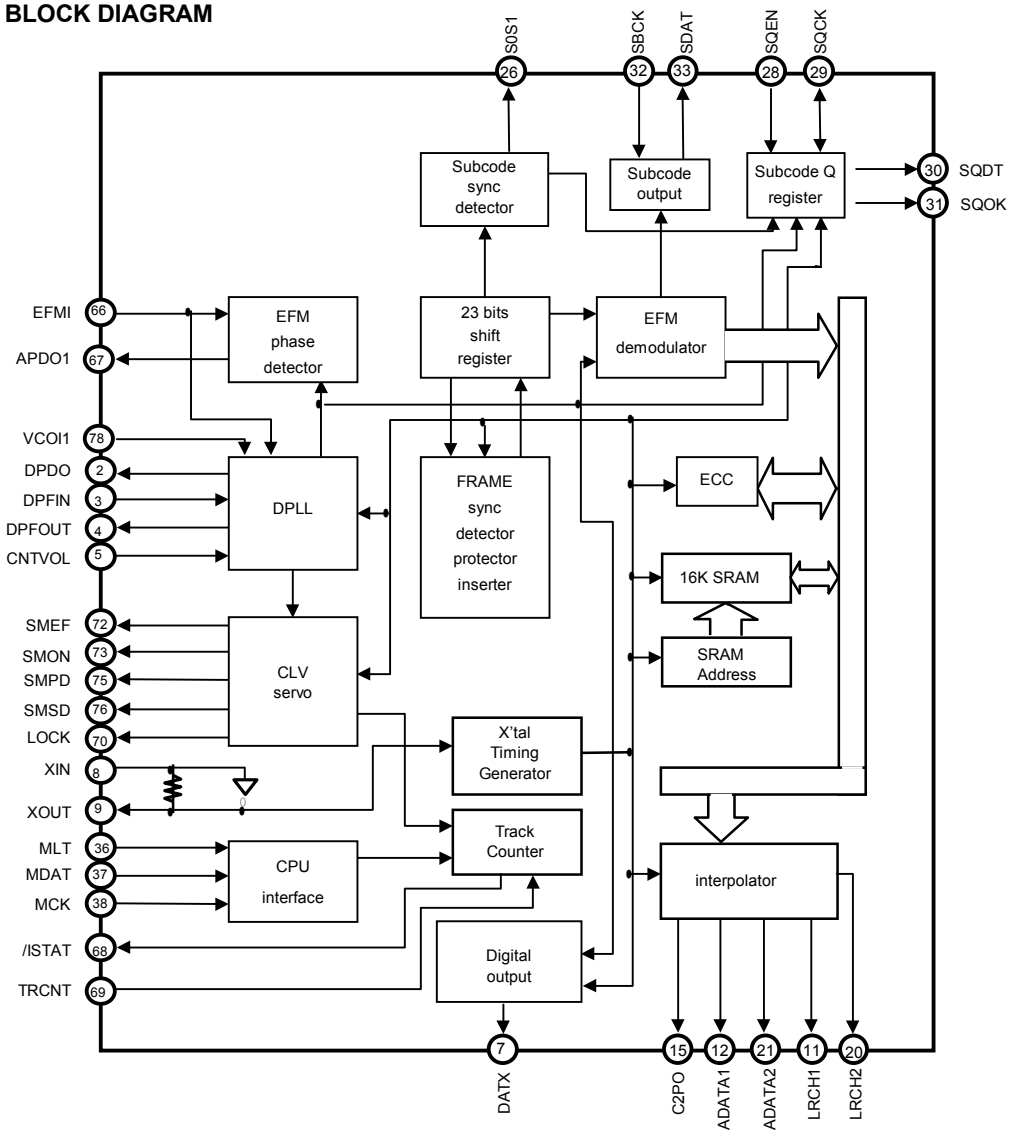
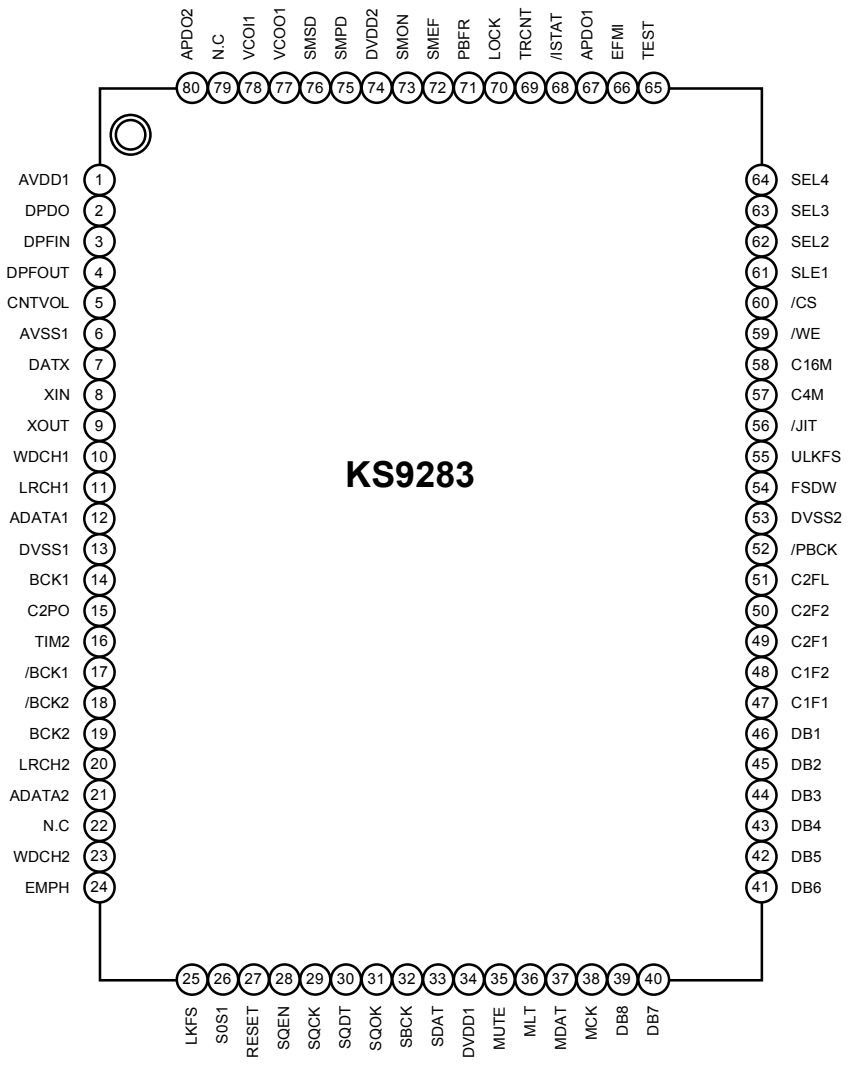


Fig. 1

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	$AV_{DD}1$	-	Analog V_{CC1}
2	DPDO	O	Charge pump output for master PLL
3	DPFIN	I	Filter input for master PLL
4	DPFOUT	O	Filter output for master PLL
5	CNTVOL	I	VCO control voltage for master PLL
6	AV_{SS1}	-	Analog ground1
7	DATX	O	Digital audio output
8	XIN	I	X-tal oscillator input
9	XOUT	O	X-tal oscillator output
10	WDCH1	O	Word clock of 48 bits/SLOT
11	LRCH1	O	Channel clock of 48 bits/SLOT
12	ADATA1	O	Serial audio data output of 48 bits/SLOT (MSB first)
13	DV_{SS1}	-	Digital ground1
14	BCK1	O	Audio data bit clock for 48 bits/SLOT
15	C2PO	O	C2 pointer for output audio data
16	TIM2	O	Terminal for test (floating)
17	/BCK1	O	negative clock of BCK1
18	/BCK2	O	negative clock of BCK2
19	BCK2	O	Audio data bit clock of 64 bits/SLOT
20	LRCH2	O	Channel clock of 64 bits/SLOT
21	ADATA2	O	Serial audio data output 64 Bit/SLOT (LSB First)
22	N.C	-	No Connection
23	WDCH2	O	Word clock of 64 bits/SLOT

PIN DESCRIPTION (continued)

Pin No.	Symbol	I/O	Description
24	EMPH	O	Emphasis/Non-emphasis output (“H”: Emphasis)
25	LKFS	O	The Lock status output of frame Sync
26	SOS1	O	Output of subcode sync signal (SO + S1)
27	RESET	I	System reset at “L”
28	SQEN	I	SQCK I/O Control (“L”: internal clock, “H”: external clock)
29	SQCK	I/O	Clock for output subcode-Q data
30	SQDT	O	Serial output of subcode-Q data
31	SQOK	O	The CRC check result signal output of subcode-Q
32	SBCK	I	Clock for output subcode-Q data
33	SDAT	O	Subcode serial data output
34	DV_{DD}	-	Digital V_{CC} 1
35	MUTE	I	Mute control input (“H”: Mute ON)
36	MLT	I	Latch signal input from micom
37	MDAT	I	Serial data input from micom
38	MCK	I	Serial clock input from micom
39	DB8	I/O	SRAM data I/O port 8 (MSB)
40	DB7	I/O	SRAM data I/O port 7
41	DB6	I/O	SRAM data I/O port 6
42	DB5	I/O	SRAM data I/O port 5
43	DB4	I/O	SRAM data I/O port 4
44	DB3	I/O	SRAM data I/O port 3
45	DB2	I/O	SRAM data I/O port 2
46	DB1	I/O	SRAM data I/O port 1 (LSB)

PIN DESCRIPTION (continued)

Pin No.	Symbol	I/O	Description
47	C1F1	I/O	Monitoring output for C1 error correction (RA1)
48	C1F2	I/O	Monitoring output for C1 error correction (RA2)
49	C2F1	I/O	Monitoring output for C2 error correction (RA3)
50	C2F2	I/O	Monitoring output for C2 error correction (RA4)
51	C2FL	I/O	C2 decoder flag(High:When processing C2 is inpossible correction status)(RA5)
52	/PBCK	I/O	Output of VCO/2
53	DV_{SS2}	-	Digital ground 2
54	FSDW	I/O	Unprotected frame Sync (RA7)
55	ULKFS	I/O	Frame sync protection state (RA8)
56	/JIT	I/O	Display of eithr RAM overflow or underflow for ± 4 frame jitter margin (RA9)
57	C4M	I/O	Only monitoring signal (Normal playback: 4.2336MHz) (RA10)
58	C16M	I/O	16.9344MHz signal output (RA11)
59	/WE	I/O	Terminal for test
60	/CS	I/O	Terminal for test
61	SEL1	I	Mode selection terminal 2 (H: 33.8688MHz, L: 16.9344MHz)
62	SEL2	I	Mode selection terminal 2 (H: APLL, L: DPLL)
63	/SEL3	I	Mode selection terminal 3 (H: CDROM, L: CDP)
64	/SEL4	I	Mode selection terminal 4
65	TEST	I	Test terminal (L= Normal operating state)
66	EFMI	I	EFM signal input
67	APDO1	O	Charge pump output for analog PLL
68	/ISTAT	O	The internal status output
69	TRCNT	I	Tracking counter input signal

PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
70	LOCK	O	Output signal of LKFS condition sampled PBFR/16 (If LKFS is “H”,LOCK is “H” and if the LKFS which is sampled by PBFR/16 is “L” at least 8 times, LOCK is “L”)
71	PBFR	O	Write frame clock (Lock: 7.35KHz)
72	SMEF	O	LPF time constant control of the spindle servo error signal
73	SMON	O	ON/OFF control signal for spindle servo
74	$DV_{DD\,2}$	-	Digital V_{CC2}
75	SMPD	O	Spindle motor drive (Rough control in the speed mode. Phase control in the phase mode)
76	SMSD	O	Spindle Motor drive (Velocity control in the phase mode)
77	VCOO 1	O	VCO output signal (When the state is lock by means of PBFR, it is 8.643MHz)
78	VCOI 1	I	VCO input signal
79	N.C	I	Mode terminal (connect to VDD)
80	APDO2	O	Termial for test (floating)

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 ~ 7.0	V
Input Voltage	VI	-0.3 ~ 7.0	V
Output Voltage	V_O	-0.3 ~ 7.0	V
Operating Temperature	T_{OPR}	-20 ~ 75	℃
Storage Temperature	T_{STG}	-40 ~ 125	℃

ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{DD} = 5V, V_{SS} = 0V, Ta = 25℃, unless otherwise specified)

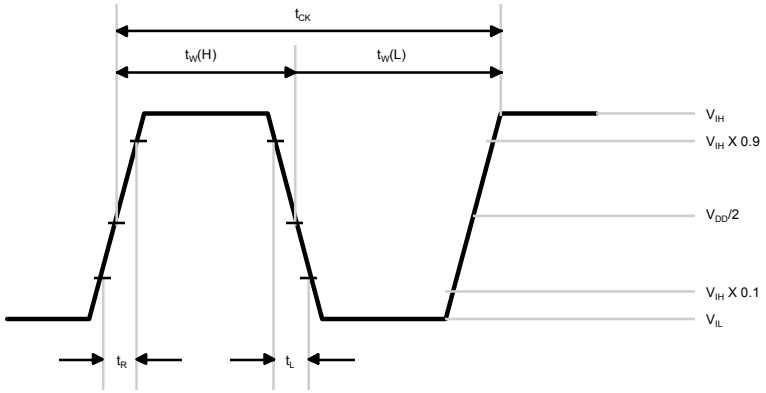
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
'H' INPUT VOLTAGE1	VIH (1)	(Note 1)	$0.7V_{DD}$	-	-	V
'L' INPUT VOLTAGE1	VIL (1)	(Note 1)	-	-	$0.3V_{DD}$	V
'H' INPUT VOLTAGE2	VIH (2)	(Note 2)	$0.8V_{DD}$	-	-	V
'L' INPUT VOLTAGE2	VIL (2)	(Note 2)	-	-	$0.2V_{DD}$	V
'H' OUTPUT VOLTAGE1	VOH (1)	I_{OH} = -1mA (Note 3)	V_{DD} - 0.5	-	V_{DD}	V
'L' OUTPUT VOLTAGE1	VOL (1)	I_{OH} = 1mA (Note 3)	0	-	0.4	V
'H' OUTUT VOLTAGE2	VOH (2)	I_{OH} = -1mA (Note 4)	V_{DD} - 0.5	-	V_{DD}	V
'L' OUTPUT VOLTAGE2	VOL (2)	I_{OL} = 2mA (Note 4)	0	-	0.4	V
INPUT LEAK CURRENT1	ILKG1	V_I = 0 ~ VDD (Note 5)	-5	-	5	uA
THREE STATE OUTPUT LEAK CURRENT	$L_{O\ (LKG)}$	V_O = 0 ~ VDD (Note 5)	-5	-	5	uA
INPUT LEAK CURRENT2	ILKG2	V_I = 0 ~ VDD (Note 6)	-30	-	30	uA

(Note 1) Related pins: All input pins except for pins of Note2
(Note 2) Related pins: Bidirection pins, MCK
(Note 3) Related pins: All output pins except for pins of Note 4
(Note 4) Related pins: /ISTAT
(Note 5) Related pins: All input pins except for pins of Note6
(Note 6) Related pins: XIN,VCOI1

2. AC Characteristics

A. XIN, VCOI (When the pulse is inputted)
(V_{DD} = 5V, V_{SS} = 0, Ta = 25℃, Unless otherwise specified)

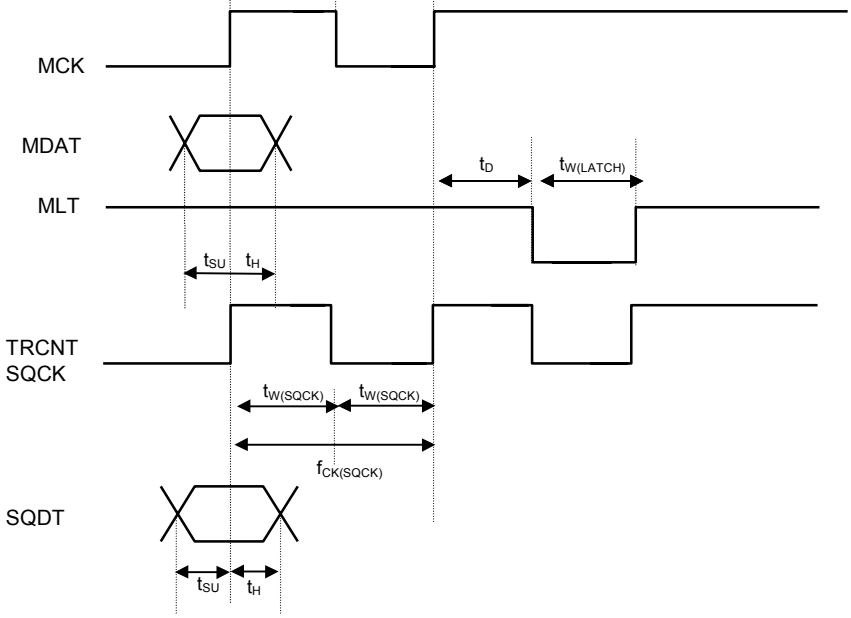
Characteristic	Symbol	Min	Typ	Max	Unit
'H' LEVEL PULSE WIDTH	$t_{w(H)}$	13	-	500	ns
'L' LEVEL PULSE WIDTH	$t_{w(L)}$	13	-	500	ns
PULSE FREQUENCY	t_{CK}	26	-	1000	ns
INPUT 'H' LEVEL	V_{IH}	V_{DD}-1.0	-	-	V
INPUT 'L' LEVEL	V_{IL}	-	-	0.8	V
RISING & FALLING TIME	t_R, t_F	-	-	8	ns



B. MCK, MDAT, MLT, TRCNT

(V_{DD} = 5V, V_{SS} = 0V, Ta = 25℃, unless otherwise specified)

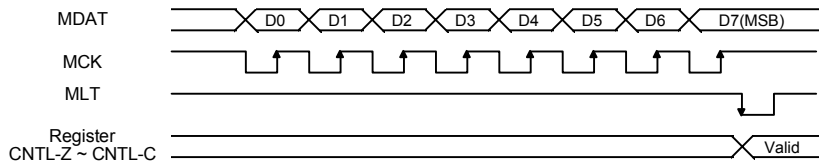
Characteristic	Symbol	Min	Typ	Max	Unit
CLOCK FREQUENCY	f_{CK}	-	-	1	MHz
CLOCK PULSE WIDTH	t_W	300	-	-	ns
SETUP TIME	t_{SU}	300	-	-	ns
HOLD TIME	t_H	300	-	-	ns
DELAY TIME	t_D	300	-	-	ns
LATCH PULSE WIDTH	$t_{W\ (LATCH)}$	300	-	-	ns
TRCNT SQCK FREQUENCY	$f_{CK\ (SQCK)}$	-	-	1	MHz
TRCNT SQCK PULSE WIDTH	$t_{W\ (SQCK)}$	300	-	-	ns



APPLICATION INFORMATION
FUNCTION DESCRIPTION

1. Micom interface

The data inputted from micom is inputted to MDAT and transfered by MCK.
The inputted signal is loaded to control register by means of MLT.
This timing chart is as follows.



(Fig. 1. Micom data input timing chart)

Control Register	Comment	Address D7 ~ D4	Data D3	Data D2	Data D1	Data D0	/ISTAT Pin
CNTL-Z	Data control	1001	ZCMT	HIPD	NCLV	CRCD	HI-Z
CNTL-S	Frame sync protection Attenuation control	1010	FSEM	FSEL	WSEL	ATTM	HI-Z
CNTL-L	Tracking counter Lower 4 bits	1011	TRC3	TRC2	TRC1	TRC0	/Complete
CNTL-U	Tracking counter Upper 4 bits	1100	TRC7	TRC6	TRC5	TRC4	/Count
CNTL-W	CLV control	1101	COM	WB	WP	GAIN	HI-Z
CNTL-C	CLV MODE	1110	CLV MODE				/(Pw≥ 64)

Table 1. Control register and data

1) CNTL-Z REGISTER
It is a register to control zero cross mute of audio data, phase terminal control, phase servo and having or not of CRCF data SQDT.

	DATA	DATA = 0	DATA = 1
ZCMT	D3	Zero cross mute is OFF	Zero cross mute is ON
HIPD	D2	It operates phase normally	The phase becomes “L” to “Hi-Z”
NCLV	D1	Phase Servo is acted by frame sync	Phase servo is controlled by base counter
CRCD	D0	SQDT outputs except for SQOK	SQDT = CRCF when SOS1 = “H”

Table 2.

2) CNTL-S REGISTER
It is a register to control frame sync protection and attenuation

FSEM	FSEL	FRAME
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	CLOCK
0	± 3
1	± 7

ATTM	MUTE	dB
0	0	0
0	1	-∞
1	0	-12
1	1	-12

Table 3.

3) CNTL-L, U REGISTER
After the counter of track that must be counted is inputted from micom , the data is load to tracking counter by CNTL-L, U register.

4) CNTL-W REGISTER
It is a register to control CLV-SERVO

	DATA	DATA = 0	DATA = 1	Comment
COM	D3	XTER/4 and PBFR/4		Phase comparison frequency control during phase mode
WB	D2	XTFR/32	XTFR/16	Bottom hold period control during speed or Hspeed-mode.
WP	D1	XTFR/4	XTFR/2	Peak hold period control during speed Mode
Gain	D0	-12dB	0dB	SMPD gain control during speed or Hspeed-Mode

Table 4.

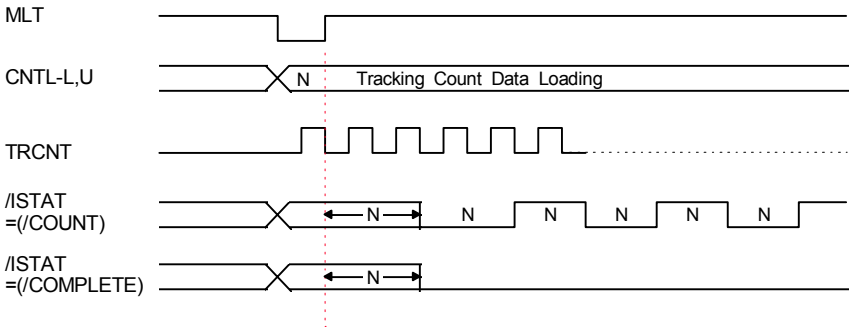
5) CNTL-C REGISTER

MODE	D7-D4	D3-D0	SMPD	SMSD	SMEF	SMON
FORWARD	1110	1000	H	HI-Z	L	H
REVERSE		1010	L	HI-Z	L	H
SPEED		1110	SPEED-MODE	HI-Z	L	H
HSPEED		1100	HSPEED-MODE	HI-Z	L	H
PHASE		1111	PHASE-MODE	PHASE-MODE	HI-Z	H
XPHSP		0110	SPEED, PHASE-MODE	HI-Z or PHZSE-MODE	L or HI-Z	H
STOP		0000	L	HI-Z	L	L
VPHSP		0101	SPEED PHASE-MODE	HI-Z or PHASE-MODE	L or HI-Z	H

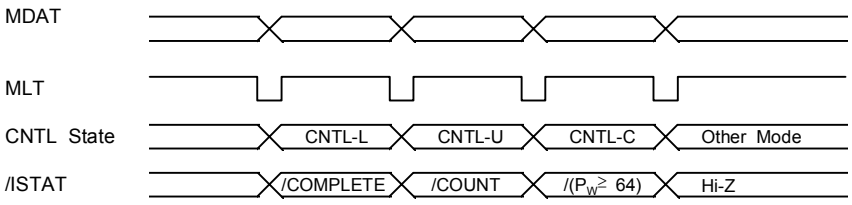
Table 5.

2. Tracking counter block

This block is used to improve track-jump characteristics.
The number of tracks that are to be jumped are loaded into either register CNTL-L or CNTL-U.
After either register CNTL-L or CNTL-U has been loaded, and at the rising edge of the next MLT, the TRCNT pulse count begins.
When n(if register DNTL-L = register = CNTL-U = 0, then n = 256) is loaded into the register, and then at low level for succeeding pulses. When the address is set in DNTL-U, the signal (COUNT) TRCNT is output.
The following is timing chart of tracking counter block. 2n



(Fig 2. Tracking Counter timing chart)



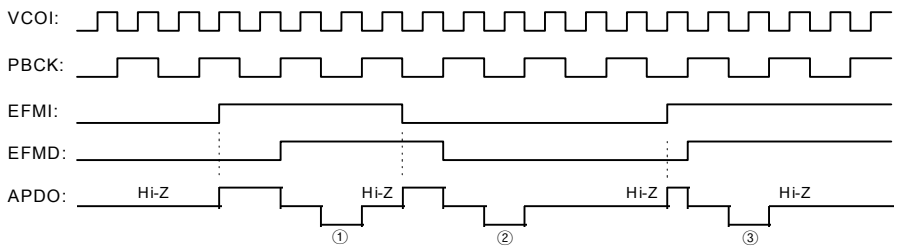
(Fig 3. $\overline{\text{ISTAT}}$ output signal according to CNRL Register)

3. EFM demodulation block

The EFM block consists of EFM demodulator which demodulates EFM data obtained from a disc, EFM phase detector and controller etc.

1) EFM phase detector
As the EFM signal inputted from a disc includes the components of 2.1609MHz, the EFM phase detector uses the bit clock (PBCK) of 4.3218MHz to detect the phase of this signal.
This PBCK detects the phase at the edge of EFM signal and the result is outputted to the APDO terminal.

A. At normal operating



In the case of ① : When the EFM signal is slower than VCO
In the case of ② : When the EFM signal is locked with VCO
In the case of ③ : When the EFM signal is faster than VCO

Fig 4. Timing chart of the EFM phase detector

B. At abnormal operating
If the HIPD of CNTL-Z is "H" and "L" of the LKFS is shorter than 3.5T (a period PBFR is T), the Hi-Z is outputted to APDO terminal as many as "L" and if be over 3.5T, the Hi-Z is outputted as many as 3.5T.

2) EFM demodulator
The 14-bit data through the circuit changes to demodulate 8-bit data.
Demodulated data have two kinds of signal, the one is subcode data and the other is audio data, and that one is inputted into the subcode block and this one is written in the 16K SRAM and performs error correction.

3) Frame sync detector, protector and inserter

A. Frame sync detector
The data consists of frame units, that is, it consists of frame sync, subcode data, PCM data, redundancy data etc. The frame sync is detected in order to maintain the sync.

B. Frame sync protector/inserter
Occasionally, the frame sync is omitted or detected in the place where it doesn't exitst by the effect of error or jitter on a disc.
In these cases, we need to protect or insert the signal.
The window is made by using the WSEL to protect the frame sync.
If the frame sync is inputted to window, it is true data and if isn't inputted, it is ignored.
The width of window is determined by WSEL of CNTL-S register.

If the frame sync is not detected in the frame sync protection window, one frame made internal counter block is inserted sequencely.
When the appointed number of frame is achieved by FSEM, FSEL of CNTL-S register, ULKFS becomes “L” and protection window is ignored.
The frame sync is received absolutely at that time. When the frame sync is received, the ULKFS signal becomes “H” and the frame sync in window is received.

LKFS	ULKFS	COMMENT
1	1	Corresponding with playback frame sync and generated frame sync
0	1	① Out of corresponding with playback frame sync generated frame sync but PBFR sync is detected in the window selected by WSEL. ② Out of corresponding with PBFR Sync and XTFR Sync, and sync is inserted because it isn’t detected in the window selected by WSEL.
0	0	① After insertion as many as the frame decided by FSEM and FSEL of CNTL-S register as frame sync isn’t detected in the window. ② In the case that the PBFR sync is not detected continually after 1.

Table 6.

4) Subcode Block
The 14-bit subcode sync signal (that is S0, S1) is detected in the subcode sync block.
After S0+S1 signal is outputted to S0S1 terminal, and the subcode data is outputted to SDAT terminal when the S0S1 signal is "H"
The subcode data among the data inputted to EFMI terminal is demodulated to 8-bit subcode data (P, Q, R, S, T, U, V,W).
It is synchronized with PBFR signal and it is outputted to SDAT by SBCK clock.
Among the eight subcode data, only Q data is selected and loaded to the eighty shift register by PBFR signal
The result of checking the CRC (Cycle Redundancy Check) of loading data is synchronized with SOS1 rising edge and outputted to SQOK terminal.
If the result of checking is error, "L" is outputted to SQOK terminal and if it is true, "H" is outputted to.
And if the CRCD of CNTL-Z mode is "H", the result of CRC check is outputted to SQDT terminal during from S0S1, "H" to SOCK following edge .

The following is the timing chart of subcode block

1) At SQEN = “L”: SDAT, SQDT, S0S1, SQOK, VCOI timing Chart.

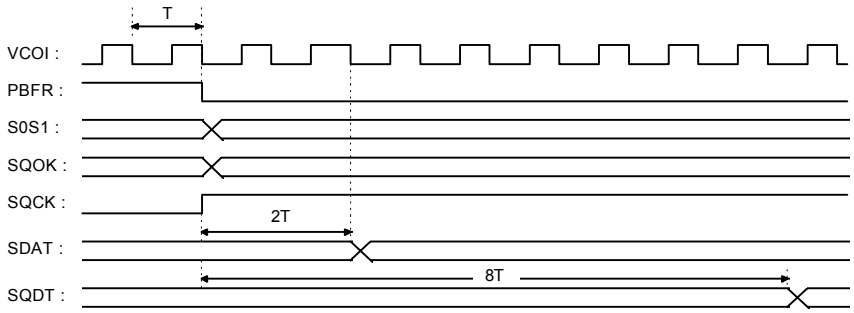


Fig 5. Subcode-Q Timing Chart 1.

2) At SQEN = “L”: SQOK, SQDT, SOS1 timing Chart

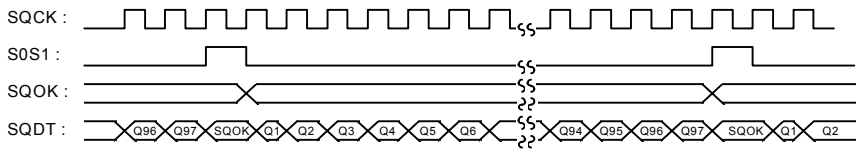


Fig 6. Subcode-Q timing chart 2.

3) At SQEN = "H": SQCK, SQDT, SOS1, SQCK Timing chart

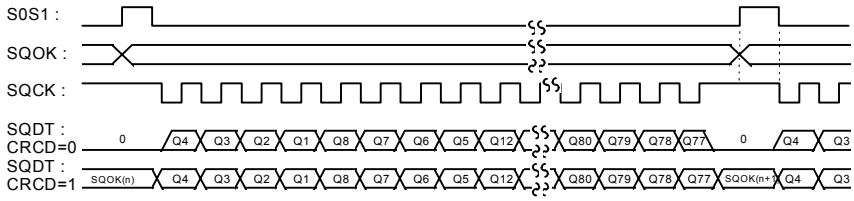


Fig 7. Subcode-Q timing chart 3.

Comment : If the SQOK of the subcode Q data is “H”, the subcode data is outputted to SQDT according to SQCK signal.
If the SQOK is “L”, it is outputted to SQDT with “L”.

4)VCOI, SDAT, SBCK Timing chart.

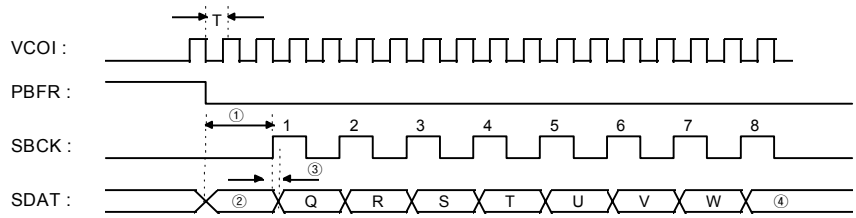


Fig 8. Timing chart of subcode data output

① : After PBFR becomes falling edge, SBCK becomes “L” during about 10μ sec.
② : If S0S1 is “L”, subcode P is outputted. And if “H”, S0S1 is outputted.
③ : If a period of VCOI is “T”, the width of ③ is 4T~6T.
④ : If the pulse inputted to the SBCK terminal be over seven, subcode data (P, Q, R, S, T, U, V, W) is repeated.

4. ECC (Error Comrrection Code) block
The function of ECC block is to recover damaged data to some extent when data on a disc is damaged.
By using CIRC (Crossed-interleave Reed-Solomon Code), C1, (32, 28) and C2 (28, 24) error are corrected.
ECC is performed by the unit of one symbol of eight bits. In correcting C1, a C1 pointer is generated, and in correcting C2, a C2 pointer is generated.
C1, C2 pointer send error information or the data which ECC is given.
After correcting C2, against uncorrectable data, Error data is sent to display by outputting a C2 flag.
The C2FL signal is handled in the interpolator by using the signal of C2F1 and C2F2.

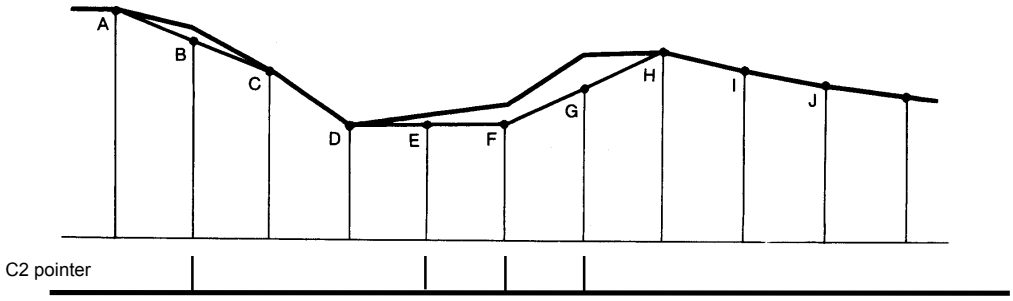
C1F1	C1F2	C1, C2 ERROR Status	C2F1	C2F2	C2FL
0	0	NO ERROR	0	0	0
0	1	SINGLE ERROR CORRECTION	0	1	0
1	0	DOUBLE ERROR CORRECTION	1	0	0
1	1	IRRETRIEVABLE ERROR	1	1	1

Table 9.

C1F1, C1F2: The error correct status is outputed by C1 decoder.
C2F1, C2F2: The error correct status is outputed by C2 decoder.
C2FL: In the case that the error can’t be corrected by C2 decoder, becomes “H”, and the reverse case becomes “L”.

5. Interpolator/Mute block

1) Interpolator
When a burst error occurs on a disc, sometimes the data can't be corrected even if a ECC process is performed.
The interpolator block revises data by using a C2 pointer outputed through the ECC block.
The data inputted to a data bus is inputted to the left and right channel, respectively, in the order of C2 pointer, lower 8-bit, and upper 8-bit.
A pre-hold method is taken when a C2 pointer is "H" continuously.
In case of the occurrence of a single error, an average interpolation method is carried out with the range of the data before and after an error happens.
When a check against a checked cycle is "L", R-CH data is outputted. L-CH data is outputted when the check is "H".



$B = \frac{A + C}{2}$; AVERAGE INTERPOLATION

F = E = D ; PREVIOUS DATA HOLD

$G = \frac{F + H}{2}$; AVERAGE INTERPOLATION

Fig 9. Interpolation.

2). Mute and Attenuation
By using a mute terminal and the ATTM signal of the CNTL-S register, audio data is muted or attenuated.
There are two kinds of mute: zero-cross muting and muting

A. Zero-cross muting
The audio data is muted, after ZCMT of CNTL-Z register goes to "H", and in case that mute is "H" and the upper 6 bits of audio data become all "L" or "H".

B. Muting
The audio data is muted when ZCMT of the CNTL-Z register is "L" and mute terminal is "H".

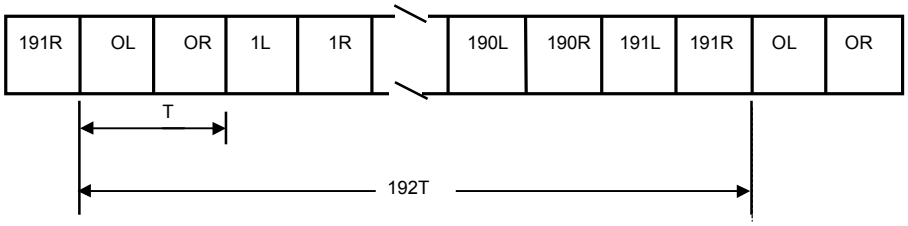
C. Attenuation
The signal attenuation is occured by ATTM of the CNTL-S register and mute signal as following.

ATTM	MUTE	Degree of Attenuation
0	0	0dB
0	1	-∞ dB
1	0	-12dB
1	1	-12dB

Table 8.

6. Digital audio output Block
The 2-channel, 16-bit data is connected and outputted serially to other digital system by the digital audio interface format.

1) Digital audio interface format for CD



OL: L-CH format included block sync preamble
1L ~ 191L: L-CH format included L-CH sync preamble
OR : R-CH format included R-CH sync preamble

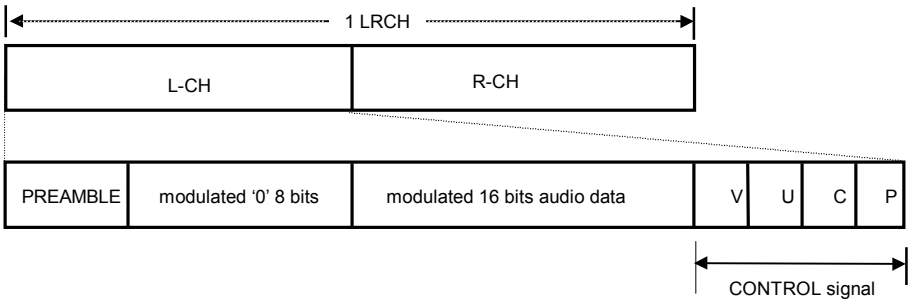


Fig 10. Digital audio out format.

A. Preamble

It is used to discriminated against the block sync of data and L/R-channel of data.

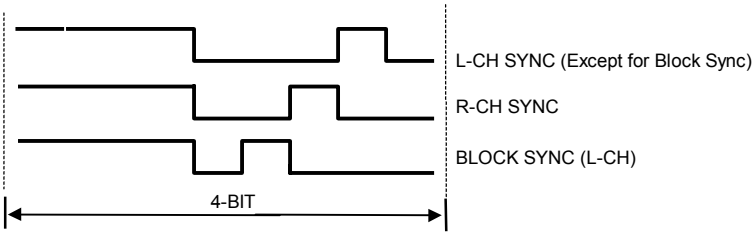


Fig 11. Preamble Signal.

B. Control signal
① Validity bit: It is indicated that the error of 16-bit audio data exists, or doesn't ("H" error, "L": Valid data)
② User definable bit: Subcode data input.

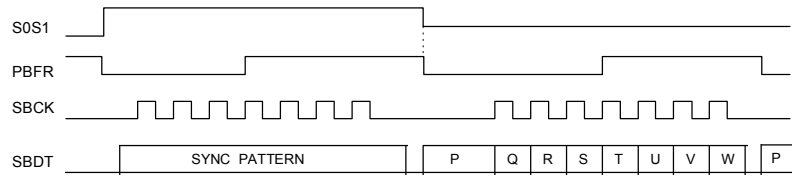


Fig 12. Timing chart of digital audio out.

③ Channel status bit: Output a high position information of 4-bit of subcode Q indicate the number of channel, pre-em-phasisand copy etc. Indicatae CDP categpry.

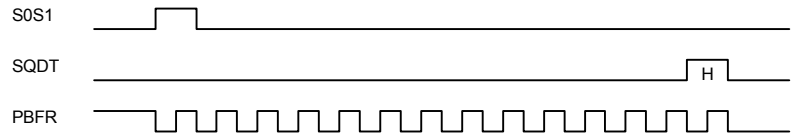


Fig 13. Timing chart of channel status data output.

④ parity bit: Making even parity

7. CLV Servo block
The CNTL-C register is selected to control CLV (Constant Linear Velocity) servo by the data inputted from micom In the CNTL-C register, the CLV servo action mode is appointed by the data inputed form Micom to control the spindle motor.

1) Forward mode
Output condition in forward mode is that SMPD is “H”, SMSD is “Hi-Z”, SMEF is “L” and SMON is “H”.

2) Reverse mode
Output condition in reverse mode is that SMPD is “L”, SMSD is “Hi-Z”, SMEF is “L” and SMON is “H”.

3) Speed mode
The spindle motor is controlled roughly by speed mode when track jumping or EFM phase is unlocked.
If a period of VCO is “T”, the pulse width of frame sync is 22T.
In case that the signal detected from EFM signal exceed “22T” by noise on the disk... etc., it must be removed.
If not, the right frame sync can’t be detected. In this case, the pulse width of EFM signal is detected by peak hold clock and bottom hold clock.

* Peak hold clock is XTFR/2 or XTFR/4, and bottom hold clock is XTFR/16 or XTFR/32

The detected value is used for syncronized frame signal.
If syncronized frame signal is less than 21T, the SMPD terminal output ‘L’, equal to 22T, output ‘HiZ’, and more than 23T output ‘H’.
If the gain signal of CNTL-W register is ‘L’ the output of SMPD terminal is reduced up to -12 dB. If it is ‘H’, there is no reduction.
Output conditions SMSD = ‘HI-z’, SMEF = ‘L’, SMON = ‘H’

4) Hspeed mode
The rough servo mode, which moves 20,000 tracks in high speed acts between the inside of the CD and outside of it.
The mirror domain of track which havn’t pit is duplicated with 20KHz signal to EFM.
In this case, servo action is to unstable because the peak value of mirror singal which is longer than orginal frame sync signal which is detected. In Hspeed mode, by using the 8.4672/256MHz signal against peak hold and XTFR/16 or XTFR/32 signal against bottom hold, the mirror is removed, and Hspeed servo action be to stable.
Output condition in Hspped mode is that SMSD is ‘Hi-z’,SMEF is ‘L’ SMON is ‘H’.

5) Phase mode
The phase mode is the mode to control the EFM phase. Phase difference between PBFR/4 and XTFR/4 is detected when NCLV or CNTL-Z is ‘L’ and phase difference between Read Base Counter/4 and Write Base Counter/4 detected when NCLV is ‘H’, and the difference is outputed to SMPD.
If a cycle of VCO/2 signal is put as ‘T’ and it is put as ‘WPB’ during a ‘H’ period of PBFR, it outputs ‘H’ to SMSD terminal from the falling edge of PBFR to the (WPB-278T) X 32, and then, outputs ‘L’ to the falling edge of the next.

6) XPHSP mode
The XPHSP mode is the mode used in normal operation
The LKFS signal made from frame sync block is to sampling which period is PBFR. If sampling is ‘H’, phase mode is performed, and if the sampling is eight of ‘L’ continuously, speed mode is performed automatically. Selection of peak hold period in speed mode and selections of bottom hold period and gain in speed/hspeed mode is determined by CNTL-W register

7) VPHSP mode
The VPHSP mode is the mode used for rough servo control. It uses VCO instead of X-tal in the EFM pattern test. When the range of VCO center changes. VCO is easily locked because the rotation of a spindle motor changes in the same direction.

8)Stop mode
The stop mode is used to stop the spindle motor.
Output is that SMPD is ‘L’, SMSD = ‘Hi-Z’ SMEF is ‘L’, and SMON is ‘L’.

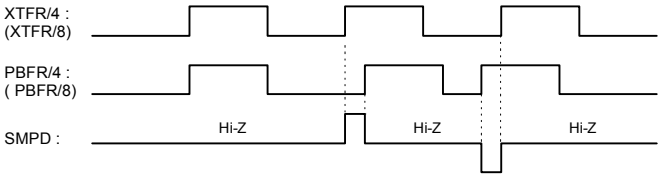
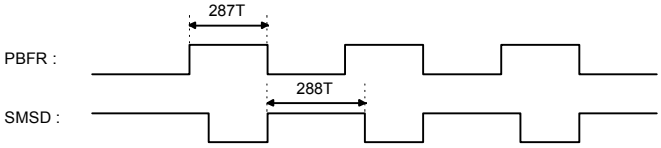
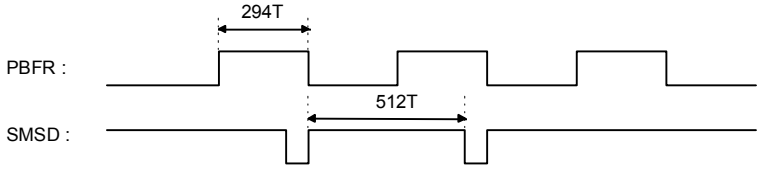


Fig 14. Timing chart of SMPD output.



(a) Timing chart of SMSD output when PBFR is “287T”.



(b) Timing chart of SMSD output when PBFR is “294T”.

Fig. 15. Timing chart of SMSD output at phase mode.

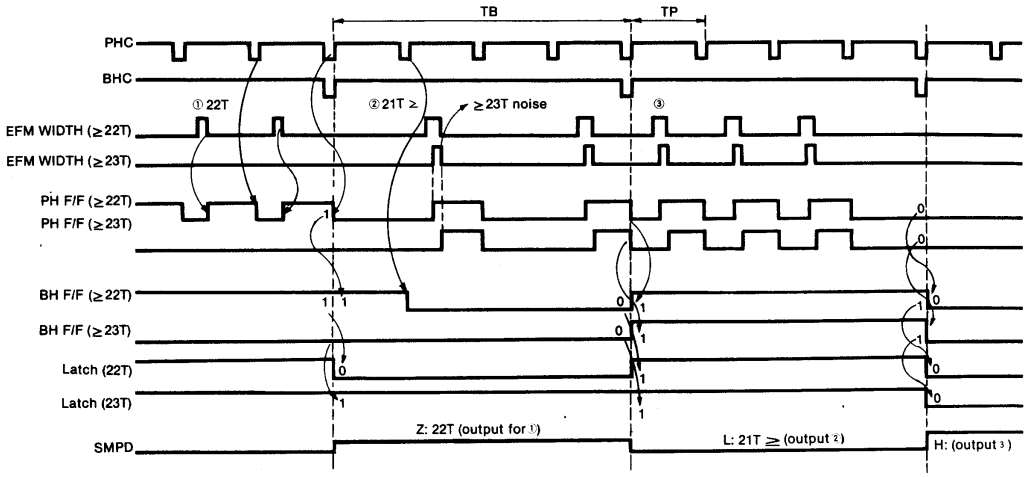


Fig. 16. Timing chart of SMPD output when the gain is “H” in the speed mode.

8. Digital PLL Block

This device contains analog PLL and digital PLL together in order to obtain the stable channel clock for demodulating EFM signal.

The block diagram of digital PLL is as follows.

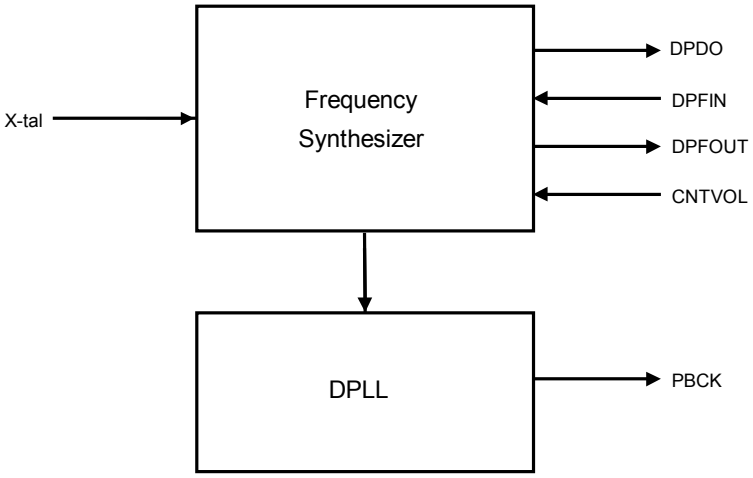
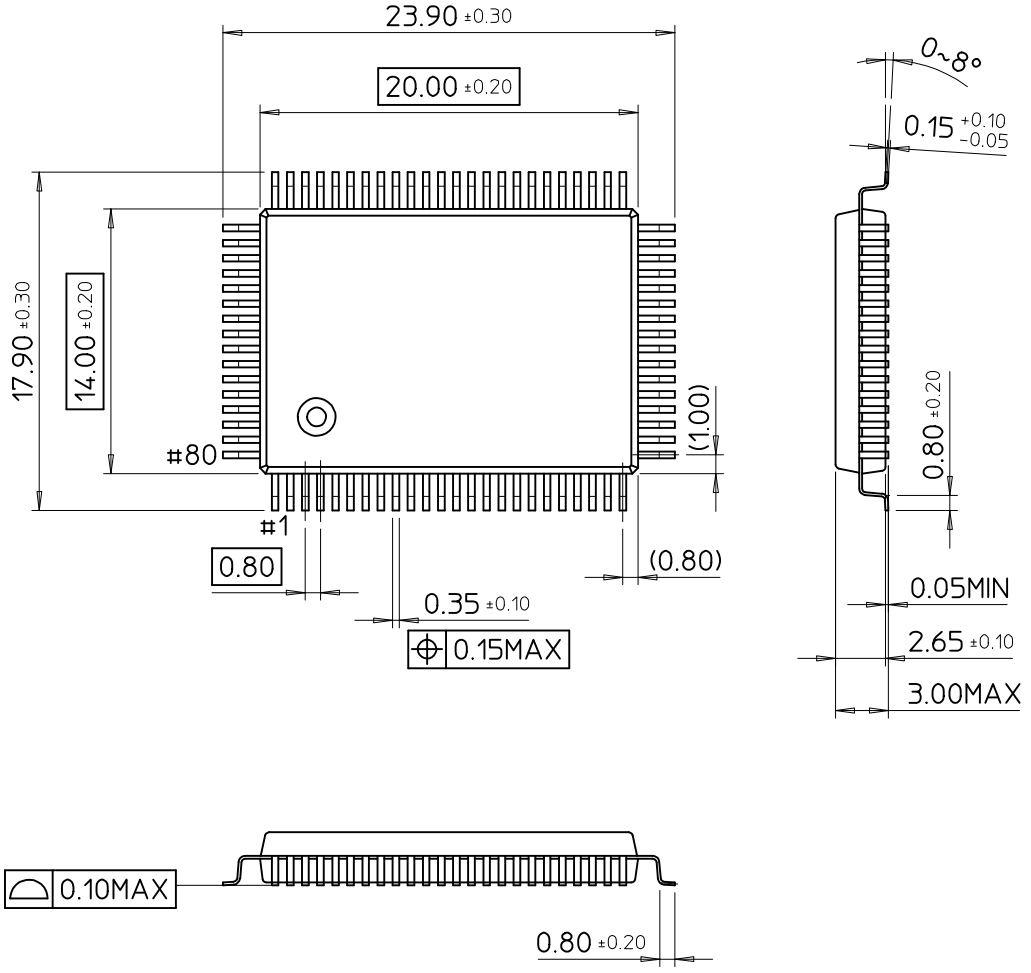


Fig 17. Digital PLL Circuit diagram

80-QFP-1420C

Dimensions in Milimeters



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