KS9284 DIGITAL SIGNAL PROCESSOR

INTRODUCTION

The KS9284 is a CMOS integrated circuit designed for the digital audio signal processor.
It is a monolithic IC that builts in 16K SRAM and DPLL.
It is similar to KS9284 IC but has advanced error correction ability.

FEATURES

- EFM data demodulation
- Built-in frame sync detection, protection and insertion circuit
- C1:2 - Error correction, C2:4 - Erasure correction
- Interpolation
- Subcode data serial output
- CLV servo controller
- Tracking counter
- Micom interface
- Built-in 16K SRAM
- Digital audio output (TX)
- Built-In digital PLL and analog PLL
- Double speed function
- Single power supply: +5V

BLOCK DIAGRAM

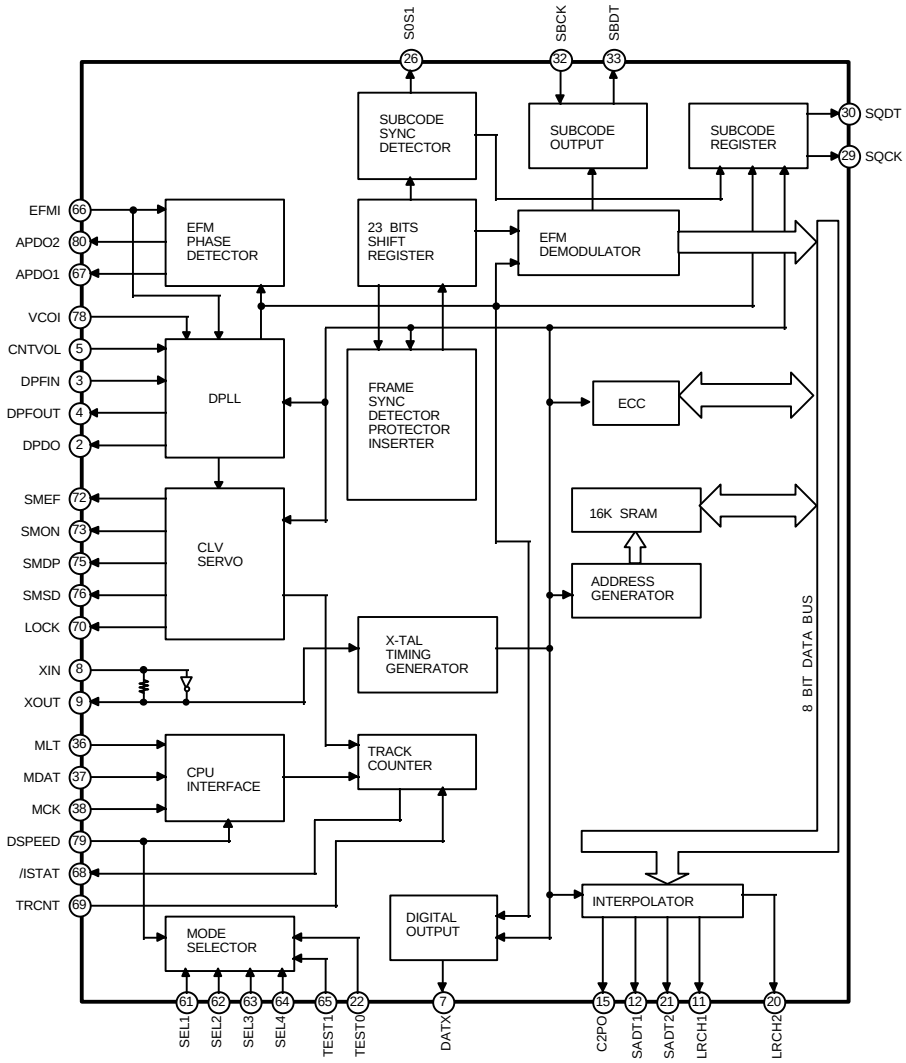


Fig. 1

PIN CONFIGURATION

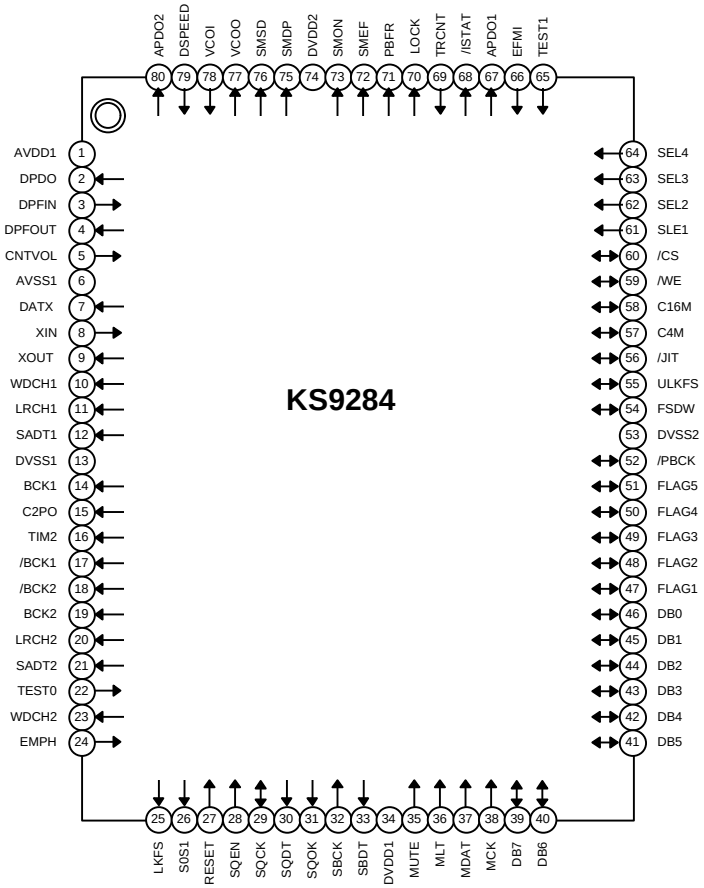


Fig. 2

PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	$AV_{DD}1$	-	Analog supply voltage 1
2	DPDO	O	Charge pump output for master PLL
3	DPFIN	I	Filter input for master PLL
4	DPFOUT	O	Filter output for master PLL
5	CNTVOL	I	VCO control voltage for master PLL
6	$AV_{SS}1$	-	Analog ground 1
7	DATX	O	Digital audio output
8	XIN	I	X-tal oscillator input (16.9344MHz / 33.8688MHz)
9	XOUT	O	X-tal oscillator output
10	WDCH1	O	Word clock of 48 bits/slot
11	LRCH1	O	Channel clock of 48 bits/slot
12	SADT1	O	Serial audio data output with 48 bits/slot
13	DV_{SS1}	-	Digital ground 1
14	BCK1	O	Serial audio data bit clock for 48 bits/slot
15	C2PO	O	C2 pointer for serial audio data
16	TIM2	O	Normal or double speed control output pin
17	/BCK1	O	Inverted clock of BCK1
18	/BCK2	O	Inverted clock of BCK2
19	BCK2	O	Serial audio data bit clock for 64 bits/slot
20	LRCH2	O	Channel clock for 64 bits/slot
21	SADT2	O	Serial audio data output with 64 bits/slot
22	TEST0	I	Test input pin (“L”: normal, “H”: test)
23	WDCH2	O	Word clock of 64 bit/slot
24	EMPH	O	Emphasis/Non-emphasis output (“H” : Emphasis)
25	LKFS	O	The lock status output of frame sync
26	S0S1	O	Output of subcode sync signal (S0 + S1)
27	RESET	I	System reset at “L”
28	SQEN	I	SQCK control input (“L”: internal clock, “H”: external clock)
29	SQCK	I/O	Subcode-Q data bit clock
30	SQDT	O	Subcode-Q data serial output

PIN DESCRIPTION (continued)

Pin No.	Symbol	I/O	Description
31	SQOK	O	The CRC check result signal output of subcode-Q
32	SBCK	I	Subcode data bit clock
33	SBDT	O	Subcode serial data output
34	$DV_{DD}1$	-	Digital supply voltage 1
35	MUTE	I	Mute control input (“H”: Mute ON)
36	MLT	I	Latch signal input from micom
37	MDAT	I	Serial data input from micom
38	MCK	I	Serial data transfering clock input from micom
39	DB7	I/O	Data port 7 for external SRAM (MSB)
40	DB6	I/O	Data port 6 for external SRAM
41	DB5	I/O	Data port 5 for external SRAM
42	DB4	I/O	Data port 4 for external SRAM
43	DB3	I/O	Data port 3 for external SRAM
44	DB2	I/O	Data port 2 for external SRAM
45	DB1	I/O	Data port 1 for external SRAM
46	DB0	I/O	Data port 0 for external SRAM (LSB)
47	FLAG1	I/O	Monitoring output for C1 error correction (RA0)
48	FLAG2	I/O	Monitoring output for C1 error correction (RA1)
49	FLAG3	I/O	Monitoring output for C2 error correction (RA2)
50	FLAG4	I/O	Monitoring output for C2 error correction (RA3)
51	FLAG5	I/O	C2 decoder flag (“H”: when the processing C2 code is impossible correction status /RA4)
52	/PBCK	I/O	VCOI/2 clock (4.3218/8.6436MHz) ; when locked in with EFMI (RA5)
53	$DV_{SS}2$	-	Digital ground 2
54	FSDW	I/O	Unprotected frame sync (RA6)
55	ULKFS	I/O	Frame sync protection status (RA7)
56	/JIT	I/O	RAM overflow and underflow status (RA8)
57	C4M	I/O	4.2336MHz clock output (RA9)
58	C16M	I/O	16.9344MHz clock output (RA10)
59	/WE	I/O	Write enable output to external SRAM
60	/ CS	I/O	Chip select output to external SRAM

PIN DESCRIPTION (continued)

Pin No.	Symbol	I/O	Description
61	SEL1	I	X-tal selection terminal (“L”:16.9344MHz; “H” : 33.8688MHz)
62	SEL2	I	DPLL selection terminal (“L”: DPLL, “H” : APLL)
63	SEL3	I	CD-ROM selection terminal (“L”: CDP, “H” : CD-ROM)
64	SEL4	I	SRAM selection terminal (“L”: internal SRAM, “H” : external SRAM)
65	TEST1	I	Test terminal (“L”: normal, “H”: test)
66	EFMI	I	EFM data input
67	APDO1	O	Charge pump output for analog PLL
68	/ISTAT	O	The internal status output
69	TRCNT	I	Tracking clock input signal
70	LOCK	O	Output signal of LKFS conditions sampled PBFR/16 (If LKFS is “H”, lock is “H”. If the LKFS is sampled “L” at least 8 times by PBFR/16, lock is “L”)
71	PBFR	O	Write frame clock (Lock : 7.35KHz)
72	SMEF	O	LPF time constant control of the spindle servo error signal
73	SMON	O	ON/OFF control signal for spindle servo
74	$DV_{DD}2$	-	Digital supply vlotage 2
75	SMDP	O	Spindle motor driving output (rough control in the speed mode, phase control in the phase mode
76	SMSD	O	Spindle motor (Velocity control in the phase mode)
77	VCOO	O	VCO output
78	VCOI	I	VCO inut (when the state is lock by means of PBFR, it is 8.6436MHz)
79	DSPEED	I	Double speed mode control (“H”: normal speed, “L”: 2-times speed)
80	APDO2	O	Analog PLL charge pump output for double speed mode

(NOTE)
1. PBFR: 7.35KHz Write frame clock produced by data which being reproduced.
2. /PBCK : Channel bit clock of data which being reproduced.
3. /JIT : Display signal of either RAM overflow or underflow for ± 4 frame jitter margin.

ABSOLUTE MAXIMUM RATINGS (Ta = 25 C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 ~ 7.0	V
Input Voltage	V_I	-0.3 ~ 7.0	V
Output Voltage	V_O	-0.3 ~ 7.0	V
Operating Temperature	T_{OPR}	-20 ~ 75	°C
Storage Temperature	T_{STG}	-40 ~ 125	°C

ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{DD} = 5V, V_{SS} = 0V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
"H" Input Voltage1	$V_{IH (1)}$	(Note 1)	$0.7V_{DD}$	-	-	V
"L" Input Voltage1	$V_{IL(1)}$	(Note 1)	-	-	$0.3V_{DD}$	V
"H" Input Voltage2	$V_{IH (2)}$	(Note 2)	$0.8V_{DD}$	-	-	V
"L" Input Voltage2	$V_{IL (2)}$	(Note 2)	-	-	$0.2V_{DD}$	V
"H" Outut Voltage1	$V_{OH (1)}$	I_{OH} = -1mA(Note 3)	V_{DD} - 0.5	-	V_{DD}	V
"L" Output Voltage1	$V_{OL (1)}$	I_{OL} = 1mA(Note 3)	0	-	0.4	V
"H" Outut Voltage2	$V_{OH (2)}$	I_{OH} = -1mA(Note 4)	V_{DD} - 0.5	-	V_{DD}	V
"L" Output Voltage2	$V_{OL (2)}$	I_{OL} = 1mA(Note 4)	0	-	0.4	V
"H" Outut Voltage3	$V_{OH (3)}$	I_{OH} = -1mA(Note 5)	V_{DD} - 0.5	-	V_{DD}	V
"L" Output Voltage3	$V_{OL (3)}$	I_{OL} = 1mA(Note 5)	0	-	0.4	V
Input Leak Current1	I_{LKG1}	V_I = 0 ~ V_{DD}(Note 6)	-5	-	+ 5	µA
Input Leak Current2	I_{LKG2}	V_O = 0 ~ V_{DD}(Note 7)	-10	-	+10	µA
Tri - State Output Leak Current	$I_{O (LKG)}$	V_I = 0 ~ V_{DD}(Note 8)	-5	-	+ 5	µA

(Note 1) Input Voltage1: All input pins
(Note 2) Input Voltage2: All BIDIR pins
(Note 3) Output Voltage1: All output pins
(Note 4) Output Voltage2: All BIDIR pins
(Note 5) Output Voltage 3: All Tri - state output pins
(Note 6) Input Leak Current 1: All input pins except for XIN, VCOI
(Note 7) Input Leak Current 2: XIN, VCOI
(Note 8) Output Leak Current : SMEF, SMDP, SMSD, APDO1, APDO2, DPDO

2. AC Characteristics

A. XIN, VCOI (When the pulse is inputted to)
(V_{DD} = 5V, V_{SS} = 0V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
"H" Level Pulse Width	t_{wH}	13	-	-	ns
"L" Level Pulse Width	t_{wL}	13	-	-	ns
Pulse Frequency	t_{CK}	26	-	-	ns
Input "H" Level	V_{IH}	V_{DD} - 1.0	-	-	V
Input "L" Level	V_{IL}	-	-	0.8	V
Rising & Falling Time	t_R, t_F	-	-	8	ns

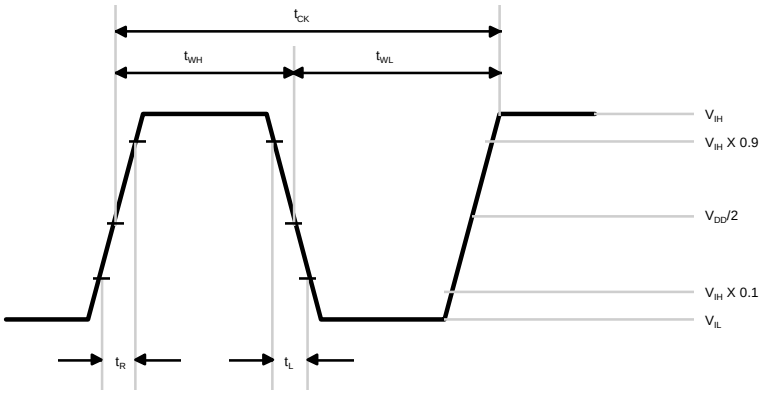


Fig. 3

B. MCK, MDAT, MLT, TRCNT
(V_{DD} = 5V, V_{SS} = 0V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{CK1}	-	-	1	MHz
Clock Pulse Width	t_W	300	-	-	ns
Setup Time	t_{SU}	300	-	-	ns
Hold Time	t_H	300	-	-	ns
Delay Time	t_D	300	-	-	ns
Latch Pulse Width	t_{WCK1}	300	-	-	ns
TRCNT, SQCK Frequency	f_{CK2}	-	-	1	MHz
TRCNT, SQCK Pulse Width	t_{WCK2}	300	-	-	ns

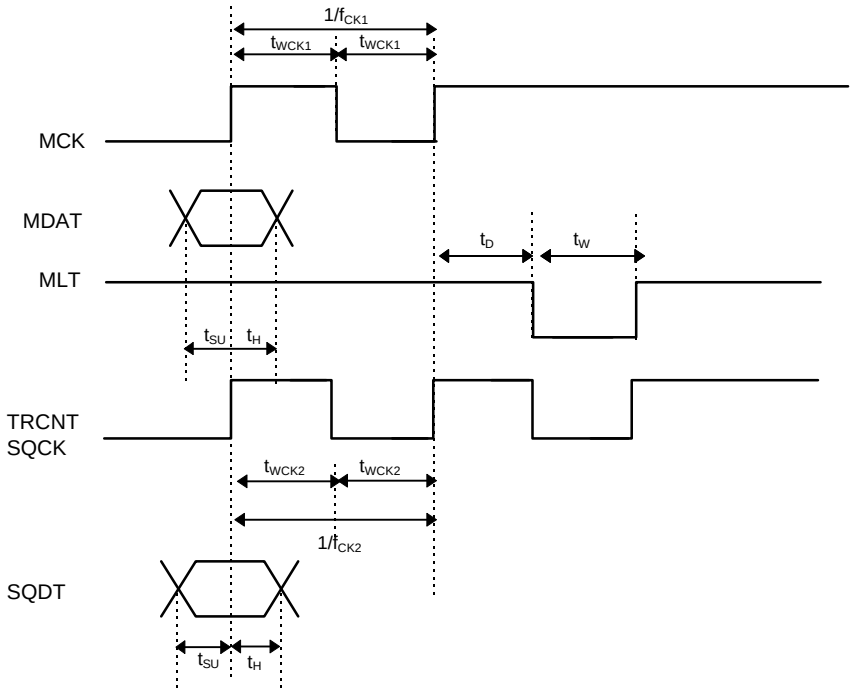


Fig. 4

APPLICATION INFORMATION
FUNCTION DESCRIPTION

1. MICOM INTERFACE BLOCK

The data inputted from micom is inputed to MDAT and transported by MCK.
The inputted signal is loaded to control register by means of MLT.
This timing chart is as follows.

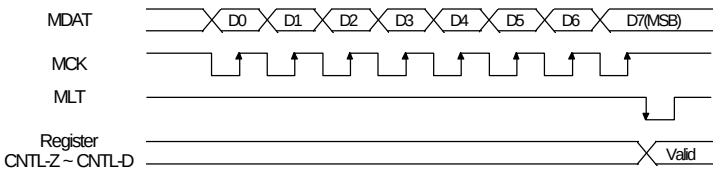


Fig. 5 : Micom data input timing chart

Control Register	Comment	Address D7 ~ D4	Data D3	Data D2	Data D1	Data D0	/ISTAT Terminal
CNTL-Z	Data Control	1001	ZCMT	HIPD	NCLV	CRCQ	HI-Z
CNTL-S	Frame Sync Protection Attenuation Control	1010	FSEM	FSEL	WSEL	ATTM	HI-Z
CNTL-L	Tracking Counter Lower 4 Bits	1011	TRC3	TRC2	TRC1	TRC0	/Complete
CNTL-U	Tracking Counter Upper 4 Bits	1100	TRC7	TRC6	TRC5	TRC4	/Count
CNTL-W	CLV Control	1101	COM	WB	WP	GAIN	HI-Z
CNTL-C	CLV Mode	1110	CLV Mode				/(Pw ≥ 64)
CNTL-D	Double Speed	1111	-	-	DS1	DS2	HI-Z

Table 1. Control register and data

1) CNTL-Z Register
It is a register to control zero cross mute of audio data, phase terminal control, phase servo and having or not CRCF data in SQDT.

	DATA	DATA = 0	DATA = 1
ZCMT	D3	Zero cross mute is OFF	Zero cross mute is ON
HIPD	D2	It operates phase normally	The phase becomes “L” to “Hi-Z”
NCLV	D1	Phase servo is acted by frame sync	Phase servo is controlled by base counter
CRCQ	D0	SQDT output except for SQOK	SQDT = CRCF when S0S1 = “H”

Table 2.

2) CNTL-S Register
It is a register to control frame sync protection and attenuation

FSEM	FSEL	FRAME
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	CLOCK
0	± 3
1	± 7

ATTM	MUTE	dB
0	0	0
0	1	- ∞
1	0	-12
1	1	-12

Table 3.

3) CNTL-L, U Register
After the number of track that must be counted is inputted from micom , the data is loaded to tracking counter by CNTL-L, U register.

4) CNTL-W Register
It is a register to control CLV-servo.

	DATA	**DATA = 0**	**DATA = 1**	**Comment**
COM	D3	XTFR/4 and PBFR/4		Phase comparison frequency control during Phase - mode
WB	D2	XTFR/32	XTFR/16	Bottom hold period control during speed or H.Speed-mode.
WP	D1	XTFR/4	XTFR/2	Peak hold period control during Speed-mode
GAIN	D0	-12dB	0dB	SMDP gain control during Speed or H.Speed-Mode

Table 4.

5) CNTL-C Register

MODE	D7-D4	D3-D0	SMDP	SMSD	SMEF	SMON
FORWARD	1110	1000	H	Hi-Z	L	H
REVERSE		1010	L	Hi-Z	L	H
SPEED		1110	SPEED-MODE	Hi-Z	L	H
HSPEED		1100	HSPEED-MODE	Hi-Z	L	H
PHASE		1111	PHASE-MODE	PHASE-MODE	Hi-Z	H
XPHSP		0110	SPEED, PHASE-MODE	Hi-Z, PHZSE-MODE	L, Hi-Z	H
VPHSP		0101	SPEED PHASE-MODE	Hi-Z, PHASE-MODE	L, Hi-Z	H
STOP		0000	L	Hi-Z	L	L

Table 5.

6) CNTL-D Register
It is a register to control normal speed mode and double speed mode.

MODE	D7-D4	D3-D0	COMMENT
NORMAL	1111	XX00	Normal Speed
DOUBLE		XX11	Double Speed

Table 6.

(NOTE) TRACKING COUNTER
This block is used to improve track-jump characteristics.
The number of track, which must be jumped, is inputted from micom and the operating of count is performed by TRCNT pulse at positive edge of MLT.
If the number of track is loaded into the register and the CNTL-L is selected, the /COMPLETE signal is outputted to /ISTAT terminal, and if the CNTL-U is selected, the /COUNT signal is outputted.
The following is timing chart of tracking counter block.

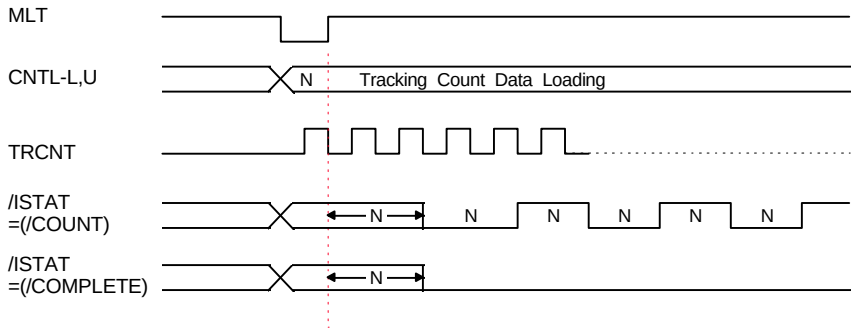


Fig. 6 : Tracking Counter Timing Chart

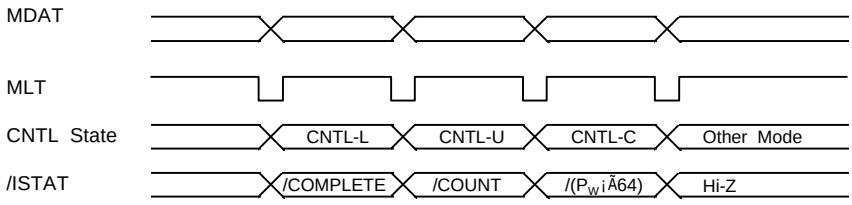
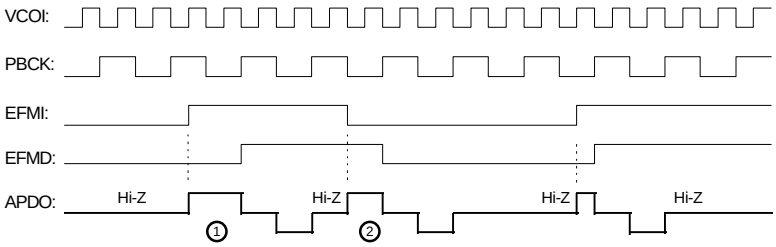


Fig 7. /$\overline{\text{ISTAT}}$ output signal according to CNTRL Register

2. EFM DEMODULATION BLOCK

This block consists of EFM demodulator which demodulates EFM data obtained from a disc, EFM phase detector and controller etc.

1)EFM phase detector
As the EFM signal inputted from a disc includes the components of 2.1609MHz, the EFM phase detector uses the bit clock (/PBCK) of 4.3218MHz, to detect the phase of this signal.
This PBCK detects the phase at the edge of EFM signal and the result is outputted to the APDO1 or APDO2 terminals.


VCOI:
PBCK:
EFMI:
EFMD:
APDO:
Hi-Z
Hi-Z
Hi-Z
Hi-Z
1
2

In these cases, we need to protect or insert the signal.
The window is made by using the WSEL to protect the frame sync.
If the frame sync is inputted to window, it is true data and if isn't inputted, it is ignored.
The width of window is determined by WSEL of CNTL-S register.
If the frame sync is not detected in the frame sync protection window, one sync which made by internal counter block, is inserted sequencely.
When the appointed number of frame is achieved by FSEM, FSEL of CNTL-S register, ULKFS becomes "L" and frame sync protection window is ignored. The frame sync is received absolute at that time. When the frame sync is received, the ULKFS signal becomes "H" and the frame sync window is received.

LKFS	ULKFS	COMMENT
1	1	Corresponding with playback frame sync and generated frame sync
0	1	① Out of corresponding with playback frame sync generated frame sync, but PBFR sync is detected in the window selected by WSEL. ② Out of corresponding with PBFR sync and XTFR sync, and sync is inserted because it isn't detected in the window selected by WSEL.
0	0	① After insertion as many as the frame decided by FSEM and FSEL of CNTL-S register as frame sync isn't detected in the window. ② In case that the PBFR sync is not detected continually after ①.

3 SUBCODE BLOCK
The subcode sync signal (that is S0, S1) is detected in the subcode sync block. After S0 is detected, S1 is detected after one frame.
At that time, the S0 + S1 signal is outputted to S0S1 terminal, and the S0S1 signal is outputted to SBDT terminal when the S0S1 signal is "H".
The subcode data among the data inputted to EFM terminal, is demodulated to 8-bit subcode data (P, Q, R, S, T, U, V, W). It is synchronized with PBFR signal and it is outputted to SBDT by SBCK clock.
Among the eight subcode data, only Q data is selected and loaded to the eighty shift register by PBFR signal.
The result of checking the CRC (Cycle Redundancy Check) of loading data is synchronized with S0S1 positive edge and outputted to SQOK terminal.
If the result of checking is error, "L" is outputted to SQOK terminal and if it is true, "H" is outputted to.
And if the CRCQ of CNTL-Z mode is "H", the result of CRC check is outputted to SQDT terminal during from S0S1, "H" to SQCK negative edge.

The following is the timing chart of subcode block

1) At SQEN = “L”: SBDT, SQDT, S0S1, SQOK, VCOI timing chart.

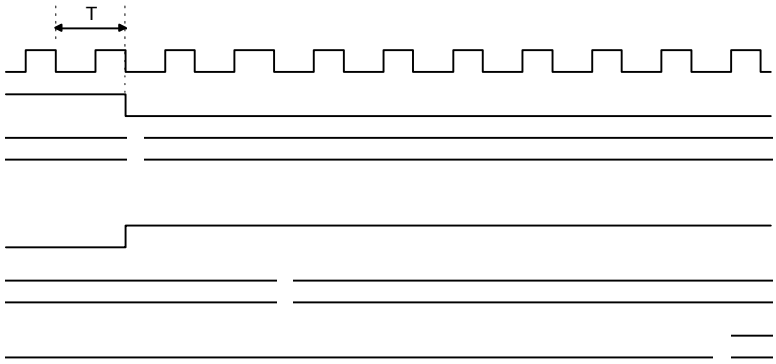


Fig 9. Subcode-Q Timing Chart 1.

2) At SQEN = “L”: SQOK, SQDT, S0S1 timing chart

Fig 10. Subcode-Q timing chart 2.

3) At SQEN = "H": SQOK, SQDT, S0S1, timing chart

Fig 11. Subcode-Q Timing Chart 3.

(Comment) : If the SQOK of the subcode Q data is “H” the subcode data is outputted to SQDT according to SQCK signal.
If the SQOK is “L”, it is outputted to SQDT with “L”.

4)VCOI, SBDT, SBCK timing chart.

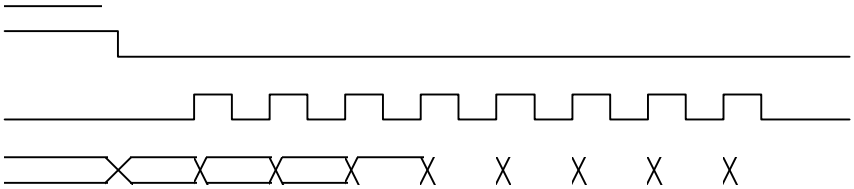


Fig 12. Timing chart of subcode data output)

① : After PBFR becomes negative edge, SBCK becomes “L” during about 10μsec.
② : If S0S1 is “L”, subcode P is outputted. And if “H”, S0S1 is outputted.
③ : If a period of VCOI is “T”, the width of ③ is 4T.
④ : If the pulse inputted to the SBCK terminal be over seven, subcode data (P, Q, R, S, T, U, V, W) is repeated.

4. ECC (Error Comrrection Code) block

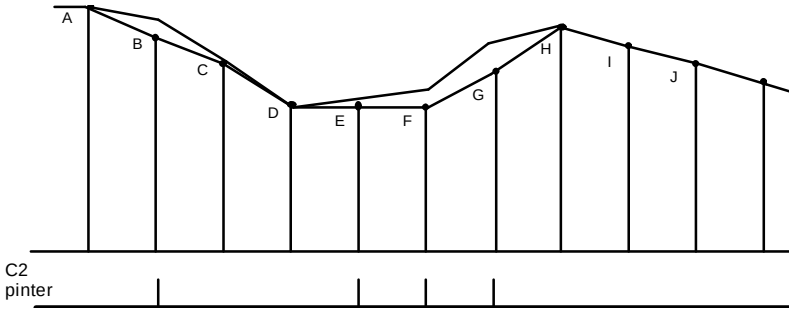
The function of ECC block is to recover damaged data to some extent when data on a disc is damaged.
By using CIRC (Cross Interleaved Reed-Solomon Code), 2-Error correction is performed for C1 (32, 28) and 4-Erasure correction is performed for C2 (28, 24).
ECC is performed by the unit of one symbol of eight bit. In correcting C1, a C1 pointer is generated, and in correcting C2, C2 pointer is generated.
C1, C2 pointers send error information to the data which ECC is given.
After correcting C2, against uncorrectable data, error data is sent to display by outputting a C2 FLAG.
This information data is inputted to interpolator block in order to handle error data.
The monitoring flow for error correction is available through FLAG1 ~ FLAG5 tesrminal.

MODE	FLAG5	FLAG4	FLAG3	FLAG2	FLAG1	REMARK
C1 0,1 error	0	1	1	1	0	
C1 2 error	0	1	1	1	1	
C1 irretrievable error	0	1	1	1	1	
C1 0,1,2 error	0	1	1	1	1	Attenuation
C2 0,1,2,3,4 error	1	1	1	0	1	
C2 irretrievable error 1	1	1	1	1	0	
C2 irretrievable error 2	1	1	1	1	1	C1 point copy 1

Table 8 : The monitoring flow for error correction

5. INTERPOLATION / MUTE BLOCK

1) Interpolator
When a burst error occurs on a disc, sometimes the data can't be corrected even if a ECC process is performed.
The interpolator block revises data by using a C2 pointer outputted through the ECC block.
The data inputted to a data bus is inputted to the left and right channel, respectively, in the order of C2 pointer, lower 8-bit and upper 8-bit.
A pre-hold method is taken when a C2 pointer is "H" continuously.
In case of the of a single error, an everage interpolation method is carried out with the range of the data before and after an error happens.
When LRCH signal during one LRCH cycle is "L", R-CH data is outputted, L-CH data is outputted when the check is "H".



$B = \frac{A + C}{2}$; average interpolation

F= E = D : provious datahold

$G = \frac{F + H}{2}$; average interpolation

Fig 13. Interpolation.

2). Mute and Attenuation
By using a mute terminal and the ATTM signal of the CNTL-S register, audio data is muted or attenuated.
There are two kinds of mute: zero-cross muting and muting

A. zero-cross muting
The audio data is muted, after ZCMT of CNTL-Z register goes to “H”, and in case that mute is “H” and the upper 6 bits of audio data became all “L” or “H”.

B. Muting
The audio data is muted when ZCMT of the CNTL-Z register is “L” and mute terminal is “H”.

C. Attenuation
The signal attenuation is occured by ATTM of the CNTL-Z register and mute signal as following.

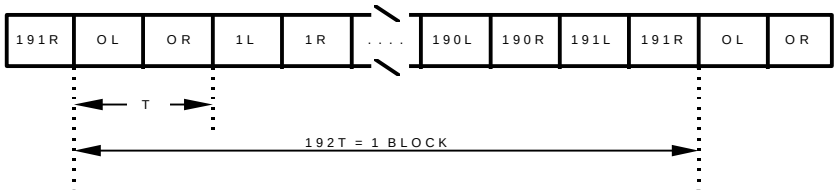
Attm	Mute	Degree of Attenuation
0	0	0dB
0	1	- ∞ dB
1	0	-12dB
1	1	-12dB

Table 9.

6. DIGITAL AUDIO OUT BLOCK

The 2 channel, 16 bits data is connected and outputed serially to other digital system by the digital audio interface format.

<Digital audio interface format for CD>



0L: L-CH format included block sync preamble.
1L ~ 191L: L-CH format included L-CH sync preamble.
0R ~ 191R: R-CH format included R-CH sync preamble.

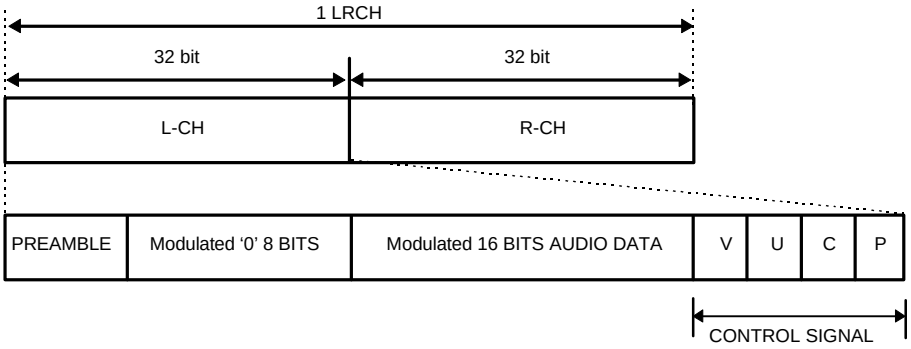


Fig 14. Digital audio out format

A. Preamble

It is used to discriminated against the block sync of data and L/R-channel of data.

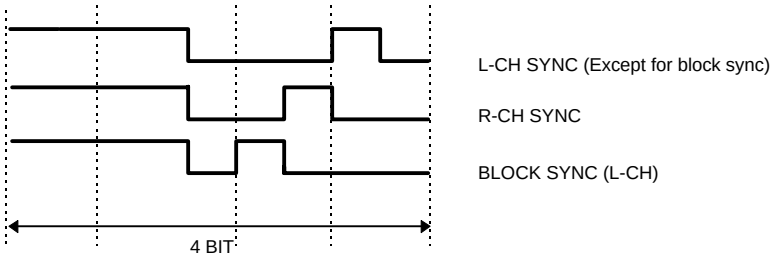


Fig 15. Preamble signal

B. Control signal

① Validity bit: It is indicated that the error of 16-bit audio data exists, or doesn't ("H" : error, "L": valid data)

② User definable bit: Subcode data input.

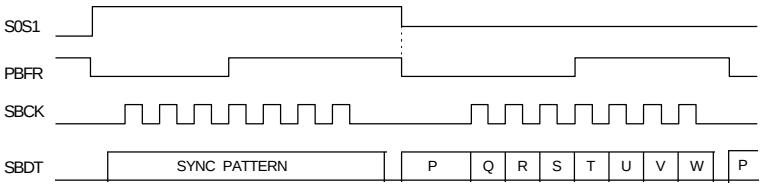


Fig 16. Timing chart of digital audio out

③ Channel status bit: The upper 4-bit of subcode Q indicate the number of channel, pre-em-phasis copy and CDP category, etc.

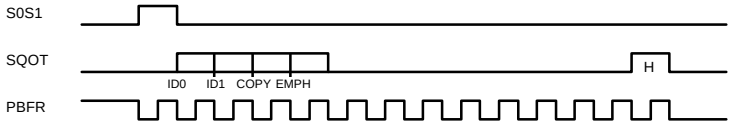


Fig 17. Timing chart of channel status data output

④ Parity bit: Making even parity

7. CLV SERVO BLOCK

The CNTL-C register is selected to control CLV (Constant Linear Velocity) servo by the data inputted from micom. In the CNTL-C register, the CLV servo action mode is appointed by the data inputted from micom to control the spindle motor. In case of double - speed setting, the CNTL-C register has to be selected after CNTL-D register sets, so it is able to detect / (Pw ≥ 64) signal from /ISTAT terminal.

1) Forward Mode
The status of the related output terminals are as follows.

SMDP	SMSD	SMEF	SMON
H	Hi-Z	L	H

2) Reverse Mode
The status of the related output terminals are as follows.

SMDP	SMSD	SMEF	SMON
L	Hi-Z	L	H

3) Speed - Mode
The speed-mode is the mode for the rough control of a spindle motor when a track is jumping or EFM phase is unlocked.
If a period of VCO is “T”, the pulse width of frame sync is “22T”.
In case that the signal detected from EFM signal exceed “22T” by noise on the disc.... etc., it must be removed.
If not, the right frame sync can’t be detected. In this case, the pulse width of EFM signal is detected by peak and bottom hold clock. the peak hold clock is XTFR/2 or XTR/4, and the bottom hold clock is XTFR/16 or XTFR/32.
The detected value is used for syncronized frame signal.
If synchronized frame signal is less than 21T, the SMDP terminal outputs ‘L’, equal to 22T, output ‘HiZ’, and more than 23T, output ‘H’.
If the gain signal of CNTL-W register is ‘L’, the output of SMDP terminal is reduced up to - 12dB. If it is ‘H’, there is no reduction.

4) Hi-Speed-Mode
The rough servo mode, which moves 20,000 tracks in high speed acts between the inside of the CD and outside of it.
The mirror domain of track which havn't pit is duplicated with 20KHz signal to EFM.
In this case, servo action is to unstable because the peak value of mirror singal which is longer than orginal frame sync signal which is detected. In Hi-Speed mode, by using the 8.4672/256MHz signal against peak hold and XTFR/16 or XTFR/32
signal against bottom hold, the mirror is removed, and Hi-Speed servo action be to stable.

SMDP	SMSD	SMEF	SMON
-	Hi-Z	L	H

5) Phase-Mode
The phase-mode is the mode to control the EFM phase. Phase difference between PBFR/4 and XTFR/4 is detected when NCLV of CNTL-Z is 'L' and the difference is outputted to SMDP terminal.
If a cycle of VCO/2 signal is put as 'T' and it is put as '/WP' during a 'H' period of PBFR, it outputs 'H' to SMSD terminal from the falling edge of PBFR to the (/WP-278T) X 32, and then, outputs 'L' to the falling edge of the next.

6) XPHSP-Mode
The XPHSP mode is the mode used in normal operation. It samples a LKFS signal made inthe frame sync block at a cycle of PBFR/16.
If the sampling is 'H', the phase mode is performed, and if the 'L' is sampled continuously 8 times, the speed mode is performed automatically.
The selection of peak hold period of speed mode, and bottom hold period and gain of speed / Hispeed mode is determined by the CNTL-W register.

7) VPHSP-Mode
The VPHSP-mode is the mode used for rough servo control. It uses VCO instead of X-tal in the EFM pattern test. When the range of VCO center changes, VCO is easily locked because the rotation of a spindle motor changes in the same direction.

8) STOP
The stop is the mode used to stop the spindle motor.

SMDP	SMSD	SMEF	SMON
L	Hi-Z	L	L

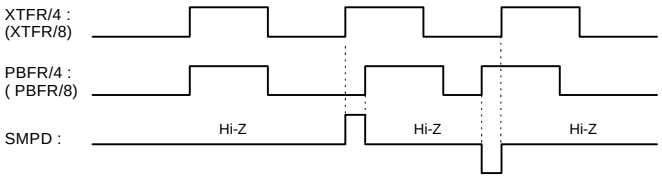
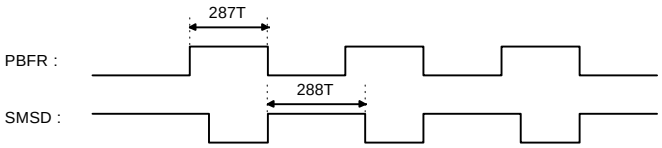
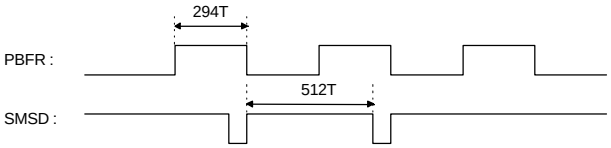


Fig 18. Timing chart SMDP output



(a) Timing chart of SMSD output when PBFR is “287T”



(b) Timing chart of SMSD output when PBFR is “294T”.

Fig. 19: Timing chart of SMSD output at phase mode.

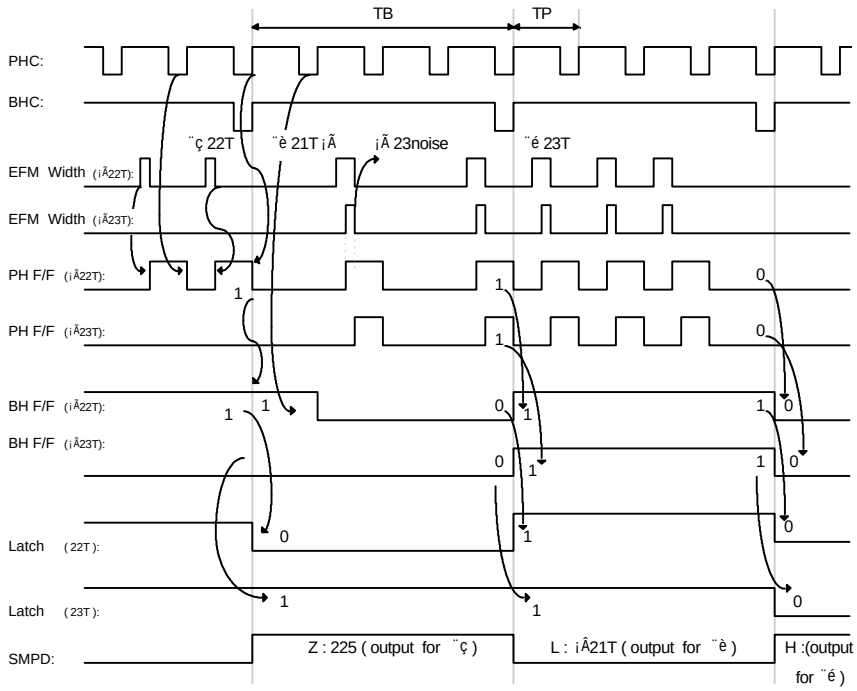


FIG.20 : Timing chart of SMPD output when the gain is "H" in the speed mode

8. DIGITAL PLL BLOCK

This device contains analog PLL and digital PLL together, in order to obtain the stable channel clock for demodulating EFM signal.

The block diagram of digital PLL is as follows.

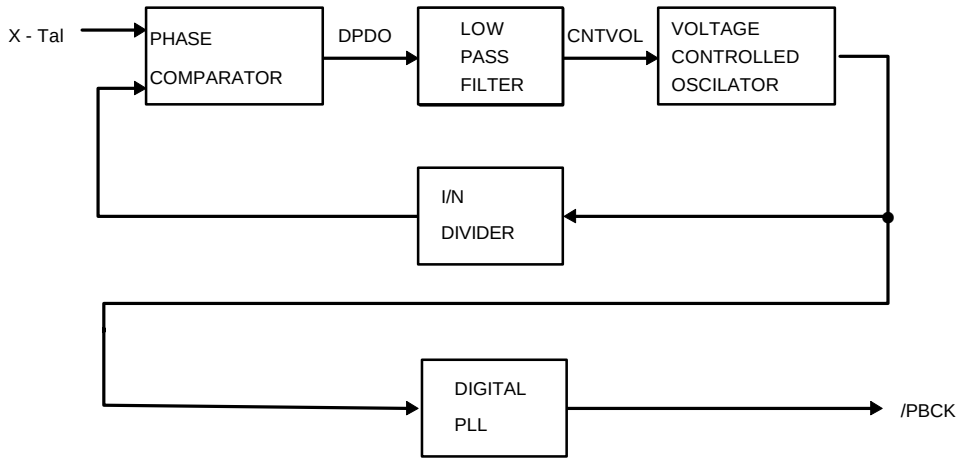


Fig. 21: The application diagram of Digital PLL