SGS-THOMSON MICROELECTRONICS

L6503

HAMMER SOLENOID CONTROLLER

PRELIMINARY DATA

- DRIVES FOUR DARLINGTONS WITH UP TO 2.5 mA DRIVE CURRENT
- FEEDBACK LOOP CONTROLS DARLINGTON CURRENT
- PRESETTABLE CONDUCTION TIME
- LATCHED µC-COMPATIBLE INPUTS
- DIAGNOSTIC CIRCUITRY

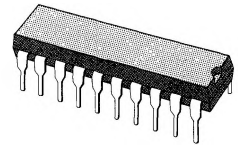
DESCRIPTION

Designed primarily for selenoid driving applications, the L6503 Hammer Solenoid Controller includes all the circuitry needed to control four darlington power devices or a quad darlington array such as the SGS L7180.

The device is controlled by four latched logic inputs, which may be connected directly to a microcomputer chip, plus an analog input which sets the load current. Additionally, the conduction time of the outputs is controlled by a clock input which drives internal timers.

Fault conditions may be detected thanks to diagnostic circuitry which allows the control micro to read (serially) the load current status of the external darlingtons.

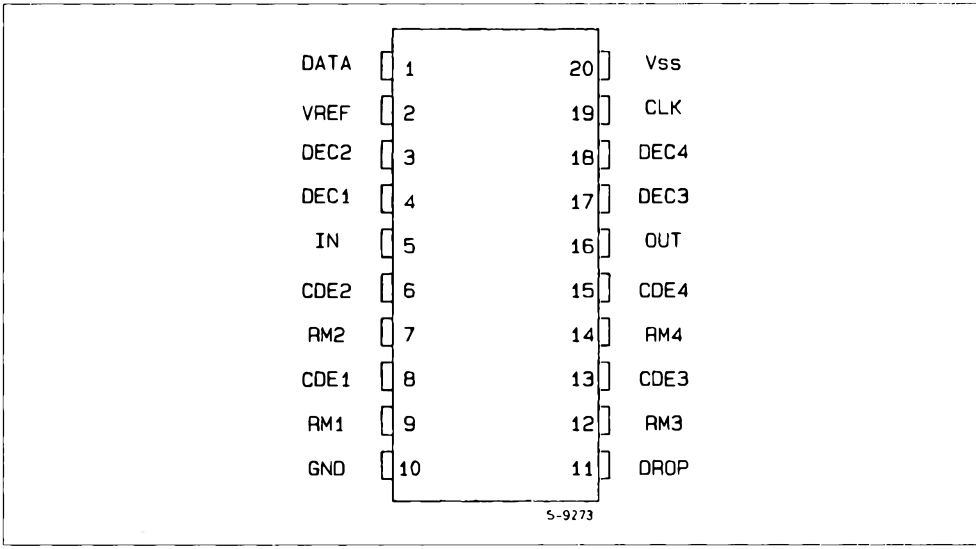
Assembled in a 20-pin DIP package, the L6503 operates on a single 5 V supply and is suitable for computer printers, solenoid valves and similar applications.



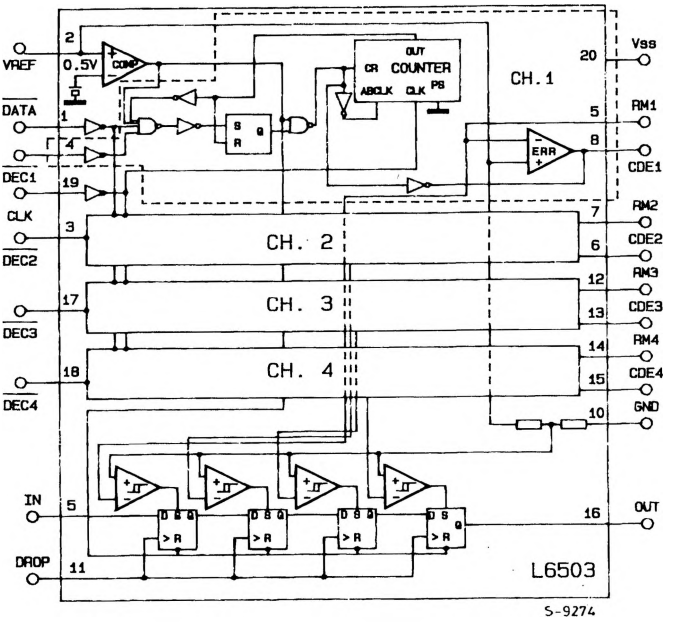
DIP-20 Plastic
(0.4)

ORDER CODE : L6503

CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{ss}	Supply Voltage	7	V
I_{CDE}	Output Current	10	mA
V_i	Input Voltage (for analog and logic inputs)	0 to V_{ss} – 0.5	V
T_{op}	Operating Temperature	0 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

PIN FUNCTIONS DESCRIPTION

N°	Name	Function
1	$\overline{DATA}$	Latches control command into the four inputs DEC1-DEC4 on the high-low transition.
2	V_{ref}	Analog reference input which sets the load current for all four channels ; when lower than 0.5 V resets the logic circuitry.
3	$\overline{DEC2}$	Data input for channel 2. Data is latched on the high-low transition of the DATA input.
4	$\overline{DEC1}$	Data Input for Channel 1.
5	IN	Input for diagnostic shift register used to cascade several device.
6	CDE2	Channel 2 output (connect to base ofdarlington). Up to 2.5 mA drive.
7	RM2	Feedback input from sensing resistor of channel 2 darlington.
8	CDE1	Channel 1 Output .
9	RM1	Feedback input for channel 1 sense resistor .
10	GND	Ground.
11	DROP	Clock Input for Diagnostic Register.
12	RM3	Feedback input for channel 3 sense resistor.
13	CDE3	Channel 3 Output.
14	RM4	Feedback input for channel 4 sense resistor.
15	CDE4	Channel 4 Output.
16	OUT	Output of Diagnostic Register.
17	$\overline{DEC3}$	Input for Channel 3.
18	$\overline{DEC4}$	Input for Channel 4.
19	CLK	Input for clock signal which sets conduction time for all four channels. $T_{on} = 128/f_{CLK}$.
20	V_{ss}	5 V Supply Input Voltage.

FUNCTIONAL DESCRIPTION

The L6503 Hammer Solenoid Controller is designed to control a quad darlington array, such as the SGS-THOMSON L7180, in solenoid driving applications.

Compatible with 5 V microcomputer and peripheral chips, the L6503 is controlled by four logic inputs - one per channel ($\overline{DEC1} - \overline{DEC4}$) - which are latched by a high-low transition on the DATA input.

When one of the channels is activated the corresponding darlington is driven, with up to 2.5 mA drive current. The conduction period is determined by the frequency applied to the CLK input which clocks the 7-bit timer in each channel. The conduction time is therefore 128/fCLK. Typically the CLK frequency will be of the order of 100KHz but the L6503's internal logic will operate at any clock rate within the range of practical conduction times.

During the conduction period the load current is controlled by feedback from a sense resistor in the darlington's emitter and set by the voltage applied to the V_{ref} input. The current depends on both the values of V_{ref} and the sensing resistor :
$I = V_{ref}/R_{sense}$.

The control microcomputer may verify correct operation of the complete drive subsystem thanks to a diagnostic circuit in the L6503. A four bit PISO shift register in the device monitors the feedback signals from the four output darlingtons and may be read serially after each command to check that the loads were driven.

Typically, this register, clocked by the DROP input, will be read a short time after each drive command has been latched into the device.

The input of this register (IN) is available externally so that multiple devices may be cascaded.

ELECTRICAL CHARACTERISTICS (V_{SS} = 5 V , T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ss}	Supply Voltage	T_j = 0 to 70 °C	4.75	5	5.25	V
I_{ss}	Total Supply Current	I_{CDE} = 2 mA All Channels On		75	90	mA
V_{REF}	Input Voltage Reference		1		2.4	V
V_{REF}	Reset Logic Function		0.3		0.65	V
I_{REF}	Input BIAS Reference Current	V_{REF} = 0 to 2.4 V			– 5	µA
V_i	Input Voltage (pin 1, 3, 4, 5, 11, 17, 18, 19)	V_{iL}			0.4	V
		V_{iH}	2.7			
V_{out}	Output Logic Voltage (pin 16)	V_{OL} I_{OUT} = + 1.6 mA			0.4	V
		V_{OH} I_{OUT} = – 100 µA	2.7			
I_b	Input Bias Current (pin 1, 3, 4, 5, 11, 17, 18, 19)	V_{IL}			– 100	µA
		V_{IH}			± 10	
I_b	Input Bias Current (pin 7, 9, 12, 14)	1 ≤ V_{RM} ≤ 2.4 V			– 100	µA
I_{CDE}	Output Current (pin 6, 8, 13, 15)	V_{OUT} = V_{SS} – 0.5 V	2.5			mA
	Output Voltage Range (pin 6, 8, 13, 15)	V_{OL}			0.2	V
		V_{OH}	V_{ss} – 0.5			
	Error Amplifier Input Offset Voltage	1 V ≤ V_{REF} ≤ 2.4 V			± 10	mV

TIMING SECTION

	Data Ability Time t		160			ns
	Data to CDE Delay Time t1 (1)	V_{RM} = 0 V		0.8	1.5	µs
	Clock to CDE Delay Time t2 (1)	V_{RM} = 0 V		7	10	µs
	Reset Time t3		1.9			µs
	Reset to CDE Delay Time t4 (1)				1.3	µ s
	Clock Frequency				100	KHz
	Low Level Clock State t5 (1)		500			ns
	RM to OUT Delay Time t6 (1)				3	µs
	Drop Frequency				500	KHz
	Low Level Drop State t7		500			ns
	Reset to Output Delay Time t8 (1)				1.3	µs
	Drop to in Delay•Time t9 (1)				1.0	µs

(1) 100% Tested

Figure 1 : Application Diagram.

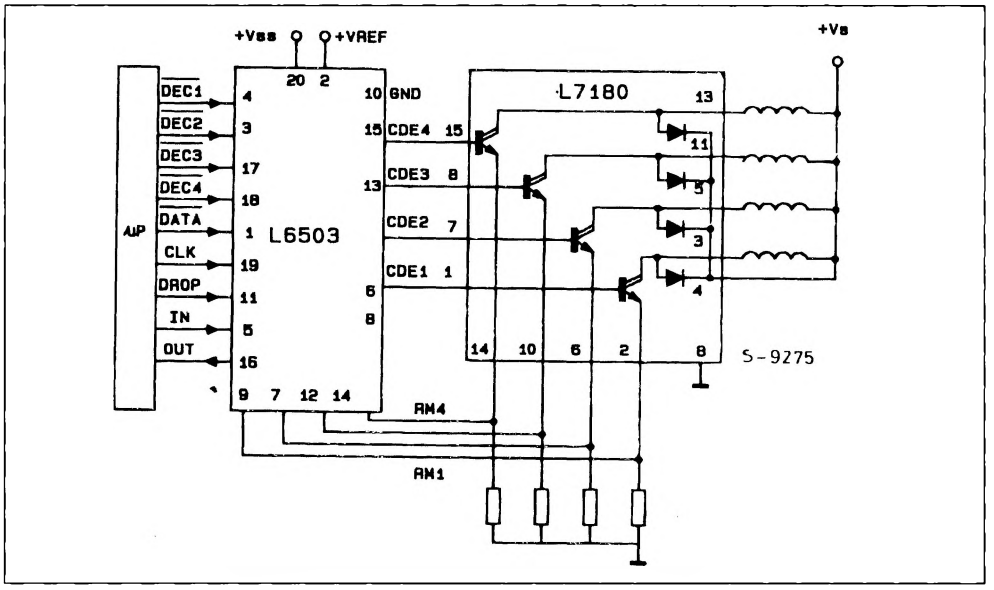


Figure 2 : Timing Diagram.