

400.774

J-FET INPUT SINGLE OPERATIONAL AMPLIFIERS

- REPLACE HYBRID AND MODULE FET OP AMPS. RUGGED J-FETs ALLOW BLOW-OUT FREE HANDLING COMPARED WITH MOSFET INPUT DEVICES
- EXCELLENT FOR LOW NOISE APPLICATIONS USING EITHER HIGH OR LOW SOURCE IMPEDANCE VERY LOW I/F CORNER
- OFFSET VOLTAGE ADJUST DOES NOT DEGRADE DRIFT OR COMMON-MODE REJECTION AS IN MOST MONOLITHIC AMPLIFIERS
- NEW OUTPUT STAGE ALLOWS USE OF LARGE CAPACITIVE LOADS (10 000 pF) WITHOUT STABILITY PROBLEMS
- INTERNAL COMPENSATION AND LARGE DIFFERENTIAL INPUT VOLTAGE CAPABILITY

TYPICAL APPLICATIONS

- PRECISION HIGH SPEED INTEGRATORS
- FAST D/A AND A/D CONVERTERS
- HIGH IMPEDANCE BUFFERS
- WIDEBAND, LOW NOISE, LOW DRIFT AMPLIFIERS
- LOGARITHMIC AMPLIFIERS
- PHOTOCCELL AMPLIFIES
- SAMPLE AND HOLD CIRCUITS

DESCRIPTION

These circuits are monolithic J-FET input operational amplifiers incorporating well matched high voltage J-FETs on the same chip with standard bipolar transistors.

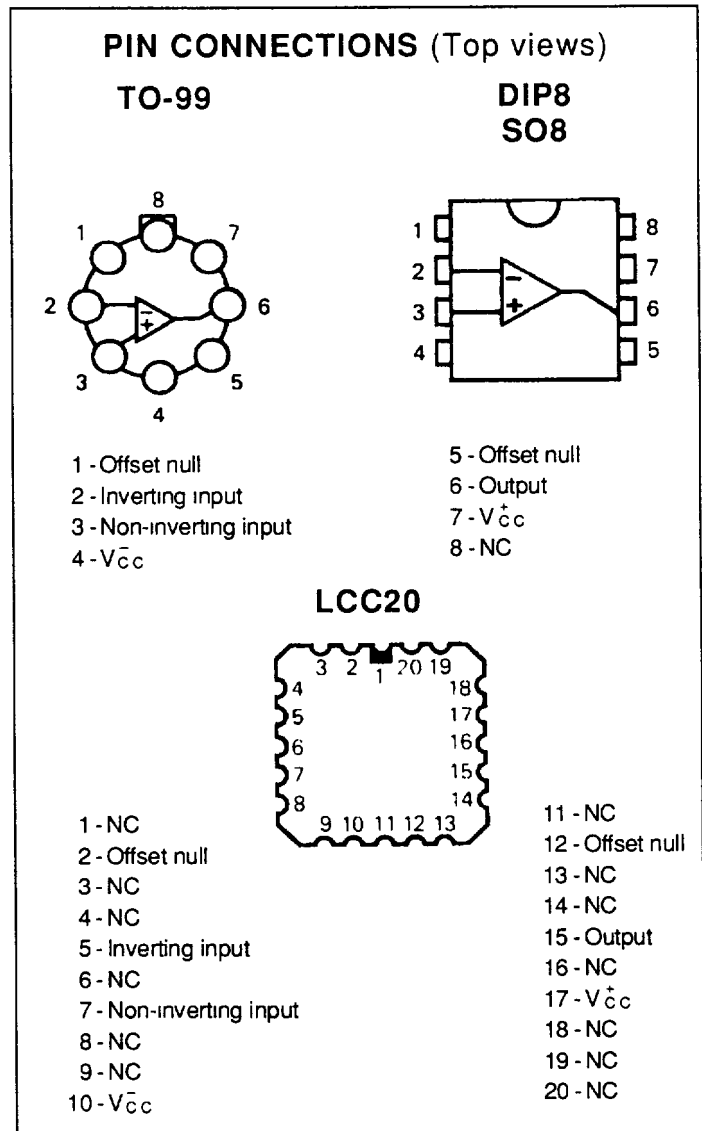
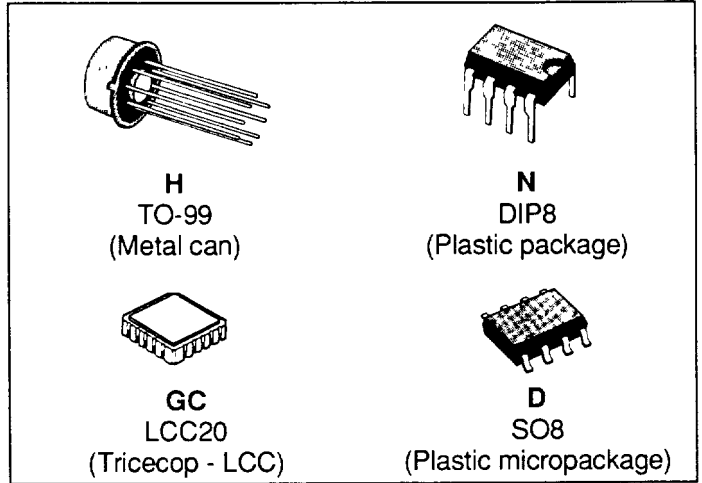
These amplifiers feature low input bias and offset currents, low input offset voltage and input offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection.

The devices are also designed for high, slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low I/f noise corner.

ORDER CODES

Part Number	Temperature Range	Package			
		N	D	H	GC
LF355./LF356, LF357, LF255/LF256	0 °C to + 70 °C	•	•		
LF257	- 40 °C to + 105 °C	•	•		
LF155/LF156 LF157	- 55 °C to + 125 °C	•		•	•

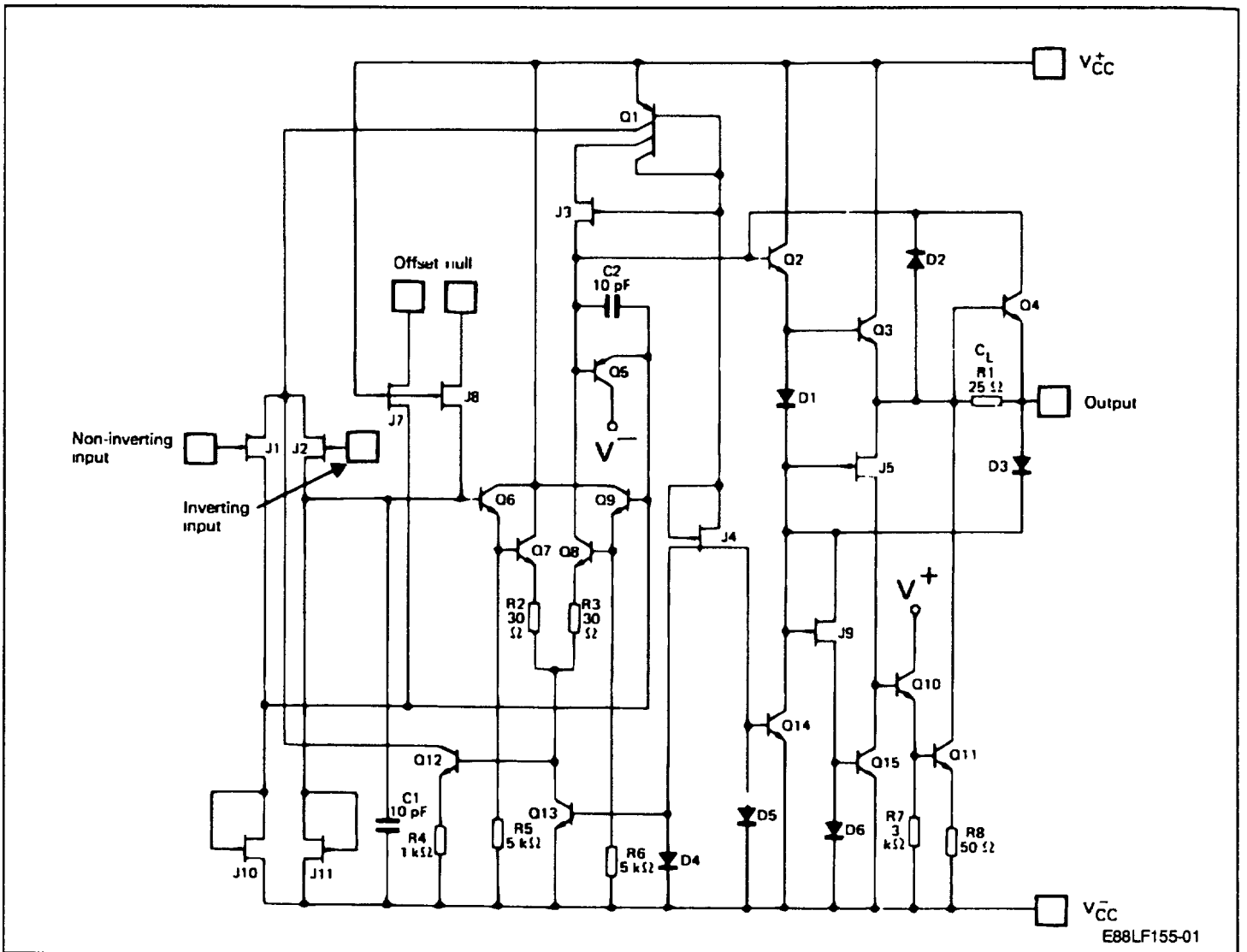
Note . Hi-Rel versions available
Examples : LF355 N, LF155 H



MAXIMUM RATINGS

Symbol	Parameter	LF355, A LF356, A LF357, A	LF255 LF256 LF257	LF155, A LF156, A LF157, A	Unit
V _{CC}	Supply Voltage	± 18	± 22	± 22	V
V _{ID}	Differential Input Voltage	± 30	± 40	± 40	V
V _I	Input Voltage (note 2)	± 16	± 20	± 20	V
	Output Short-circuit Duration	Continuous	Continuous	Continuous	
P _{tot}	Power Dissipation	500	570	670	mW
T _{oper}	Operating Free-air, Temperature Range	0 to + 70	- 40 to + 105	- 55 to + 125	°C
T _{stg}	Storage Temperature Range	- 65 to + 150	- 65 to + 150	- 65 to + 150	°C

SCHEMATIC DIAGRAM



Case	Offset Null	Inverting Input	Non-Inverting Input	V _{CC} ⁻	V _{CC} ⁺	Output	N.C.
DIP8 SO8	1, 5	2	3	4	7	6	8
LCC20	2, 12	5	7	10	17	15	*

* LCC20 : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

LF155, LF156, LF157 : - 55 °C ≤ T_{amb} ≤ + 125 °C, ± 15V ≤ V_{CC} ≤ ± 20V (note 3)

LF155A, LF156A, LF157A : - 55 °C ≤ T_{amb} ≤ + 125 °C, ± 15V ≤ V_{CC} ≤ ± 20V (note 3)

LF255, LF256, LF257 : - 40 °C ≤ T_{amb} ≤ + 105 °C, ± 15V ≤ V_{CC} ≤ ± 20V (note 3)

(Unless otherwise specified).

Symbol	Parameter	LF155, LF156, LF157 LF255, LF256, LF257			LF155A, 156A, 157A			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V _{IO}	Input Offset Voltage (R _S = 50 Ω) T _{amb} = + 25 °C T _{min} ≤ T _{amb} ≤ T _{max} LF155, LF156, LF157 LF255, LF256, LF257		3	5 7 6.5		1	2 2.5	mV
I _{IO}	Input Offset Current (note 5) T _j = + 25 °C T _j ≤ T _{max} LF155, LF156, LF157 LF255, LF156, LF257		3	20 20 1		3	10 10	pA nA
I _{IB}	Input Bias Current (note 5) T _j = + 25 °C T _j ≤ T _{max} LF155, LF156, LF157 LF255, LF256, LF257		30	100 50 5		30	50 25	pA nA
A _{VO}	Large Signal Voltage Gain (V _{CC} = ± 15 V, V _{OPP} = ± 10 V, R _L = 20 KΩ) T _{amb} = + 25 °C T _{min} ≤ T _{amb} ≤ T _{max}	50 25	200		50 25	200		V/mV
SVR	Supply Voltage Rejection Ratio (note 6)	85	100		85	100		dB
I _{CC}	Supply Current (V _{CC} = ± 15 V, T _{amb} = + 25 °C) LF155, LF255 LF156, LF256 LF157, LF257		2 5 5	4 7 7		2 5 5	4 7 7	mA
α V _{IO}	Temperature Coefficient of Input Offset Voltage (R _S = 50 Ω) - Note 4		5			3	5	μV/°C
αV _{IO} /V _{IO}	Change in Average Temperature Coefficient with V _{IO} adjust R _S = 50 Ω		0.5			0.5		μV/°C per mV
V _I	Input Voltage Range (V _{CC} = ± 15 V)	± 11	± 15.1 - 12		± 11	± 15.1 - 12		V
CMR	Common-mode Rejection Ratio	85	100		85	100		dB
V _{OPP}	Output Voltage Swing (V _{CC} = ± 15 V) R _L = 10 KΩ R _L = 2 KΩ	± 12 ± 10	± 13 ± 12		± 12 ± 10	± 13 ± 12		V
GB _p	Gain-bandwidth Product (V _{CC} = + 15 V, T _{amb} = + 25 °C) LF155, LF255 LF156, LF256 LF157, LF257		2.5 5 20		4 15	2.5 4.5 20		MHz
S _{VO}	Slew Rate (V _{CC} = ± 15 V, T _{amb} = + 25 °C) A _V = 1 LF155, LF255 LF156, LF256 A _V = 5 LF157, LF257	7.5 30	5 12 50		3 10 40	5 12 50		V/μs
R _I	Input Resistance (T _j = + 25 °C)		10 ¹²			10 ¹²		Ω
C _I	Input Capacitance (V _{CC} = ± 15 V, T _{amb} = + 25 °C)		3			3		pF
V _n	Equivalent Input Noise Voltage (V _{CC} = ± 15 V, T _{amb} = + 25 °C, R _S = 100 Ω) f = 1000 Hz LF155 LF255 LF156, LF157 LF256, LF257 f = 100 Hz LF155 LF255 LF156, LF157 LF256, LF257		25 20 12 15 20 25 12 15			20 15 25 15		nV/√Hz
I _n	Equivalent Input Noise Current (V _{CC} = ± 15 V, T _{amb} = + 25 °C, f = 100 Hz or f = 1000 Hz)		0.01			0.01		pA/√Hz
t _s	Settling Time (V _{CC} = ± 15 V, T _{amb} = + 25 °C) - Note 7 LF155, LF255 LF156, LF256 LF157, LF257		4			1.5 4		1.5

ELECTRICAL CHARACTERISTICS

LF355, LF356, LF357 : 0 °C ≤ T_{amb} ≤ + 70 °C, V_{CC} = ± 15V

LF355A, LF356A, LF357A : 0 °C ≤ T_{amb} ≤ + 70 °C, ± 15V ≤ V_{CC} ≤ ± 18V (note 3)
(Unless otherwise specified).

Symbol	Parameter	LF355, LF356, LF357			LF355A, 356A, 357A			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V _{IO}	Input Offset Voltage (R _S = 50 Ω) T _{amb} = + 25 °C T _{min} ≤ T _{amb} ≤ T _{max}		3	10 13		1	2 2.3	mV
I _{IO}	Input Offset Current (note 5) T _J = + 25 °C T _J ≤ + 70 °C		3	50 2		3	10 1	pA nA
I _{IB}	Input Bias Current (note 5) T _J = + 25 °C T _J = + 70 °C		30	200 8		30	50 5	pA nA
A _{VD}	Large Signal Voltage Gain (V _{CC} = ± 15 V, V _{OPP} = ± 10 V, R _L = 2 KΩ) T _{amb} = + 25 °C T _{min} ≤ T _{amb} ≤ T _{max}	25 15	200		50 25	200		V/mV
SVR	Supply Voltage Rejection Ratio (note 6)	80	100		85	100		dB
I _{CC}	Supply Current (V _{CC} = ± 15 V, T _{amb} = + 25 °C) LF355 LF356, LF357		2 5	4 10		2 5	4 10	mA
α V _{IO}	Temperature Coefficient of Input Offset Voltage (R _S = 50 Ω) - Note 4		5			3	5	μV/°C
αV _{IO} /V _{IO}	Change in Average Temperature Coefficient with V _{IO} Adjust R _S = 50 Ω		0.5			0.5		μV/°C per mV
V _I	Input Voltage Range (V _{CC} = ± 15 V)	± 10	± 15.1 - 12		± 11	± 15.1 - 12		V
CMR	Common-mode Rejection Ratio	85	100		85	100		dB
V _{OPP}	Output Voltage Swing (V _{CC} = ± 15 V) R _L = 10 KΩ R _L = 2 KΩ	± 12 ± 10	± 13 ± 12		± 12 ± 10	± 13 ± 12		V
GB _p	Gain-bandwidth Product (V _{CC} = ± 15 V, T _{amb} = + 25 °C) LF355 LF356 LF357		2.5 5 20		4 15	2.5 4.5 20		MHz
S _{VO}	Slew Rate (V _{CC} = ± 15 V, T _{amb} = + 25 °C) A _V = 1 LF355 LF356 LF357 A _V = 5		5 12 50		3 10 40	5 12 50		V/μs
R _I	Input Resistance (T _J = + 25 °C)		10 ¹²			10 ¹²		Ω
C _I	Input Capacitance (V _{CC} = ± 15 V, T _{amb} = + 25 °C)		3			3		pF
V _n	Equivalent Input Noise Voltage (V _{CC} = ± 15 V, T _{amb} = + 25 °C, R _S = 100Ω) f = 1000 Hz LF355 LF356, LF357 f = 100 Hz LF355 LF356, LF357		20 12 25 15			20 12 25 15		nV/√Hz
I _n	Equivalent Input Noise Current (V _{CC} = ± 15 V, T _{amb} = + 25 °C, f = 100 Hz or f = 1000 Hz)		0.01			0.01		pA/√Hz
t _s	Settling Time (V _{CC} = ± 15 V, T _{amb} = + 25 °C) Note 7 LF355 LF356, LF357		4 1.5			4 1.5		μs

- Notes :**
- 1 The CB package must be derated based on a thermal resistance of 150 °C/W junction ambient or 45 °C/W junction to case, for the DIP package, the device must be derated based on thermal resistance of 175 °C/W junction to ambient.
 2. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage
 - 3 For the LF155, A, LF156, A, LF157, A these specifications apply for ± 15 ≤ V_{CC} ≤ ± 20 V, - 55 °C ≤ T_{amb} ≤ + 125 °C and T_{high} = + 125 °C unless otherwise stated.
For the LF255, A, LF256, A, LF257, A these specifications apply for ± 15 V ≤ V_{CC} ≤ ± 20 V, - 40 °C ≤ T_{amb} ≤ + 105 °C and T_{high} = + 105 °C unless otherwise stated.
For the LF355, A, LF356, A, LF357, A these specifications apply for ± 15 V ≤ V_{CC} ≤ ± 20 V, 0 °C ≤ T_{amb} ≤ + 70 °C and T_{high} = + 70 °C, unless otherwise stated

- Notes :**
- 4 The temperature coefficient of the adjusted input offset voltage changes only a small amount (0.5 $\mu\text{V}/^\circ\text{C}$ typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.
 - 5 The input bias currents are junction leakage currents which approximately double for every 10 $^\circ\text{C}$ increase in the junction temperature T_j . Due to limited production test time, the input bias current measured is correlated to junction temperature. In a normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, $P_{\text{tot}} T_j = T_{\text{amb}} + R_{\text{th(j-a)}} \times P_{\text{tot}}$ where $R_{\text{th(j-a)}}$ is the thermal resistance from junction to ambient. Use of a heatsink is recommended if input currents are to be kept to a minimum.
 - 6 Supply voltage rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.
 - 7 Settling time is defined here, for a unity gain inverter connection using 2 k Ω resistors for the LF155, LF156 series. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01 % of its final value from the time a 10 V step input is applied to the inverter. For the LF157 series $A_v = -5$, the feedback resistor from output to input is 2 k Ω and the output step is 10 V.

APPLICATION HINTS

The LF155, LF156, LF157 series are op amps with J-FET input devices. These JFETs have large reverse breakdown voltages from gate to source or drain eliminating the need of clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase of input currents. The maximum differential input voltage is independent of the supply voltage. However, neither of the negative input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes

reversed in polarity or that the unit is not inadvertently metallised backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

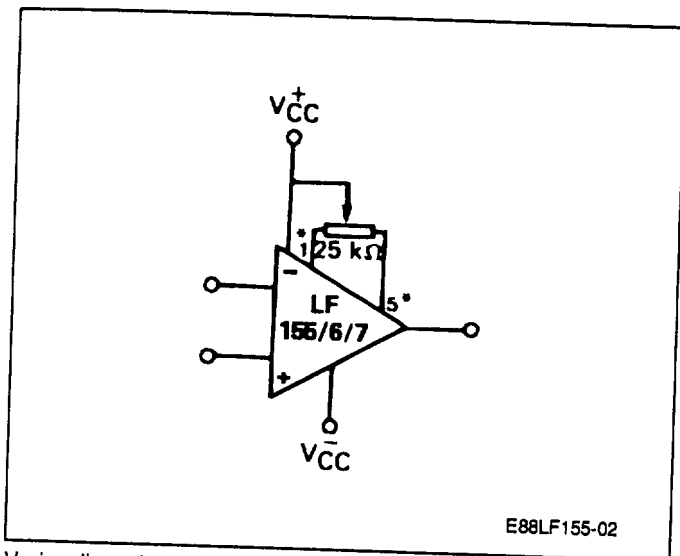
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltages.

As with most amplifiers, care should be taken with lead dress, components placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of that added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

TYPICAL CIRCUITS

V_{IO} ADJUSTMENT

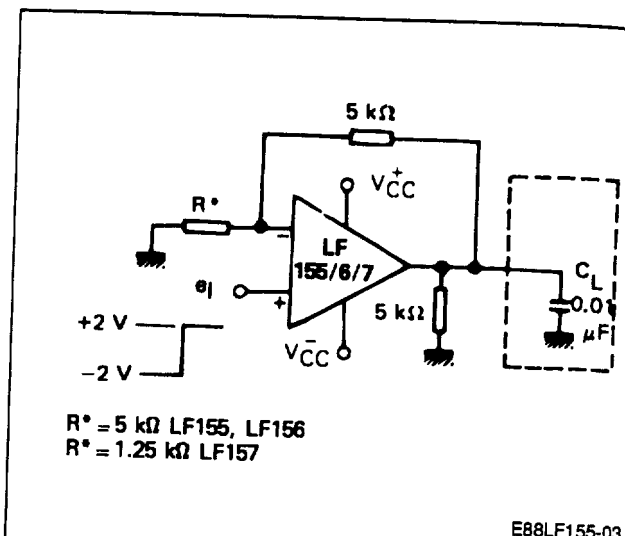


E88LF155-02

V_{IO} is adjusted with a 25 kΩ potentiometer. The potentiometer wiper is connected to V_{CC}

* CB-11, CB-98 pin configuration.

DRIVING CAPACITIVE LOADS



R* = 5 kΩ LF155, LF156
R* = 1.25 kΩ LF157

E88LF155-03

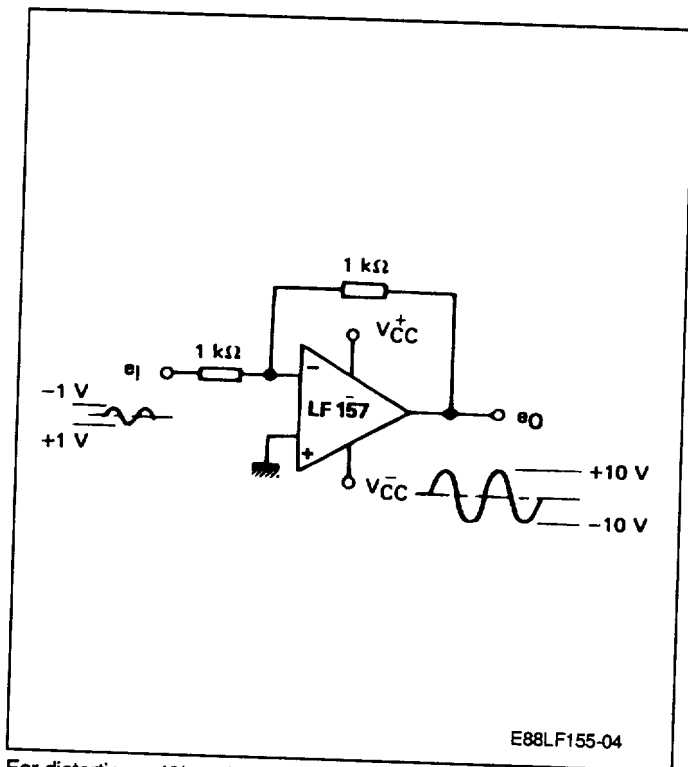
Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability.

C_{L(max)} = 0.01 μF

Overshoot ≤ 20%

Settling time (t_s) = 5 μs

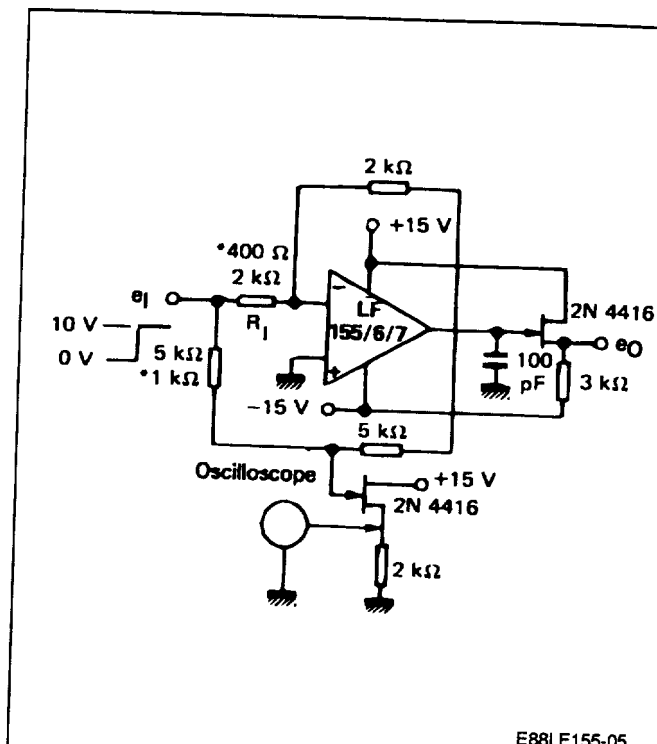
LARGE POWER BW AMPLIFIER



E88LF155-04

For distortion < 1% and a 20 V_{PP} V_O swing, power bandwidth is : 500 kHz.

SETTLING TIME TEST CIRCUIT

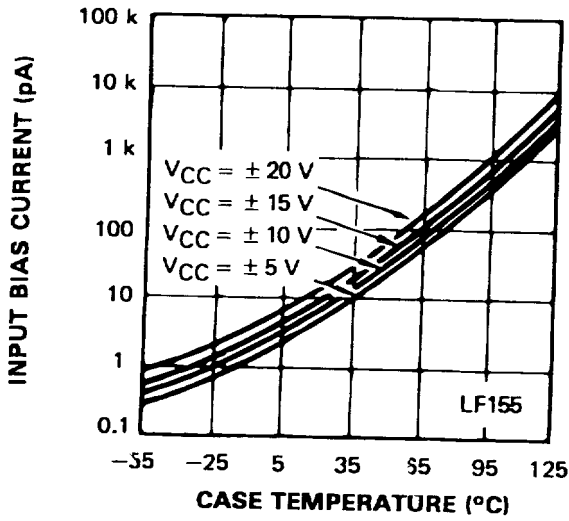


E88LF155-05

Settling time is tested with the LF155, LF156 connected as unity gain converter R₁ = 2 kΩ and LF157 connected for A_v = -5, R₁ = 0.4 kΩ.

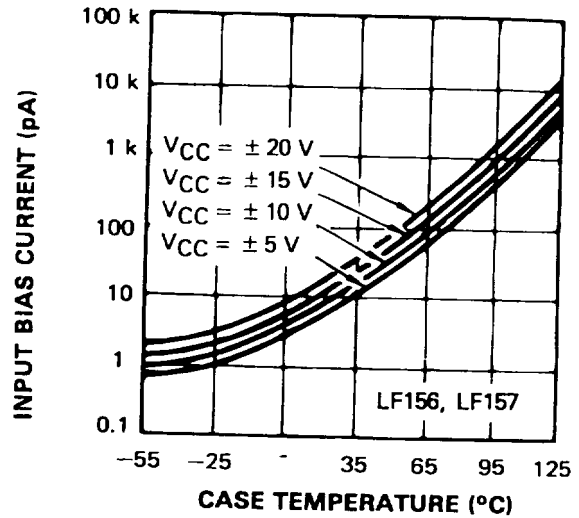
TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT



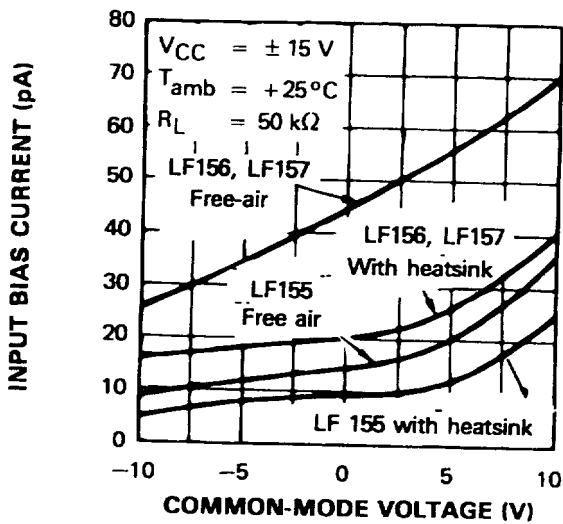
E88LF155-06

INPUT BIAS CURRENT



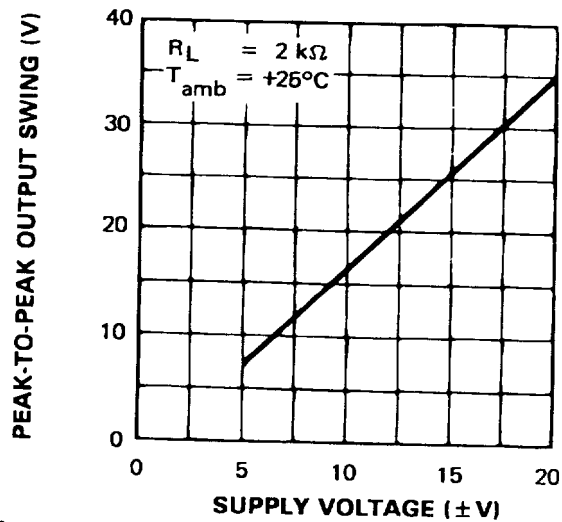
E88LF155-07

INPUT BIAS CURRENT



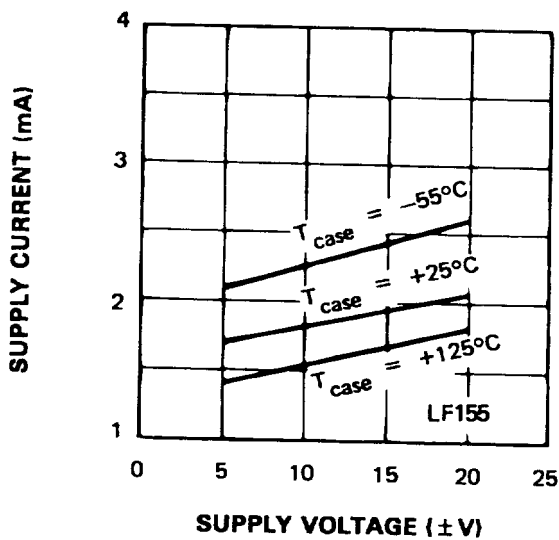
E88LF155-08

VOLTAGE SWING



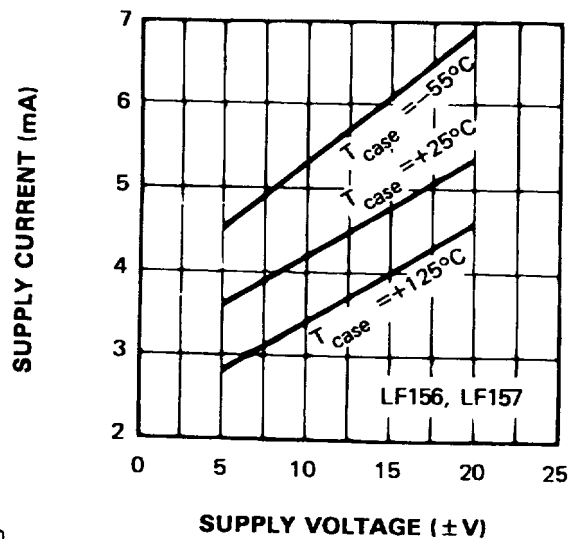
E88LF155-09

SUPPLY CURRENT



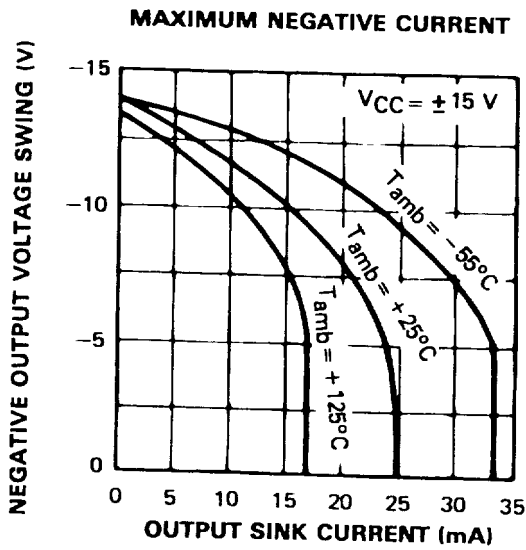
E88LF155-10

SUPPLY CURRENT

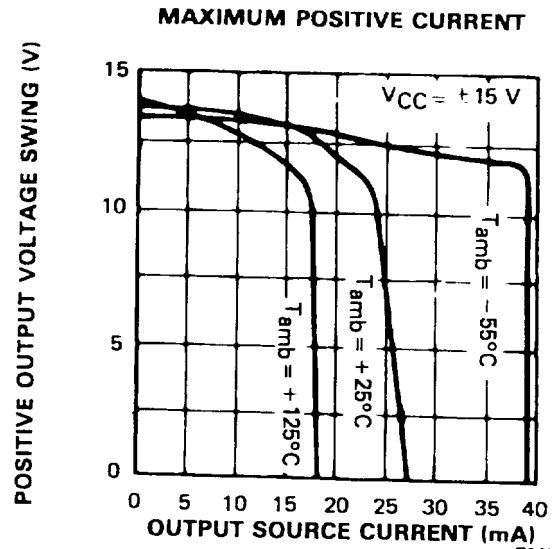


E88LF155-11

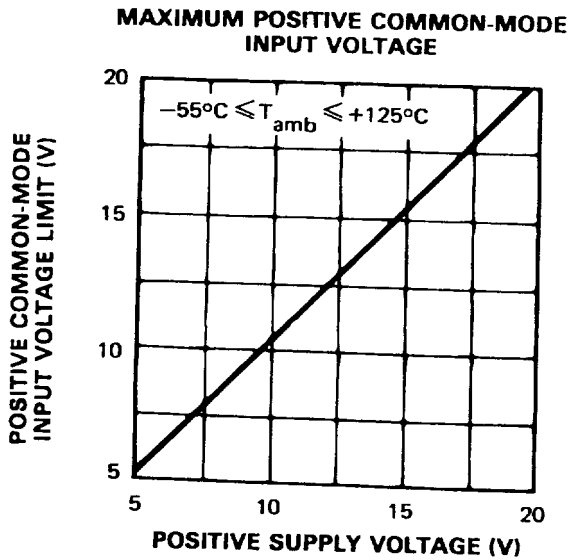
TYPICAL CHARACTERISTICS (continued)



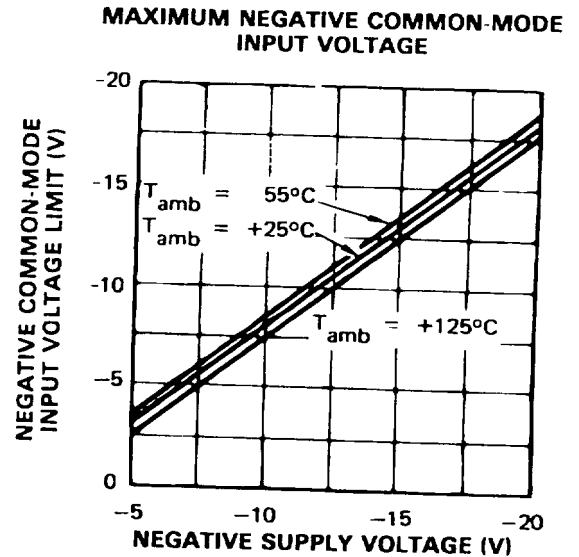
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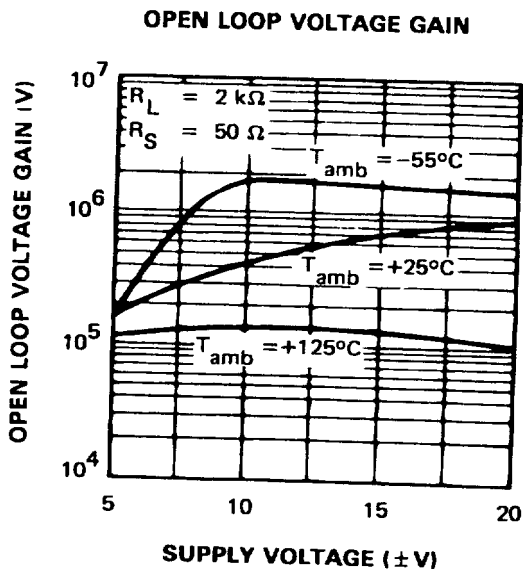
E88LF156



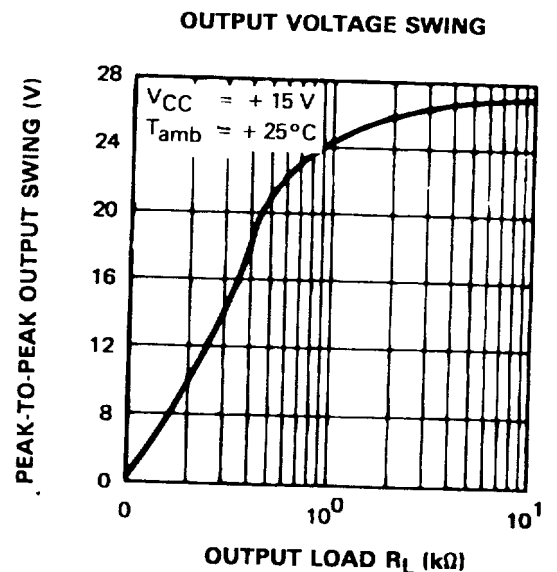
E88LF155-14



E88LF155-



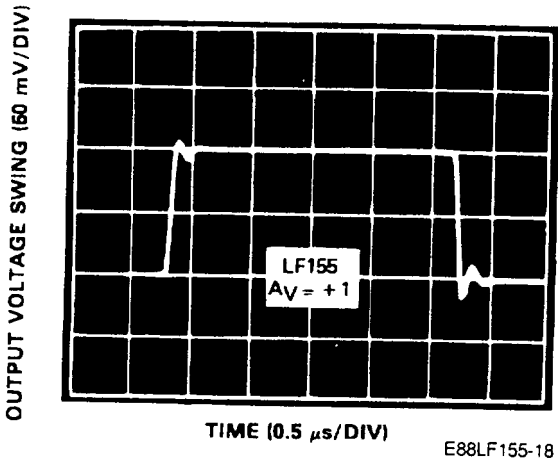
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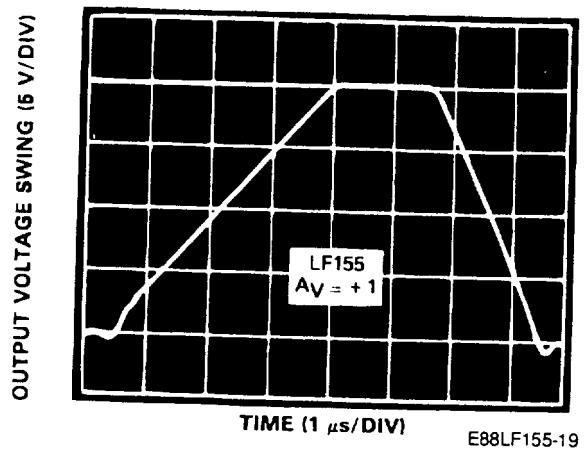
E88LF155-1

TYPICAL CHARACTERISTICS (continued)

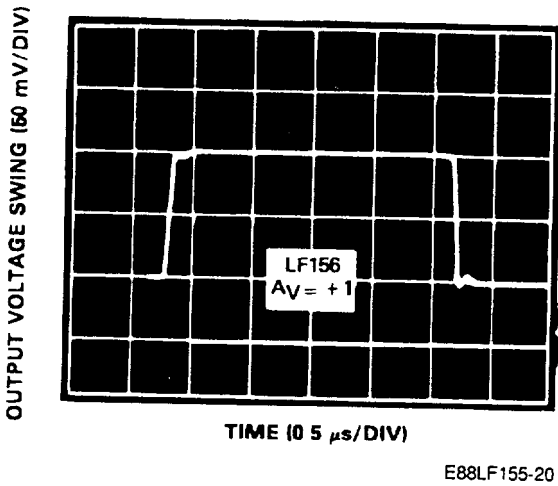
SMALL SIGNAL PULSE RESPONSE



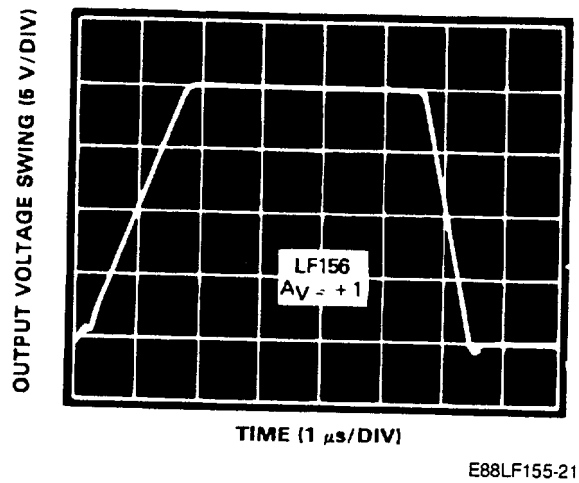
LARGE SIGNAL PULSE RESPONSE



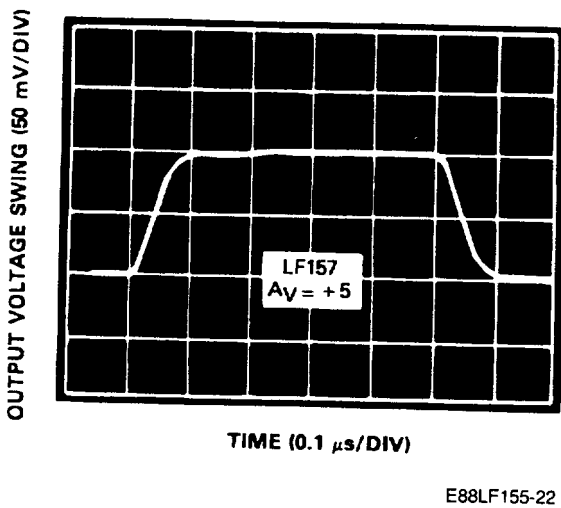
SMALL SIGNAL PULSE RESPONSE



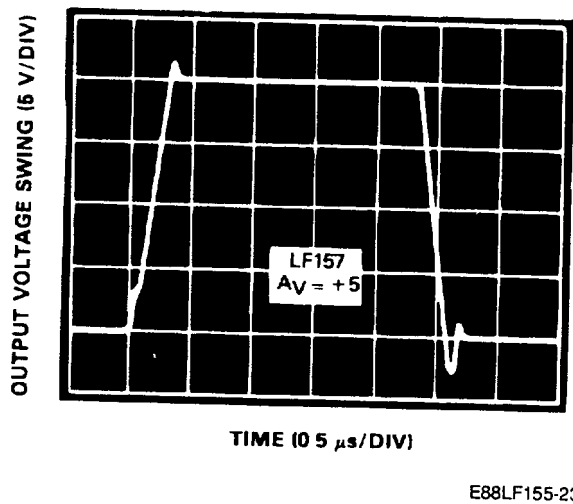
LARGE SIGNAL PULSE RESPONSE



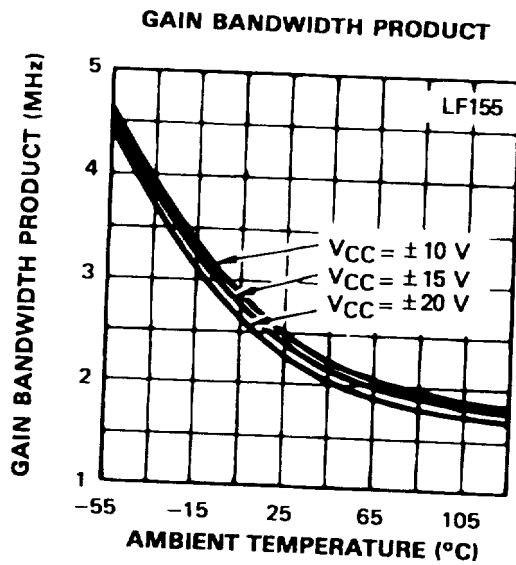
SMALL SIGNAL PULSE RESPONSE



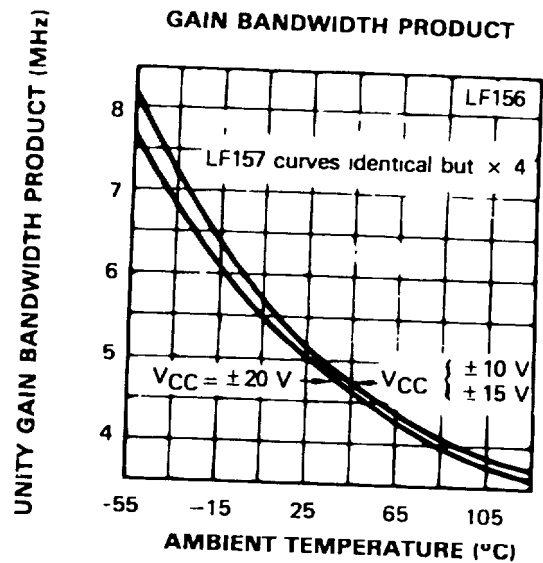
LARGE SIGNAL PULSE RESPONSE



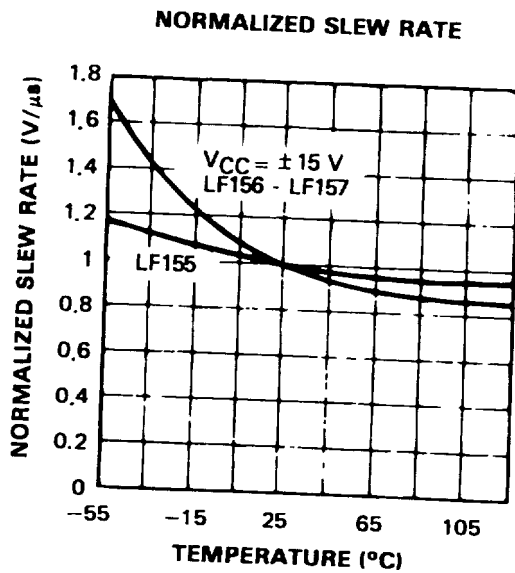
TYPICAL CHARACTERISTICS (continued)



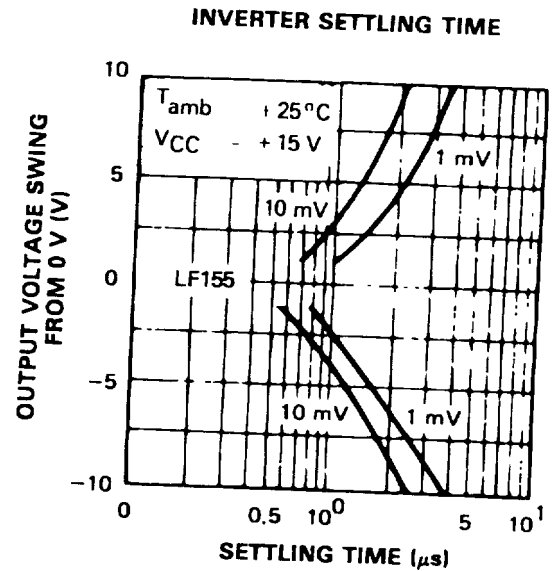
E88LF155-24



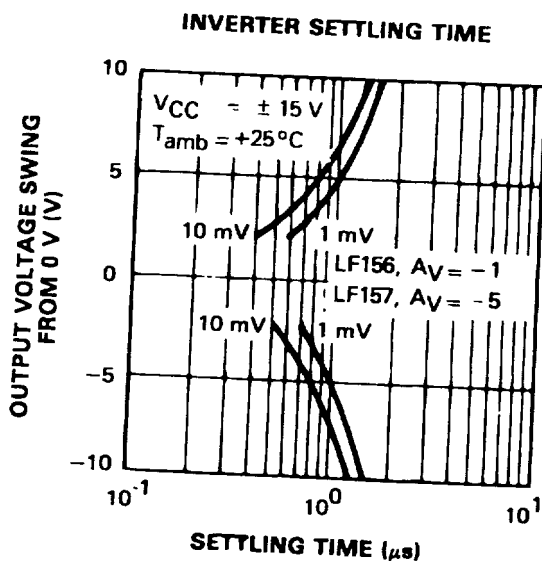
E88



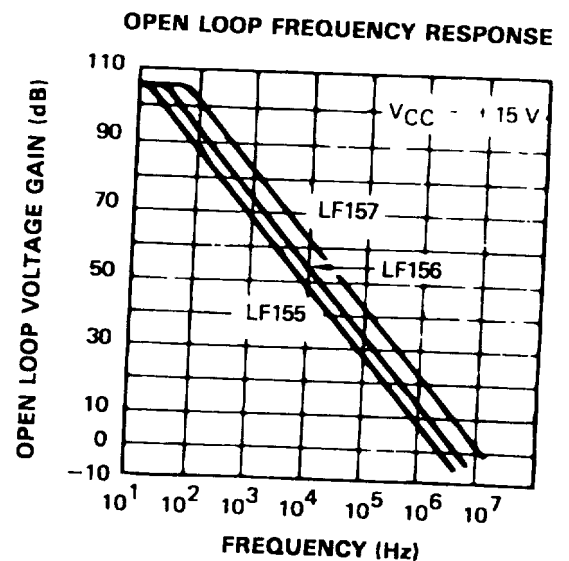
E88LF155-26



E88LF

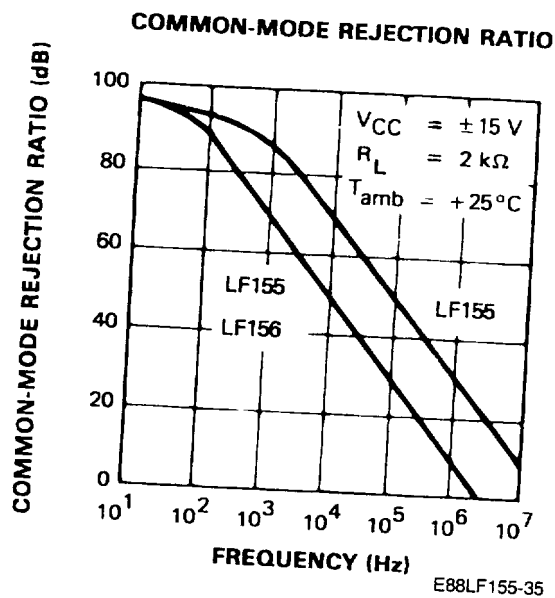
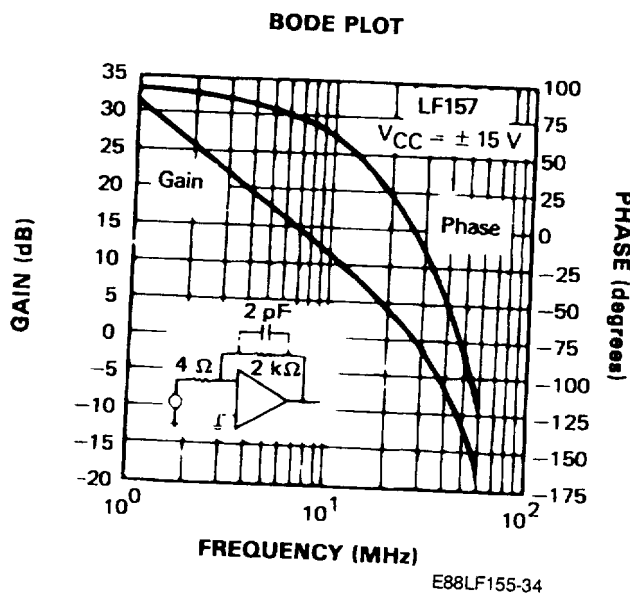
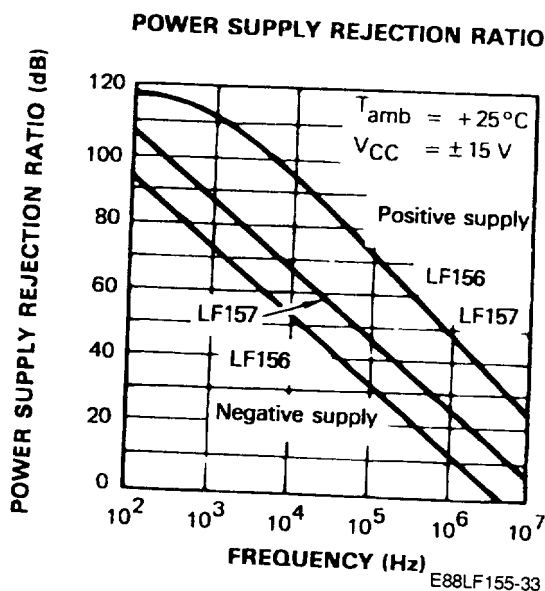
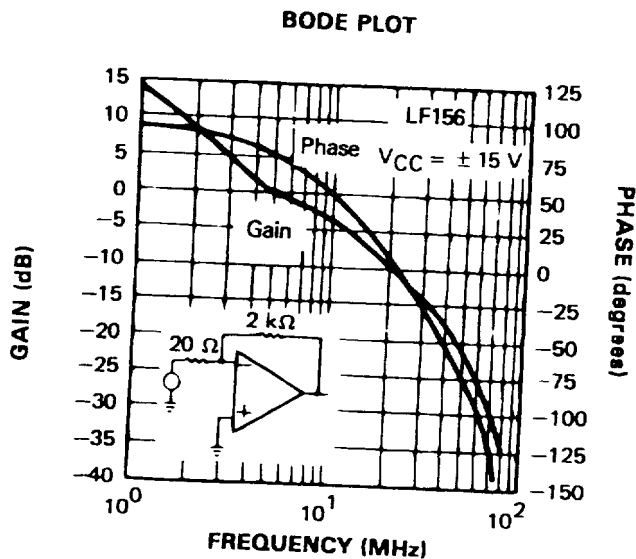
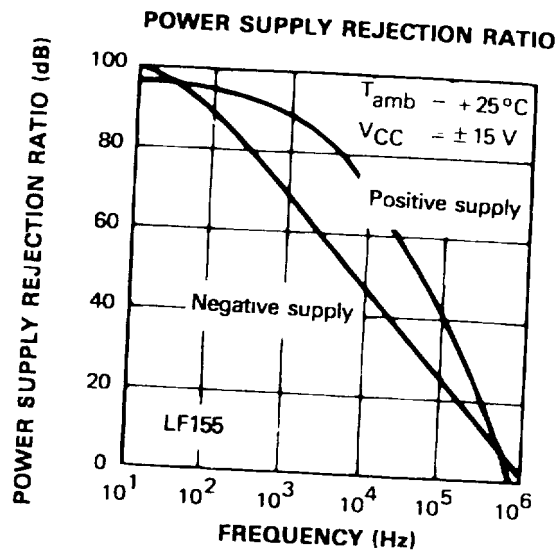
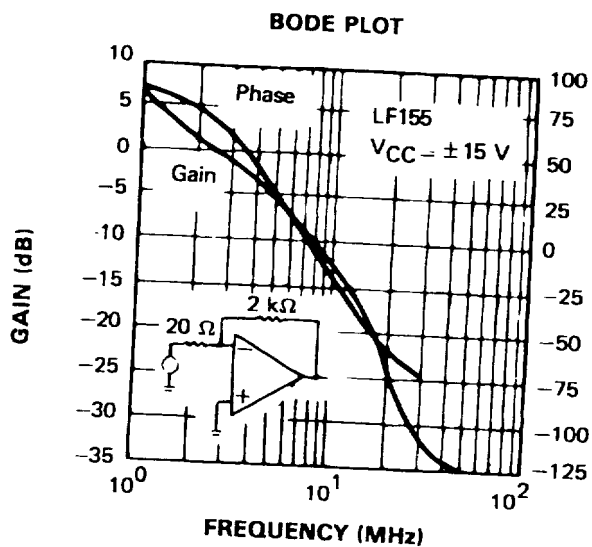


E88LF155-28



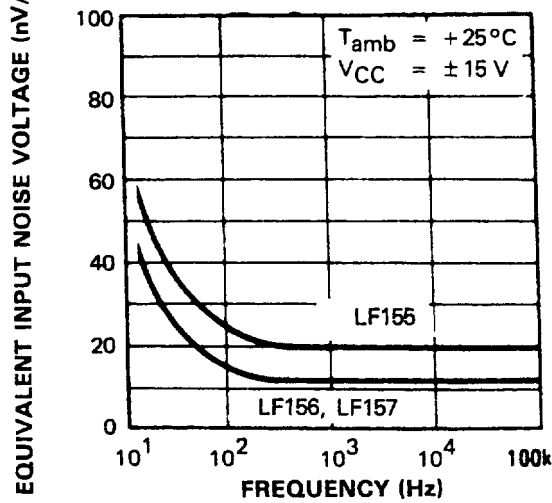
E88LF15

TYPICAL CHARACTERISTICS (continued)



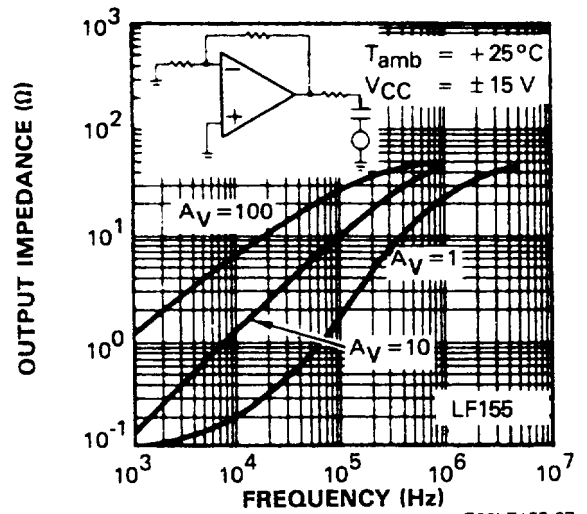
TYPICAL CHARACTERISTICS (continued)

EQUIVALENT INPUT NOISE VOLTAGE (EXPANDED SCALE)



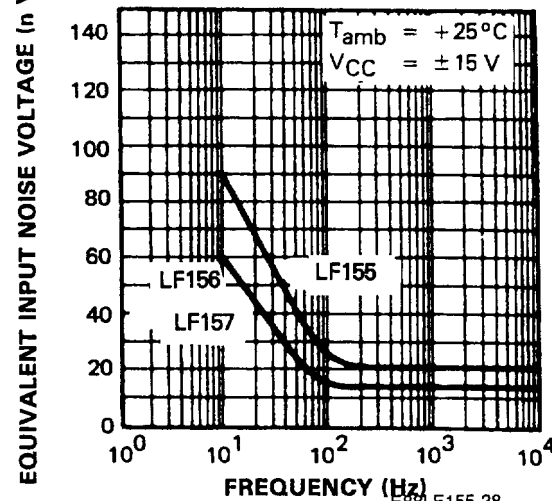
E88LF155-36

OUTPUT IMPEDANCE



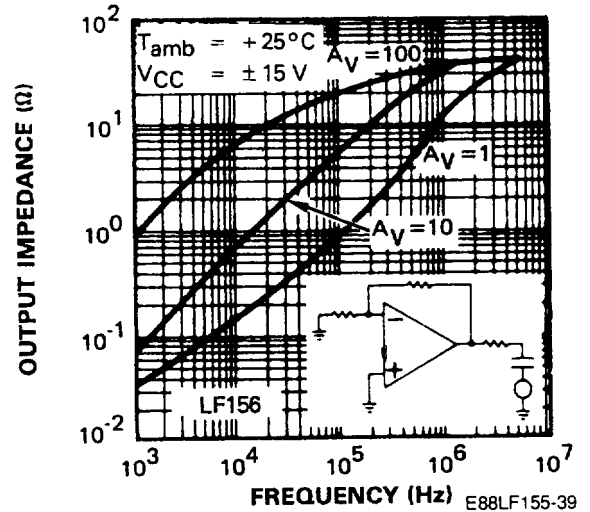
E88LF155-37

EQUIVALENT INPUT NOISE VOLTAGE



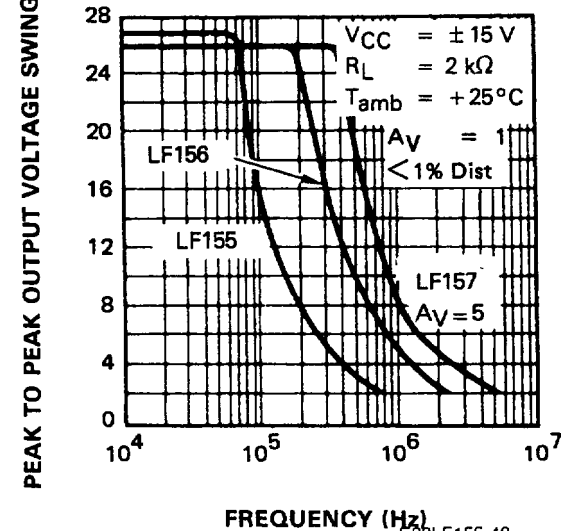
E88LF155-38

OUTPUT IMPEDANCE



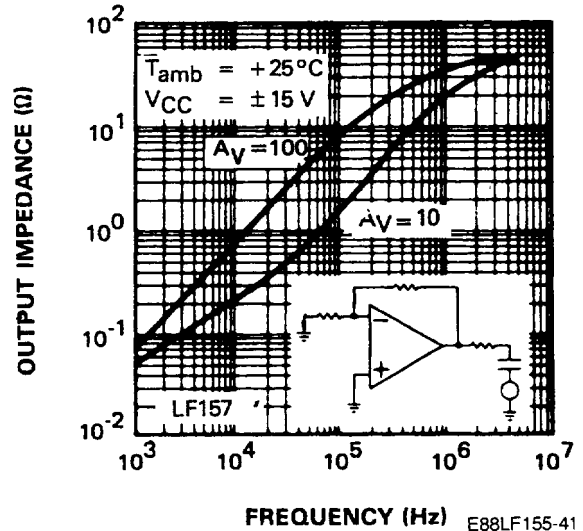
E88LF155-39

UNDISTORTED OUTPUT VOLTAGE SWING



E88LF155-40

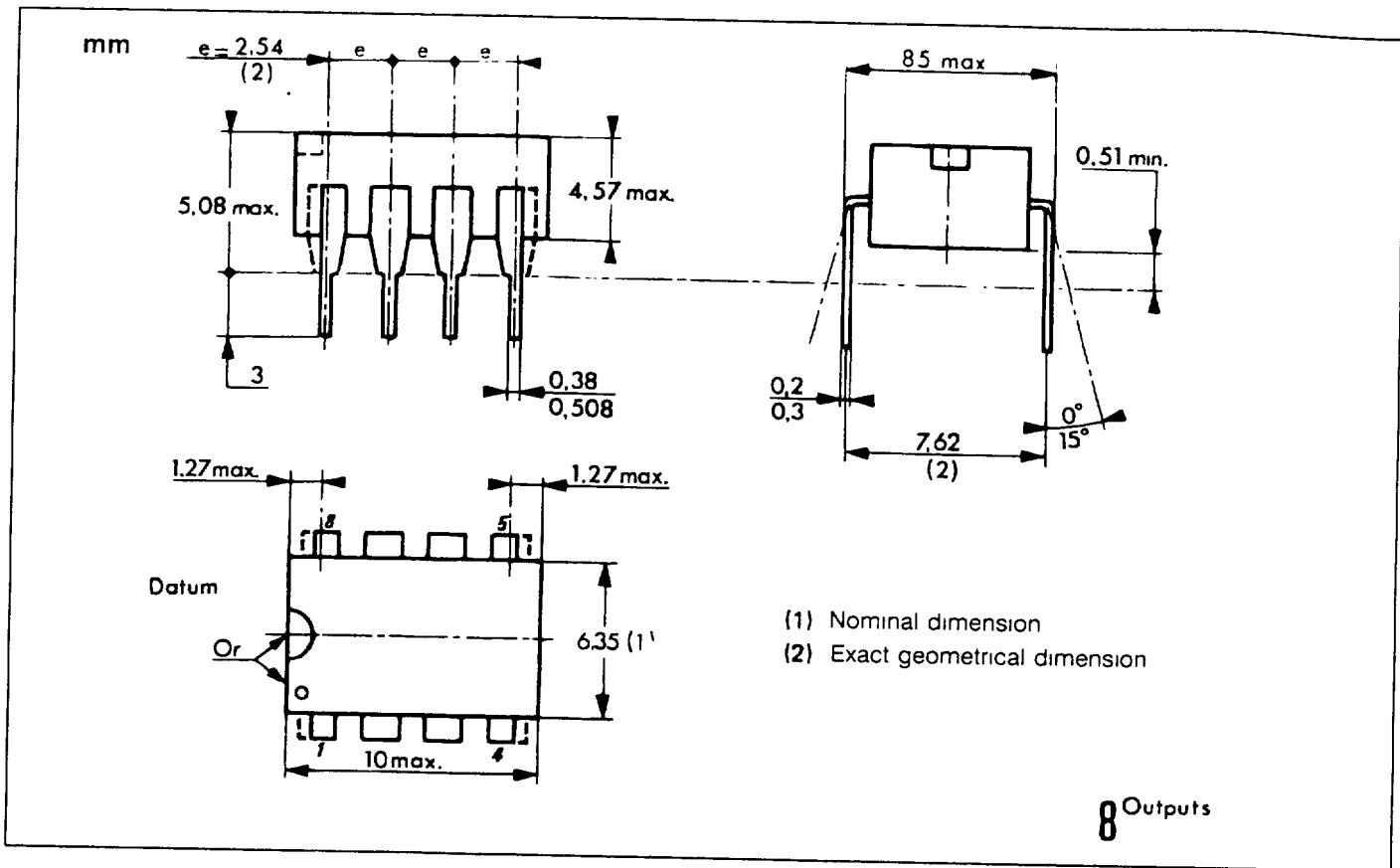
OUTPUT IMPEDANCE



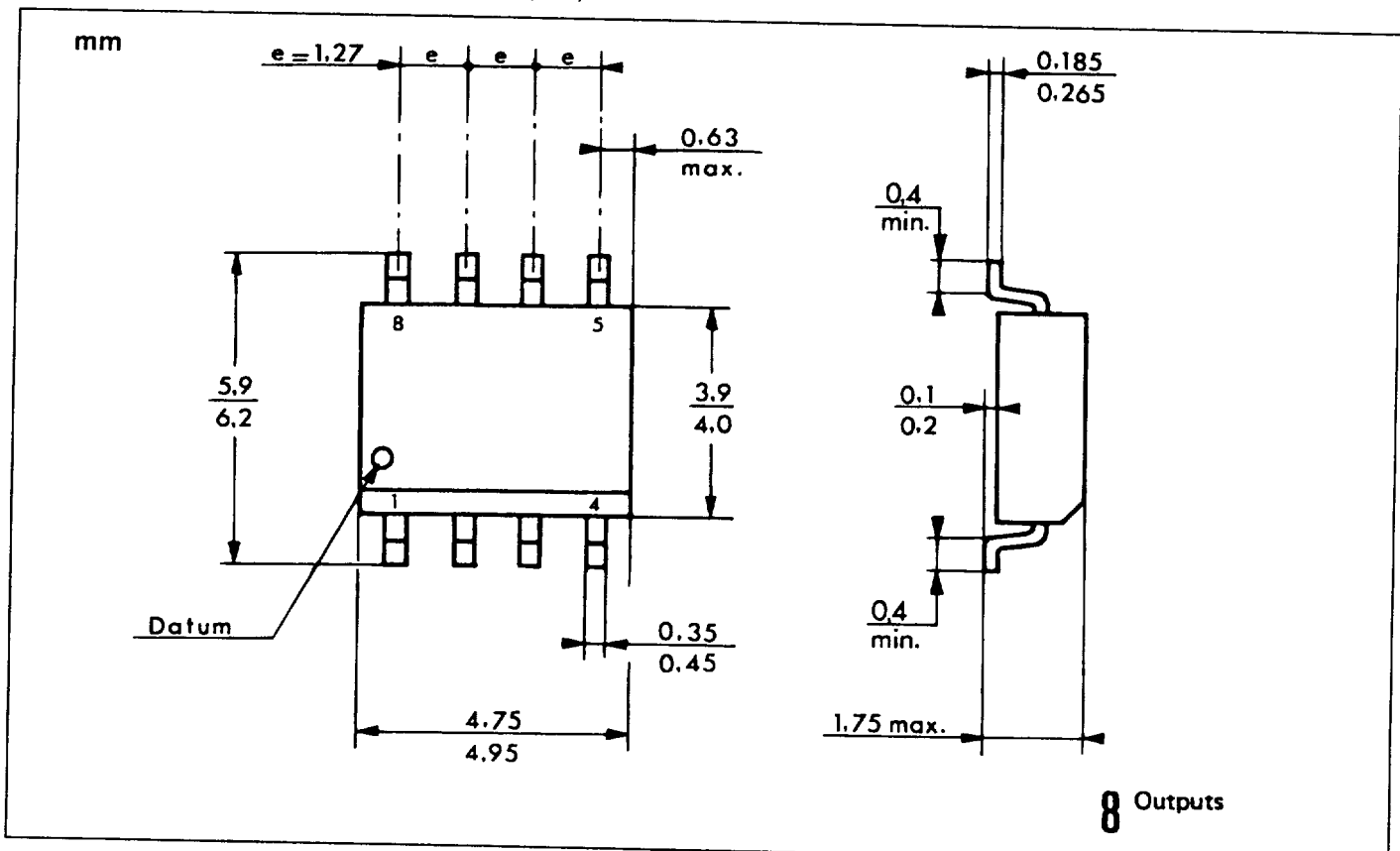
E88LF155-41

PACKAGE MECHANICAL DATA

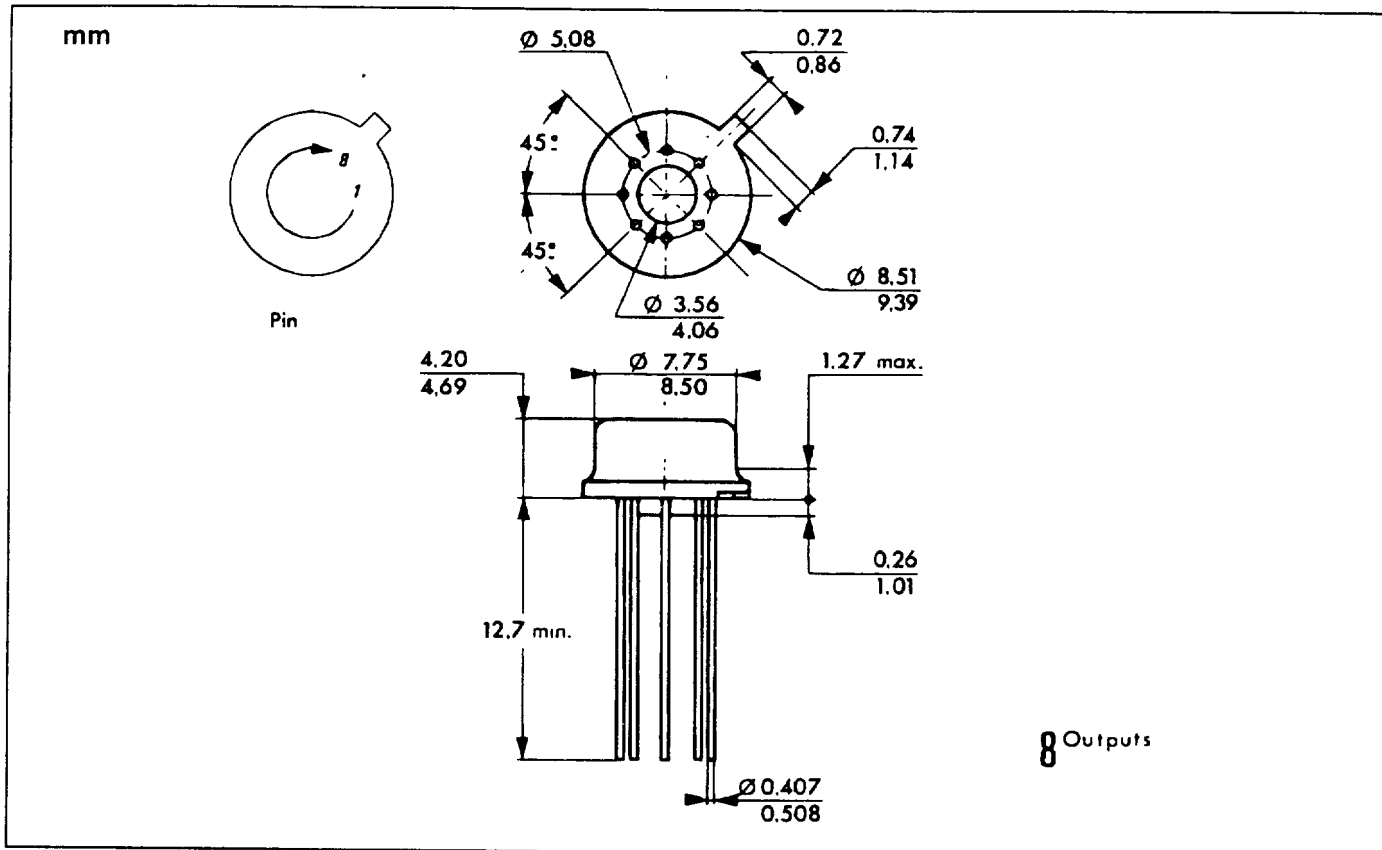
8 PINS – PLASTIC DIP



8 PINS – PLASTIC MICROPACKAGE (SO)



T0-99 – METAL CAN



20 PINS – TRICECOP (LCC)

