LF444 Quad Low Power JFET Input Operational Amplifier

Check for Samples: LF444

FEATURES

- ¼ Supply Current of a LM148: 200 µA/Amplifier (max)
- Low Input Bias Current: 50 pA (max)
- High Gain Bandwidth: 1 MHz
- High Slew Rate: 1 V/µs
- Low Noise Voltage for Low Power 35 nV/√Hz
- Low Input Noise Current 0.01 pA/√Hz
- High Input Impedance: $10^{12}\Omega$
- High Gain: 50k (min)

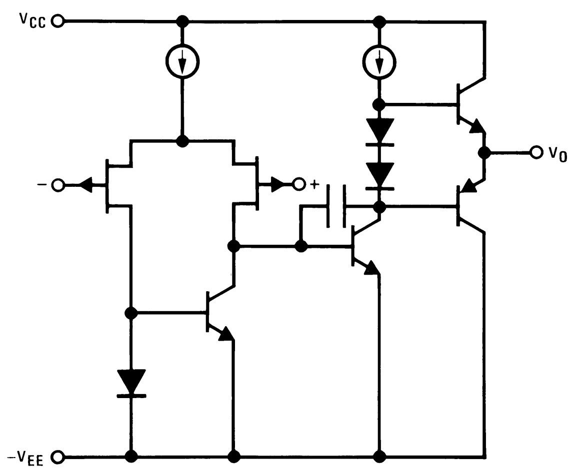
DESCRIPTION

The LF444 quad low power operational amplifier provides many of the same AC characteristics as the industry standard LM148 while greatly improving the DC characteristics of the LM148. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM148 and only draws one fourth the supply current of the LM148. In addition the well matched high voltage JFET input devices of the LF444 reduce the input bias and offset currents by a factor of 10,000 over the LM148. The LF444 also has a very low equivalent input noise voltage for a low power amplifier.

The LF444 is pin compatible with the LM148 allowing an immediate 4 times reduction in power drain in many applications. The LF444 should be used wherever low power dissipation and good electrical characteristics are the major considerations.

Simplified Schematic

Figure 1. 1/4 Quad



Connection Diagram

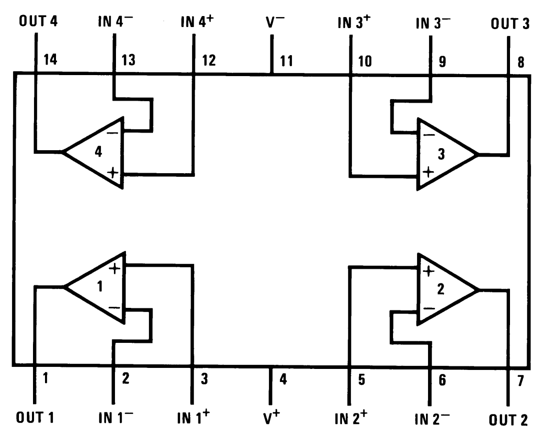


Figure 2. PDIP/SOIC Package
Top View
See Package Number NAK0014D, D0014A or NFF0014A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings[1][2][3]

			LF444A	LF444
Supply Voltage			±22V	±18V
Differential Input Voltage			±38V	±30V
Input Voltage Range[4]			±19V	±15V
Output Short CircuitDuration[5]			Continuous	Continuous
			NAK Package	**D, NFF Packages**
Power Dissipation[6][7]			900 mW	670 mW
T_j max			150°C	115°C
θ_{jA} (Typical)			100°C/W	85°C/W
			LF444A/LF444	
Operating Temperature Range			See[8]	
ESD Tolerance[9]			Rating to be determined	
Storage Temperature Range			$-65°C \le T_A \le 150°C$	
Soldering Information[10]	Dual-In-Line Packages (Soldering, 10 sec.)		260°C	
	Small Outline Package	Vapor Phase (60 sec.)	215°C	
		Infrared (15 sec.)	220°C	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Refer to RETS444X for LF444MD military specifications.
(4) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
(5) Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
(6) For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.
(7) Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.
(8) The LF444A is available in both the commercial temperature range $0°C \le T_A \le 70°C$ and the military temperature range $-55°C \le T_A \le 125°C$. The LF444 is available in the commercial temperature range only. The temperature range is designated by the position just before the package type in the device number. A “C” indicates the commercial temperature range and an “M” indicates the military temperature range. The military temperature range is available in “NAK” package only.
(9) Human body model, 1.5 kΩ in series with 100 pF.
(10) See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

DC Electrical Characteristics [1]

Symbol	Parameter	Conditions		LF444A			LF444			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10k, T_A = 25°C			2	5		3	10	mV
		$0°C \le T_A \le +70°C$				6.5			12	mV
		$-55°C \le T_A \le +125°C$				8				mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ			10			10		μV/°C
I_{OS}	Input Offset Current	V_S = ±15V[1] [2]	T_j = 25°C		5	25		5	50	pA
			T_j = 70°C			1.5			1.5	nA
			T_j = 125°C			10				nA

(1) Unless otherwise specified the specifications apply over the full temperature range and for V_S = ±20V for the LF444A and for V_S = ±15V for the LF444. V_{OS}, I_B, and I_{OS} are measured at V_{CM} = 0.
(2) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

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DC Electrical Characteristics (1) (continued)

Symbol	Parameter	Conditions		LF444A Min	LF444A Typ	LF444A Max	LF444 Min	LF444 Typ	LF444 Max	Units
I_B	Input Bias Current	$V_S = \pm15V$ (1) (2)	$T_j = 25°C$		10	50		10	100	pA
			$T_j = 70°C$			3			3	nA
			$T_j = 125°C$			20				nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $V_O = \pm10V$		50	100		25	100		V/mV
		$R_L = 10\ k\Omega$, $T_A = 25°C$								
		Over Temperature		25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10\ k\Omega$		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range			±16	+18 −17		±11	+14 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$		80	100		70	95		dB
PSRR	Supply Voltage Rejection Ratio	See (3)		80	100		70	90		dB
I_S	Supply Current				0.6	0.8		0.6	1.0	mA

(3) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from ±15V to ±5V for the LF444 and from ±20V to ±5V for the LF444A.

AC Electrical Characteristics (1)

Symbol	Parameter	Conditions	LF444A Min	LF444A Typ	LF444A Max	LF444 Min	LF444 Typ	LF444 Max	Units
	Amplifier-to-Amplifier Coupling			−120			−120		dB
SR	Slew Rate	$V_S = \pm15V$, $T_A = 25°C$		1			1		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm15V$, $T_A = 25°C$		1			1		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		35			35		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

(1) Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm20V$ for the LF444A and for $V_S = \pm15V$ for the LF444. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

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Typical Performance Characteristics

Input Bias Current

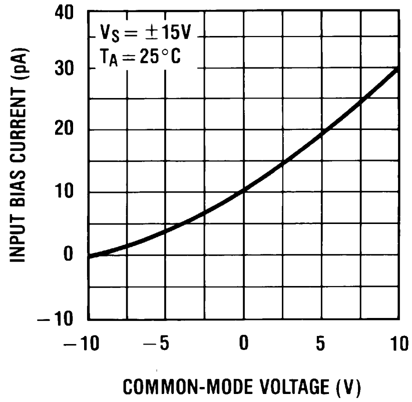

Figure 3.

Input Bias Current

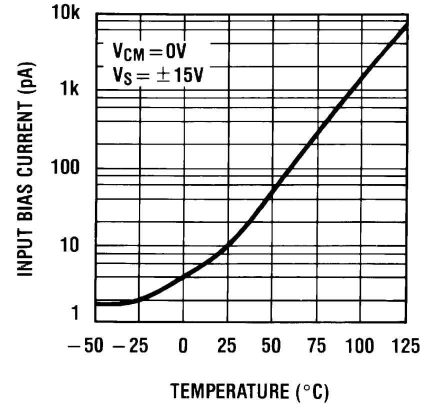

Figure 4.

Supply Current

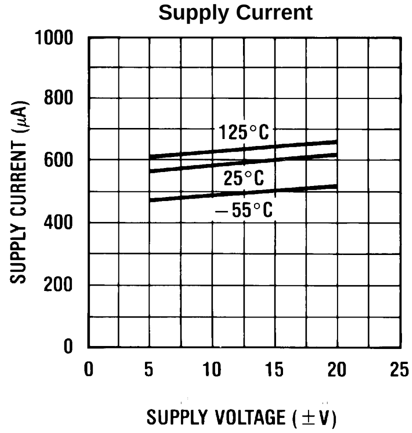

Figure 5.

Positive Common-Mode Input Voltage Limit

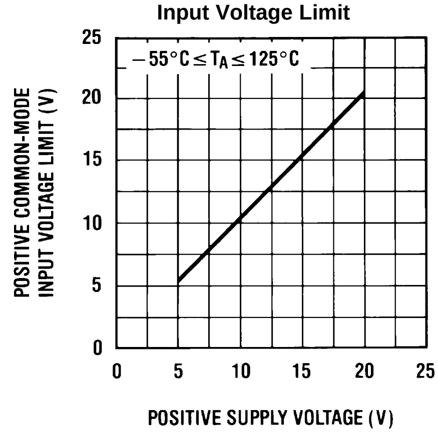

Figure 6.

Negative Common-Mode Input Voltage Limit

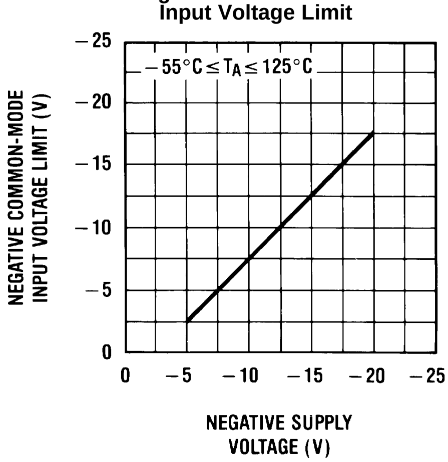

Figure 7.

Positive Current Limit

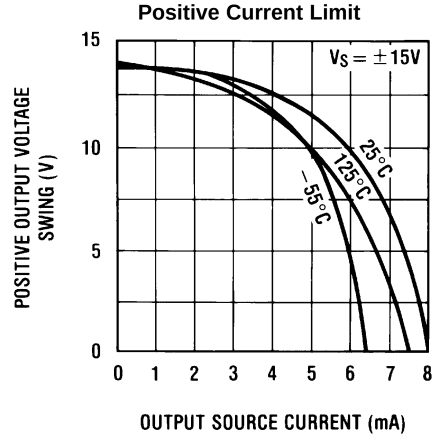

Figure 8.

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Typical Performance Characteristics (continued)

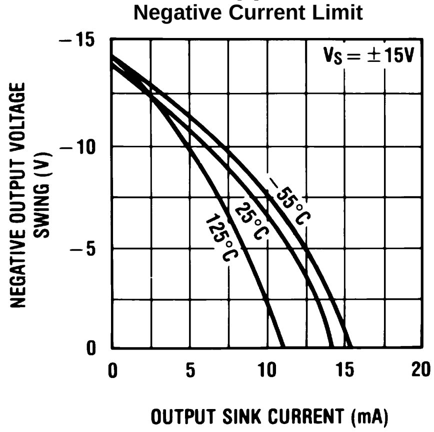

Figure 9.

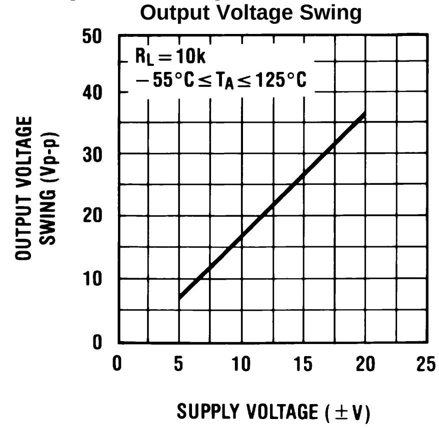

Figure 10.

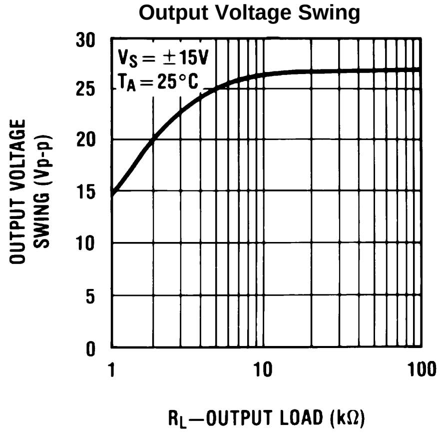

Figure 11.

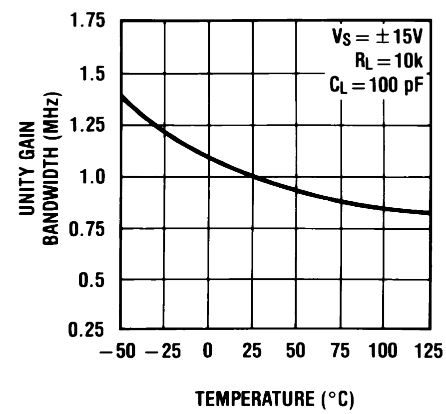

Figure 12.

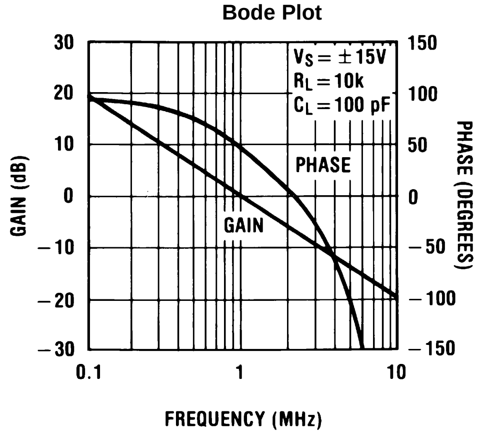

Figure 13.

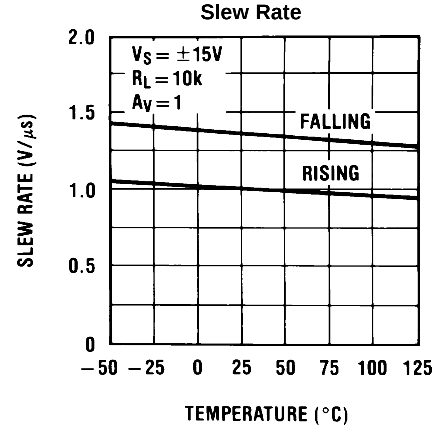

Figure 14.

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Typical Performance Characteristics (continued)

Distortion vs Frequency

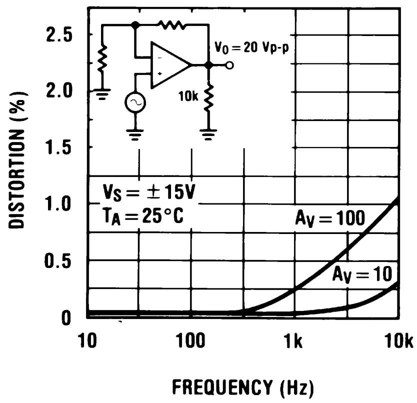

Figure 15.

Undistorted Output Voltage Swing

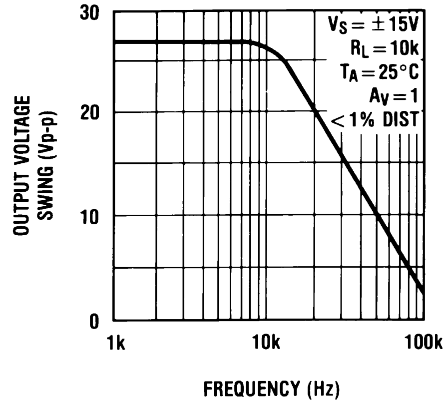

Figure 16.

Open Loop Frequency Response

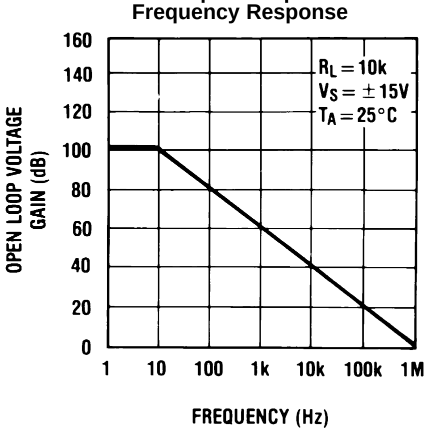

Figure 17.

Common-Mode Rejection Ratio

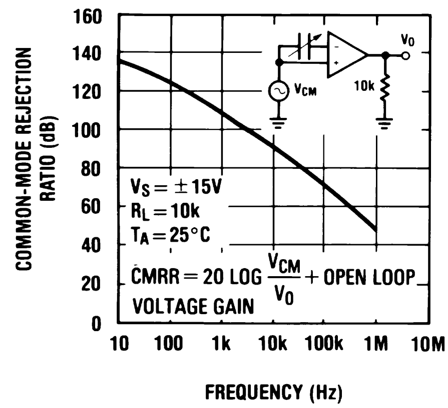

Figure 18.

Power Supply Rejection Ratio

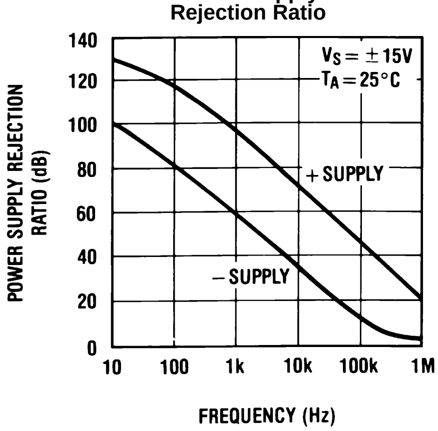

Figure 19.

Equivalent Input Noise Voltage

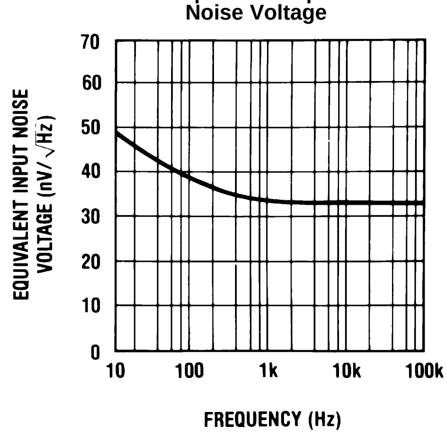

Figure 20.

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Typical Performance Characteristics (continued)

Open Loop Voltage Gain

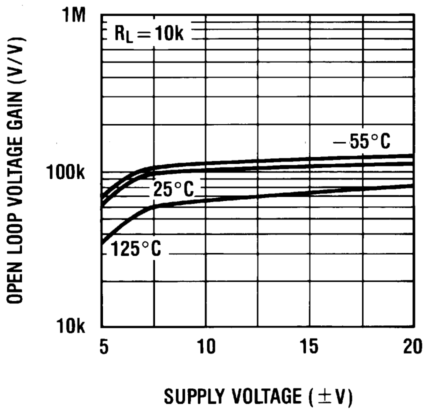

Figure 21.

Output Impedance

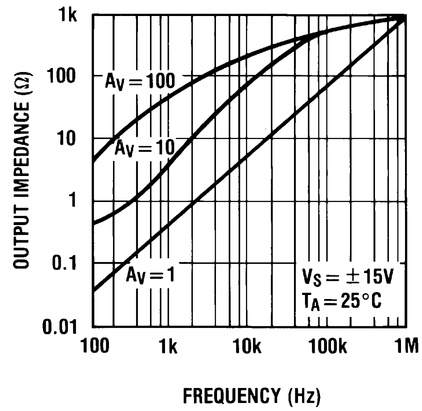

Figure 22.

Inverter Settling Time

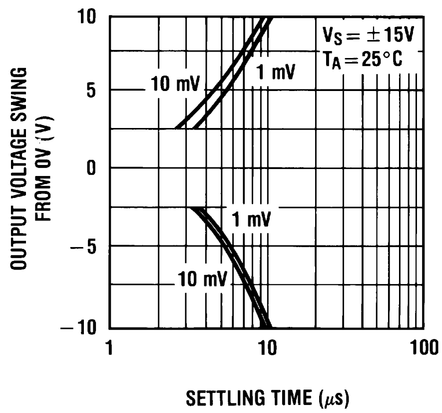

Figure 23.

Pulse Response

R_L = 10 kΩ, C_L = 10 pF

Small Signal Inverting

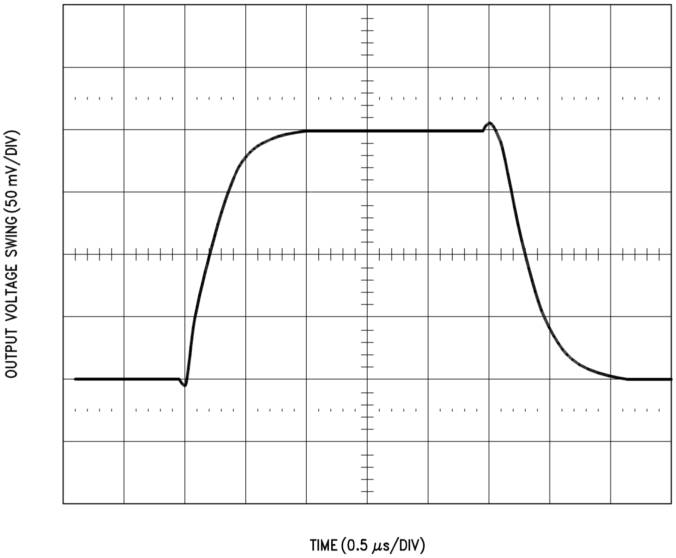

Figure 24.

Large Signal Inverting

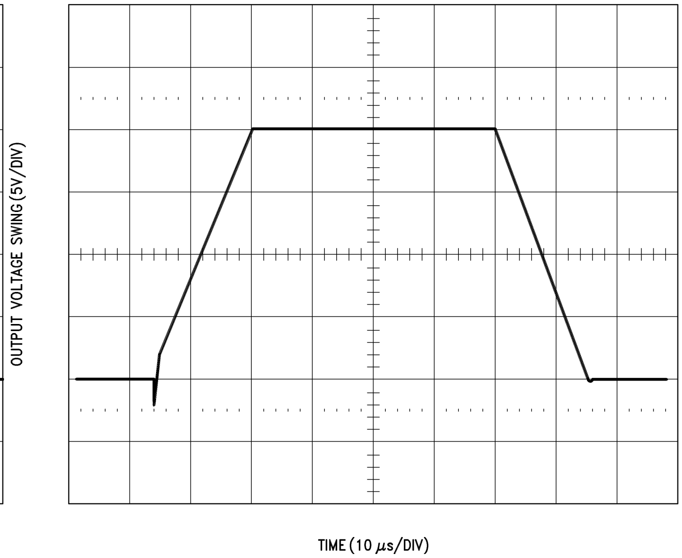

Figure 25.

Small Signal Non-Inverting

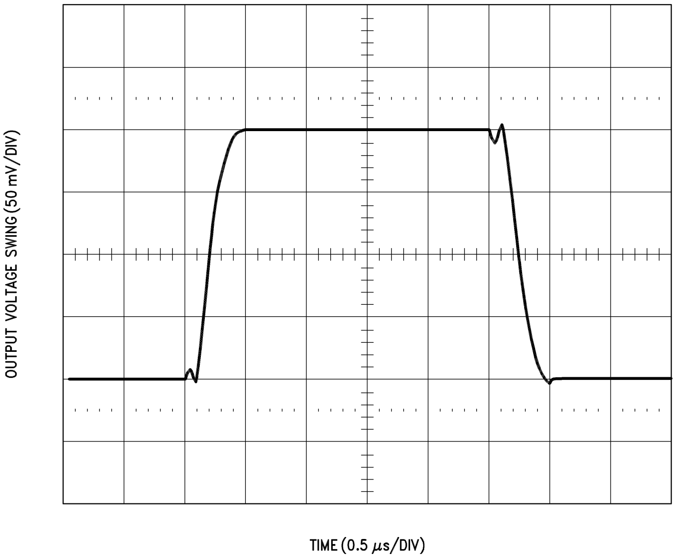

Figure 26.

Large Signal Non-Inverting

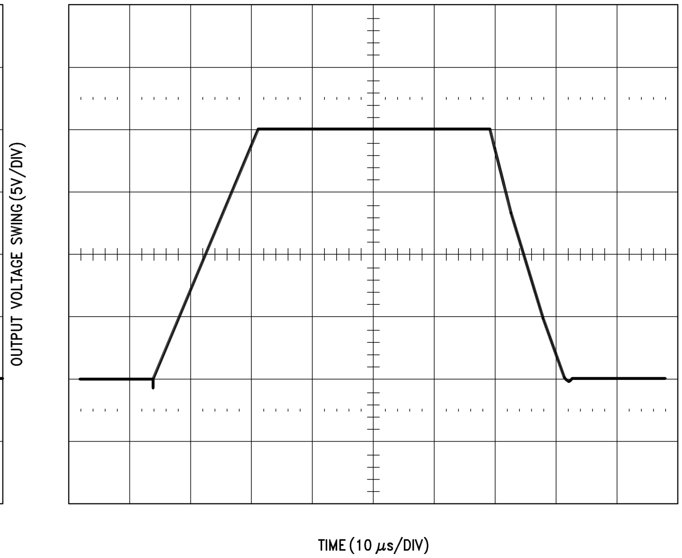

Figure 27.

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APPLICATION HINTS

This device is a quad low power op amp with JFET input devices (BI-FET™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

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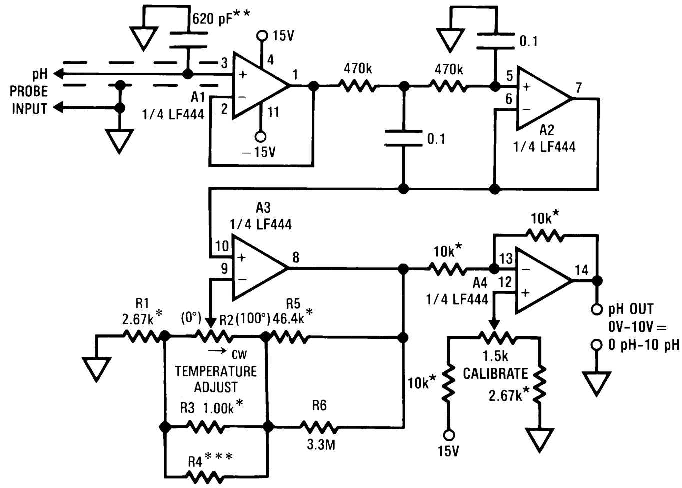
Typical Application

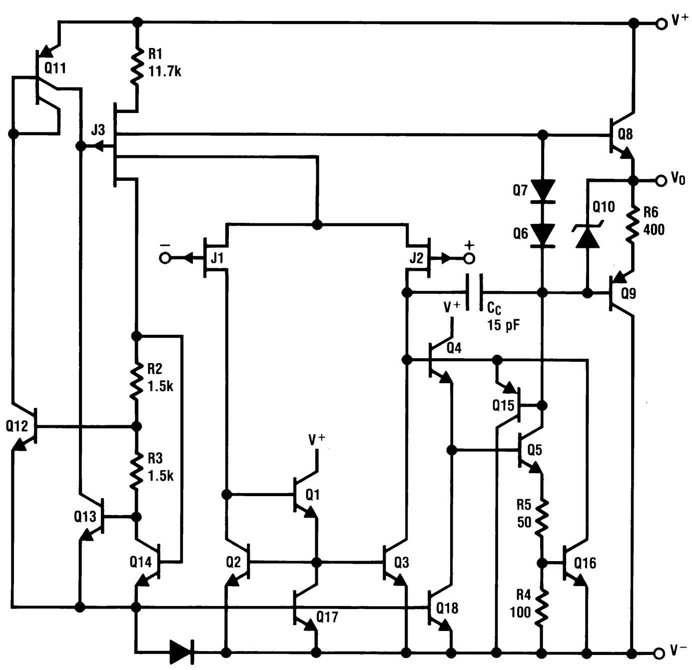
Figure 28. pH Probe Amplifier/Temperature Compensator



***For R2 = 50k, R4 = 330k ±1%
For R2 = 100k, R4 = 75k ±1%
For R2 = 200k, R4 = 56k ±1%
**Polystyrene
*Film resistor type RN60C
To calibrate, insert probe in pH =7 solution. Set the "TEMPERATURE ADJUST" pot, R2, to correspond to the solution temperature: full clockwise for 0°C, and proportionately for intermediate temperatures, using a turns-counting dial.
Then set "CALIBRATE" pot so output reads 7V.
Typical probe = Ingold Electrodes #465-35

Detailed Schematic

Figure 29. 1/4 Quad



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LF444ACN	ACTIVE	PDIP	NFF	14	25	TBD	SNPB	Level-1-NA-UNLIM	0 to 70	LF444ACN	Samples
LF444ACN/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	0 to 70	LF444ACN	Samples
LF444CM	ACTIVE	SOIC	D	14	55	TBD	CU SNPB	Level-1-235C-UNLIM	0 to 70	LF444CM	Samples
LF444CM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LF444CM	Samples
LF444CMX	ACTIVE	SOIC	D	14	2500	TBD	CU SNPB	Level-1-235C-UNLIM	0 to 70	LF444CM	Samples
LF444CMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LF444CM	Samples
LF444CN	ACTIVE	PDIP	NFF	14	25	TBD	SNPB	Level-1-NA-UNLIM	0 to 70	LF444CN	Samples
LF444CN/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	0 to 70	LF444CN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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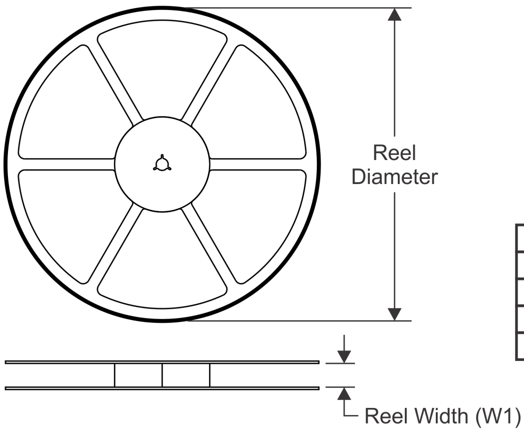
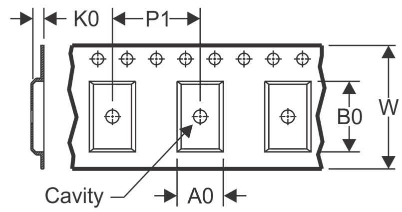
TAPE AND REEL INFORMATION

REEL DIMENSIONS

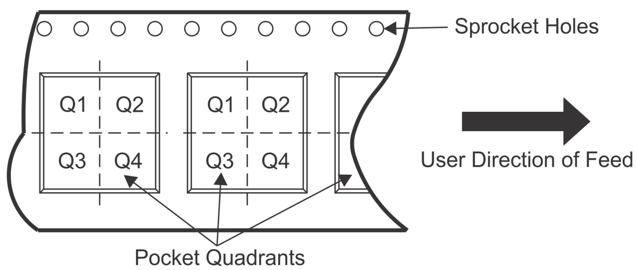


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

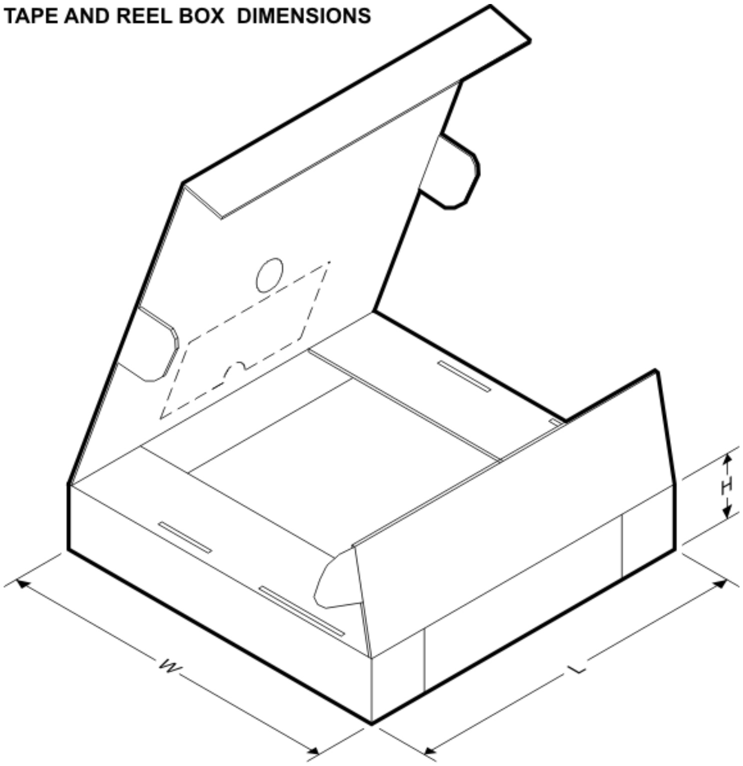
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LF444CMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LF444CMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

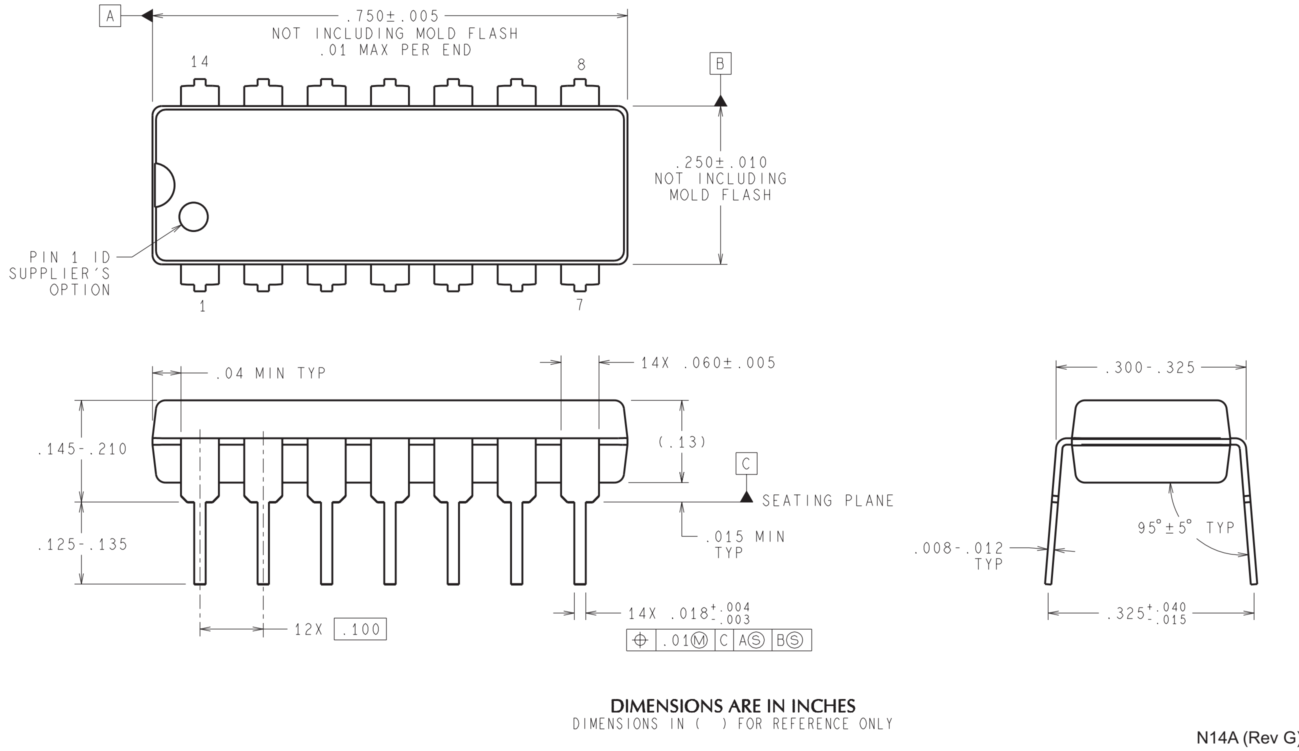
TAPE AND REEL BOX DIMENSIONS



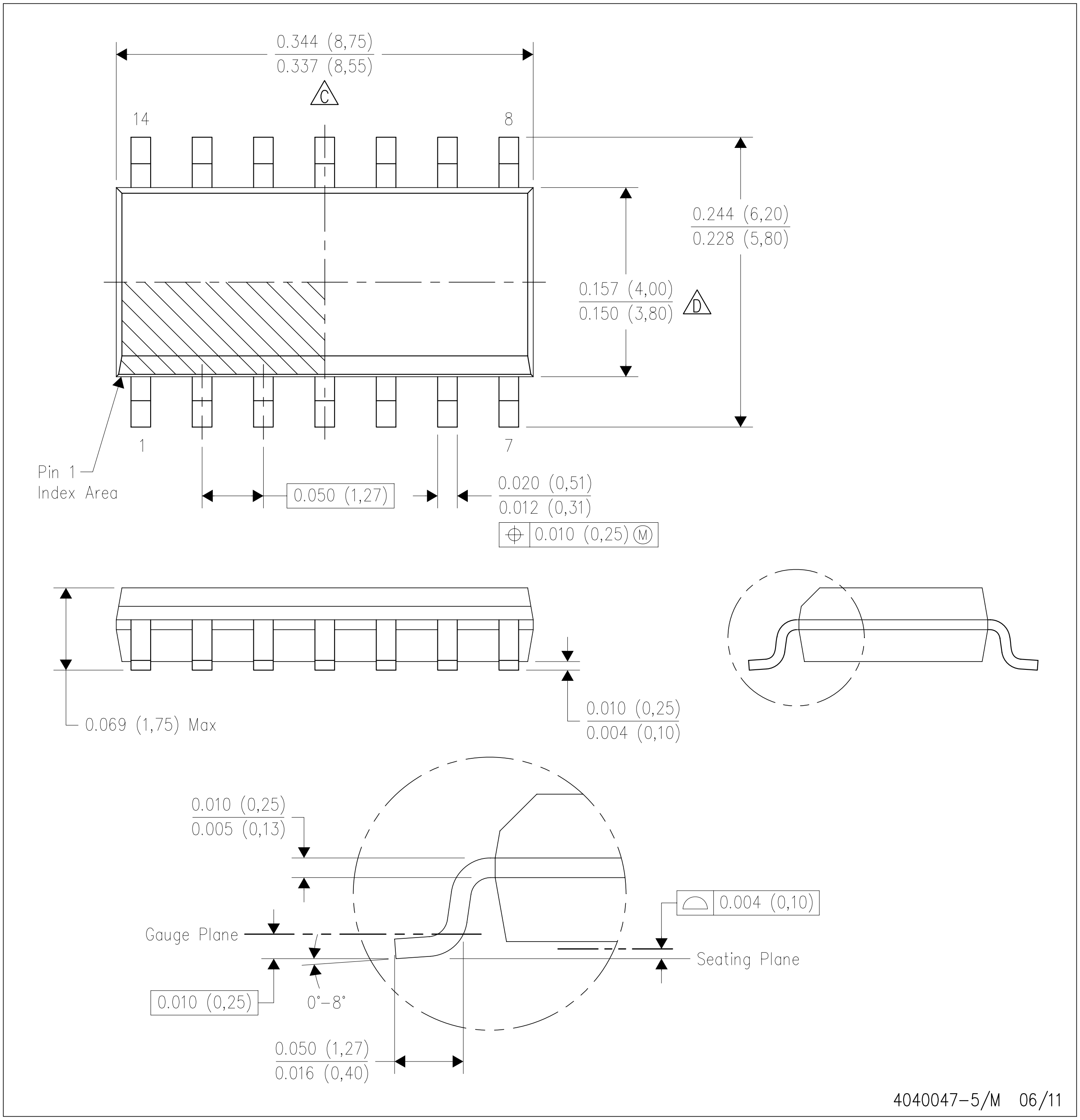
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LF444CMX	SOIC	D	14	2500	349.0	337.0	45.0
LF444CMX/NOPB	SOIC	D	14	2500	349.0	337.0	45.0

NFF0014A


A
.750±.005
NOT INCLUDING MOLD FLASH
.01 MAX PER END
14
8
B
.250±.010
NOT INCLUDING
MOLD FLASH
PIN 1 ID
SUPPLIER'S
OPTION
1
7
.04 MIN TYP
14X .060±.005
.300-.325
.145-.210
(.13)
C
SEATING PLANE
.125-.135
.015 MIN
TYP
.008-.012
TYP
95°±5° TYP
14X .018+.004 -.003
.01 M C A S B S
12X .100
.325+.040 -.015
DIMENSIONS ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY
N14A (Rev G)

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

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