Voltage Regulators

LM114/LM114A/LM115/LM115A transistor pairs

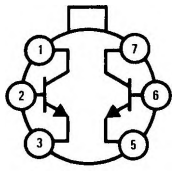
general description

These devices contain a pair of junction-isolated NPN transistors fabricated on a single silicon substrate. This monolithic structure makes possible extremely-tight parameter matching at low cost. Further, advanced processing techniques yield exceptionally high current gains at low collector currents, virtual elimination of "popcorn noise," low leakages and improved long-term stability. Some of the major features of these pairs are indicated by the following specifications:

- Low offset voltage—0.5 mV maximum
- Low drift—2 μV/°C maximum from −55°C to 125°C
- High current gain—500 minimum at 10 μA
- Tight beta match—10% maximum
- High breakdown voltage—to 60V
- Matching guaranteed over a 0V to 45V collector-base voltage range.

Although designed primarily for high breakdown voltage and exceptional dc characteristics, these transistors have surprisingly good high-frequency performance. The gain-bandwidth product is 450 MHz with 1 mA collector current and 5V collector-base voltage and 22 MHz with 10 μA collector current. Collector-base capacitance is only 1.3 pF at 5V.

connection diagram



TOP VIEW

absolute maximum ratings

	LM114 LM114A	LM115 LM115A
Collector-Base Voltage (BV_{CBO})	45V	60V
Collector-Emitter Voltage (BV_{CER})	45V	60V
Collector-Collector Voltage	45V	60V
Emitter-Emitter Voltage	45V	60V
Emitter-Base Voltage (BV_{EBO})	6V	
Collector Current	20 mA	
Total Power Dissipation (Note 1)	1.8W	
Operating Junction Temperature	−55°C to 150°C	
Storage Temperature	−65°C to 150°C	
Lead Temperature (soldering, 10 sec)	300°C	

Note 1: The maximum dissipation given is for a 25°C case temperature. For operation under other conditions, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 70°C/W junction to case or 230°C/W junction to ambient.

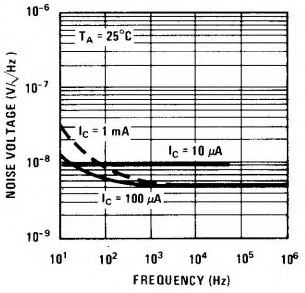
electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MAXIMUM LIMITS				UNITS
		LM114	LM114A	LM115	LM115A	
Offset Voltage	$1\,\mu A \leq I_C \leq 100\,\mu A$	2.0	0.5	2.0	0.5	mV
Offset Current	$I_C = 10\,\mu A$ $I_C = 1\,\mu A$	10	2.0 0.5	10	2.0 0.5	nA nA
Bias Current	$I_C = 10\,\mu A$ $I_C = 1\,\mu A$	40	20 3.0	40	40 6.0	nA nA
Offset Voltage Change	$0V \leq V_{CB} \leq V_{max}$ $I_C = 10\,\mu A$	1.5	0.2	2.0	0.3	mV
Offset Current Change	$0V \leq V_{CB} \leq V_{max}$ $I_C = 10\,\mu A$	4.0	1.0	4.0	1.0	nA
Offset Voltage Drift	$-55°C \leq T_A \leq 125°C$ $I_C = 10\,\mu A$	10	2.0	10	2.0	$\mu V/°C$
Offset Current	$-55°C \leq T_A \leq 125°C$ $I_C = 10\,\mu A$	50	12	50	20	nA
Bias Current	$-55°C \leq T_A \leq 125°C$ $I_C = 10\,\mu A$	150	60	150	150	nA
Collector-Base Leakage Current	$V_{CB} = V_{max}$ $T_A = 25°C$ $T_A = 125°C$	 50 50	 10 10	 50 50	 10 10	 pA nA
Collector-Emitter Leakage Current	$V_{CE} = V_{max}$, $V_{EB} = 0$ $T_A = 25°C$ $T_A = 125°C$	 200 200	 50 50	 200 200	 50 50	 pA nA
Collector-Collector Leakage Current	$V_{CC} = V_{max}$ $T_A = 25°C$ $T_A = 125°C$	 300 300	 100 100	 300 300	 100 100	 pA nA

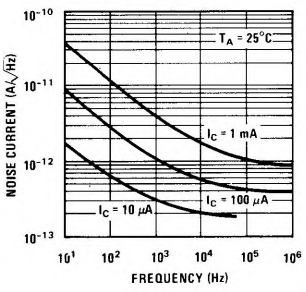
Note 2: These specifications apply for $T_A = 25°C$ and $0V \leq V_{CB} \leq V_{max}$, unless otherwise specified. For the LM114 and LM114A, $V_{max} = 30V$. For the LM115 and LM115A, $V_{max} = 45V$.

typical performance

Noise Voltage



Noise Current



Saturation Voltage