LM193A/LM193QML Low Power Low Offset Voltage Dual Comparators

Check for Samples: LM193A, LM193QML

FEATURES

- **Available with radiation guarantee**
  - **Total Ionizing Dose 100 krad(Si)**
  - **ELDRS Free 100 krad(Si)**
- **Wide supply**
  - **Voltage range: $2.0V_{DC}$ to $36V_{DC}$**
  - **Single or dual supplies: ±1.0V to ±18V**
- **Very low supply current drain (0.4 mA) — independent of supply voltage**
- **Low input biasing current: 25 nA typ**
- **Low input offset current: ±5 nA typ**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to the power supply voltage**
- **Low output saturation voltage,: 250 mV at 4 mA typ**
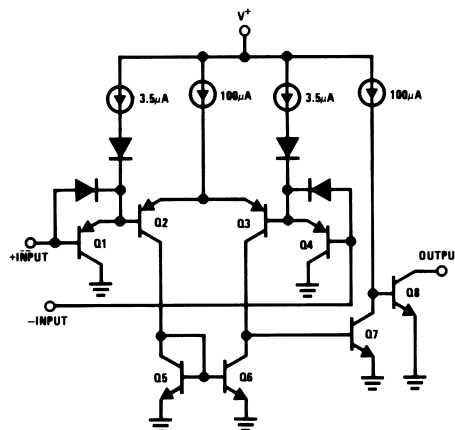- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems**

ADVANTAGES

- **High precision comparators**
- **Reduced V_{OS} drift over temperature**
- **Eliminates need for dual supplies**
- **Allows sensing near ground**
- **Compatible with all forms of logic**
- **Power drain suitable for battery operation**

DESCRIPTION

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

Schematic and Connection Diagrams

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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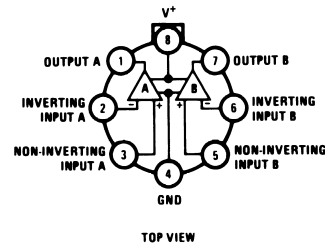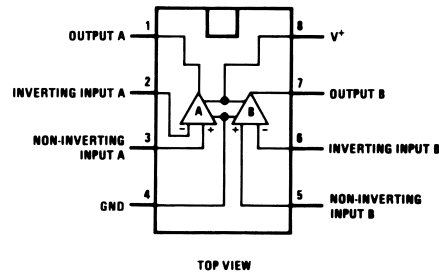**Figure 1. Metal Can Package**

TOP VIEW

Figure 2. Dual-In-Line Package

TOP VIEW

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [(1)]

Supply Voltage, V^+	$36V_{DC}$ or $\pm18V_{DC}$
Differential Input Voltage [(2)]	36V
Input Voltage	$-0.3V_{DC}$ to $+36V_{DC}$
Input Current ($V_{IN}< -0.3V_{DC}$) [(3)]	50 mA
Maximum Junction Temperature	150°C
Power Dissipation [(4)], [(5)]	
Metal Can	660 mW
CERDIP	780 mW
Output Short-Circuit to Ground [(6)]	Continuous
Operating Temperature Range	$-55°C \le T_A \le +125°C$
Storage Temperature Range	$-65°C \le T_A \le +150°C$
Thermal Resistance	
θ_{JA}	
Metal Can (Still Air)	174°C/W
Metal Can (500LF/Min Air flow)	99°C/W
CERDIP (Still Air)	146°C/W
CERDIP (500LF/Min Air flow)	85°C/W
θ_{JC}	
Metal Can	44°C/W
CERDIP	33°C/W
Lead Temperature (Soldering, 10 seconds)	260°C
ESD Tolerance [(7)]	500V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used).

(3) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{DC}$.

(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

(5) The LM193A must be derated based on a 150°C, T_{Jmax}. The low bias dissipation and the ON-OFF characteristic of the outputs keep the chip dissipation very small ($P_D \le 100mV$), provided the output transistors are allowed to saturate.

(6) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

(7) Human body model, 1.5KΩ in series with 100pF.

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp°C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125

Subgroup	Description	Temp°C
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

Product Folder Links: *LM193A LM193QML*

LM193 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified.   +V = 5V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Supply Current				1.0	mA	1, 2, 3
		+V = 36V			2.5	mA	1, 2, 3
I_{CEX}	Output Leakage Current	+V = 30V, +V_I = 1V, V_O = 30V, -V_I = 0V		-0.65	0.65	µA	1
				-1.0	1.0	µA	2, 3
I_{Sink}	Output Sink Current	V_O = 1.5V, -V_I = 1V, +V_I = 0V		6.0		mA	1
V_{Sat}	Output Saturation Voltage	I_{Sink} = 4mA, -V_I = 1V, +V_I = 0V			0.4	V	1
					0.7	V	2, 3
V_{IO}	Input Offset Voltage			-5.0	5.0	mV	1
				-9.0	9.0	mV	2, 3
		+V = 30V		-5.0	5.0	mV	1
				-9.0	9.0	mV	2, 3
		+V = 30V, V_{CM} = 28.5V		-5.0	5.0	mV	1
		+V = 30V, V_{CM} = 28.0V		-9.0	9.0	mV	2, 3
±I_{IB}	Input Bias Current			-100	-1.0	nA	1
				-300	-1.0	nA	2, 3
I_{IO}	Input offset Current	R_S = 50Ω		-25	25	nA	1
				-100	100	nA	2, 3
V_{CM}	Common Mode Voltage	+V = 30V	(1)		28.5	V	1
			(1)		28	V	2, 3
PSRR	Power Supply Rejection Ratio	+V = 5V to 30V, R_S = 50Ω		60		dB	1
CMRR	Common Mode Rejection Ratio	+V = 30V, R_S = 50Ω V_{CM} = 0V to 28.5V,		60		dB	1
V_{Diff}	Differential Input Voltage	+V = 30V, +V_I = 36V, -V_I = 0V	(2)		500	nA	1, 2, 3
		+V = 30V, +V_I = 0V, -V_I = +36V	(2)		500	nA	1, 2, 3
A_{VS}	Voltage Gain	+V = 15V, R_{PullUp} = 15KΩ 1V ≤ V_O ≤ 11V,	(3)	50		V/mV	4

(1) Parameter guaranteed by the V_{IO} tests.
(2) The value for V_{Diff} is not datalogged during Read and Record.
(3) Datalog reading in K = V/mV.

LM193 Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified.   +V = 5V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_{OD} = 5mV			5.0	µS	9
		V_{OD} = 50mV			0.8	µS	9
t_{RHL}	Response Time	V_{OD} = 5mV			2.5	µS	9
		V_{OD} = 50mV			0.8	µS	9

Product Folder Links: *LM193A LM193QML*

LM193A Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified.   +V = 5V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Supply Current	R_L = Infinity			1.0	mA	1, 2, 3
		+V = 36V, R_L = Infinity			2.5	mA	1, 2, 3
I_{CEX}	Output Leakage Current	+V = 30V, +V_I = 1V, V_O = 30, -V_I = 0		-0.65	0.65	µA	1
				-1.0	1.0	µA	2, 3
I_{Sink}	Output Sink Current	V_O = 1.5V, -V_I = 1V, +V_I = 0V		6.0		mA	1
				4.0		mA	2, 3
V_{Sat}	Output Saturation Voltage	I_{Sink} = 4mA, -V_I = 1V, +V_I = 0V			0.4	V	1
					0.7	V	2, 3
V_{IO}	Input Offset Voltage			-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V, V_{CM} = 28.5V		-2.0	2.0	mV	1
		+V = 30V, V_{CM} = 28.0V		-4.0	4.0	mV	2, 3
±I_{IB}	Input Bias Current	V_O = 1.5V		-100	-1.0	nA	1
				-300	-1.0	nA	2, 3
I_{IO}	Input offset Current	R_S = 50Ω, V_O = 1.5V		-25	25	nA	1
				-100	100	nA	2, 3
V_{CM}	Common Mode Voltage	+V = 30V	(1)		28.5	V	1
			(1)		28	V	2, 3
PSRR	Power Supply Rejection Ratio	+V = 5V to 30V, R_S = 50Ω		60		dB	1
CMRR	Common Mode Rejection Ratio	+V = 30V, R_S = 50Ω V_{CM} = 0V to 28.5V,		60		dB	1
V_{Diff}	Differential Input Voltage	+V = 30V, +V_I = 36V, -V_I = 0V	(2)		500	nA	1, 2, 3
		+V = 30V, +V_I = 0V, -V_I = +36V	(2)		500	nA	1, 2, 3
A_{VS}	Voltage Gain	+V = 15V, R_{PullUp} = 15KΩ 1V ≤ V_O ≤ 11V,	(3)	50		V/mV	4
			(3)	25		V/mV	5, 6

(1)   Parameter guaranteed by the V_{IO} tests.
(2)   The value for V_{Diff} is not datalogged during Read and Record.
(3)   Datalog reading in K = V/mV.

LM193A Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified.   +V = 5V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_{OD} = 5mV			5.0	µS	9
		V_{OD} = 50mV			0.8	µS	9
t_{RHL}	Response Time	V_{OD} = 5mV			2.5	µS	9
		V_{OD} = 50mV			0.8	µS	9

Product Folder Links: *LM193A LM193QML*

LM193A Electrical Characteristics DC Drift Parameters

The following conditions apply, unless otherwise specified.   +V = 5V, V_{CM} = 0V
Delta calculations performed on QMLV devices at Group B, Subgroup 5 only

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	+V = 30V		-1.0	1.0	mV	1
$\pm I_{IB}$	Input Bias Current			-15	15	nA	1

LM193A - 100K Radiation Electrical Characteristics DC Parameters[1][2]

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Supply Current	R_L = Infinity			1.0	mA	1, 2, 3
		+V = 36V, R_L = Infinity			2.5	mA	1, 2, 3
I_{CEX}	Output Leakage Current	+V = 30V, +V_I = 1V, V_O = 30, -V_I = 0		-0.65	0.65	µA	1
				-1.0	1.0	µA	2, 3
I_{Sink}	Output Sink Current	V_O = 1.5V, -V_I = 1V, +V_I = 0V		6.0		mA	1
				4.0		mA	2, 3
V_{Sat}	Output Saturation Voltage	I_{Sink} = 4mA, -V_I = 1V, +V_I = 0V			0.4	V	1
					0.7	V	2, 3
V_{IO}	Input Offset Voltage			-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V, V_{CM} = 28.5V		-2.0	2.0	mV	1
		+V = 30V, V_{CM} = 28.0V		-4.0	4.0	mV	2, 3
$\pm I_{IB}$	Input Bias Current	V_O = 1.5V		-100	-1.0	nA	1
				-300	-1.0	nA	2, 3
I_{IO}	Input offset Current	R_S = 50Ω, V_O = 1.5V		-25	25	nA	1
				-100	100	nA	2, 3
V_{CM}	Common Mode Voltage	+V = 30V	[3]		28.5	V	1
			[3]		28	V	2, 3
PSRR	Power Supply Rejection Ratio	+V = 5V to 30V, R_S = 50Ω		60		dB	1
CMRR	Common Mode Rejection Ratio	+V = 30V, R_S = 50Ω V_{CM} = 0V to 28.5V,		60		dB	1
V_{Diff}	Differential Input Voltage	+V = 30V, +V_I = 36V, -V_I = 0V	[4]		500	nA	1, 2, 3
		+V = 30V, +V_I = 0V, -V_I = +36V	[4]		500	nA	1, 2, 3
A_{VS}	Voltage Gain	+V = 15V, R_{PullUp} = 15KΩ 1V ≤ V_O ≤ 11V,	[5]	50		V/mV	4
			[5]	25		V/mV	5, 6

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019
(2) Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.
(3) Parameter guaranteed by the V_{IO} tests.
(4) The value for V_{Diff} is not datalogged during Read and Record.
(5) Datalog reading in K = V/mV.

Product Folder Links: *LM193A LM193QML*

LM193A - 100K Radiation Electrical Characteristics AC Parameters[1][2]

The following conditions apply, unless otherwise specified.   +V = 5V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_{OD} = 5mV			5.0	µS	9
		V_{OD} = 50mV			0.8	µS	9
t_{RHL}	Response Time	V_{OD} = 5mV			2.5	µS	9
		V_{OD} = 50mV			0.8	µS	9

(1)   Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019
(2)   Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.

LM193A, LM193QML

LM193A - 100K Radiation Electrical Characteristics (Continued) DC Drift Parameters[1][2]

The following conditions apply, unless otherwise specified.   +V = 5V, V_{CM} = 0V
Delta calculations performed on QMLV devices at Group B, Subgroup 5 only

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	+V = 30V		-1.0	1.0	mV	1
$\pm I_{IB}$	Input Bias Current			-15	15	nA	1

(1)   Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019

(2)   Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.

Product Folder Links: *LM193A LM193QML*

LM193A - 100K Radiation Electrical Characteristics (Continued) AC Parameters - Post Radiation Limits @ +25°C [1][2]

The following conditions apply, unless otherwise specified.   +V = 5V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_{OD} = 50mV			1.0	µS	9

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019
(2) Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.

Typical Performance Characteristics

Supply Current

Input Current

Output Saturation Voltage
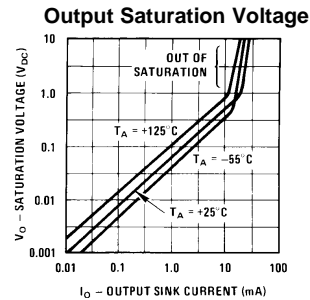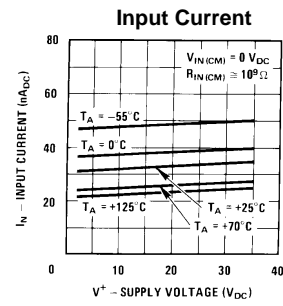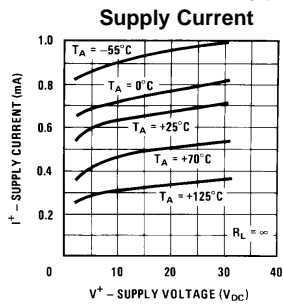
Response Time for Various Input Overdrives—Negative Transition
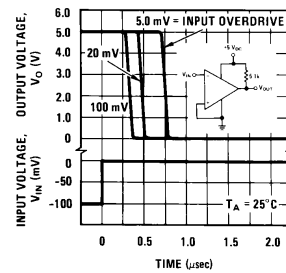
Response Time for Various Input Overdrives—Positive Transition
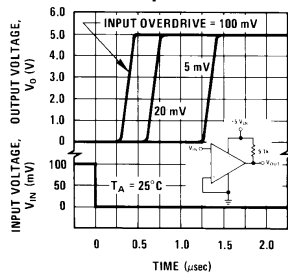
Application Hints

The LM193 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to < 10 KΩ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All input pins of any unused comparators should be tied to the negative supply.

The bias network of the LM193 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device [1]. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

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[1] Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used).

Product Folder Links: *LM193A LM193QML*

The output of the LM193 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V⁺ terminal of the LM193 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{SAT} of the output transistor. The low offset voltage of the output transistor (1.0mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications

(V^+=5.0 V_{DC})

Figure 3. Basic Comparator
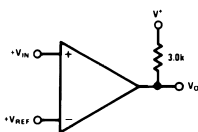
Figure 4. Driving CMOS
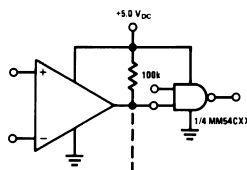
Figure 5. Driving TTL
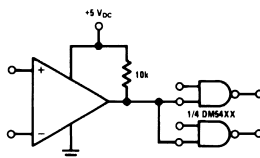
Figure 6. Squarewave Oscillator
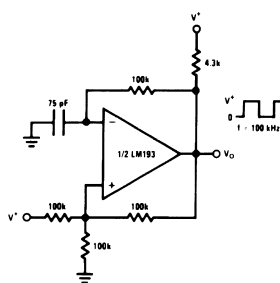
(V^+=5.0 V_{DC})

Figure 7. Pulse Generator
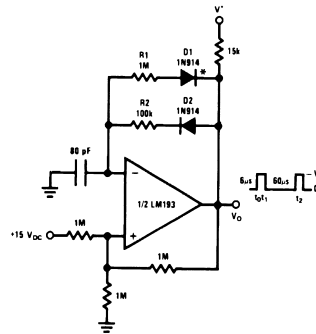
* For large ratios of R1/R2,
D1 can be omitted.

Figure 8. Crystal Controlled Oscillator
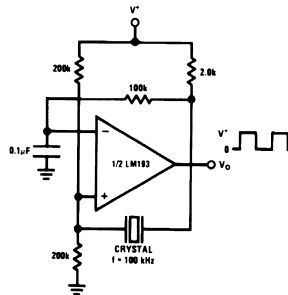
Figure 9. Two-Decade High Frequency VCO
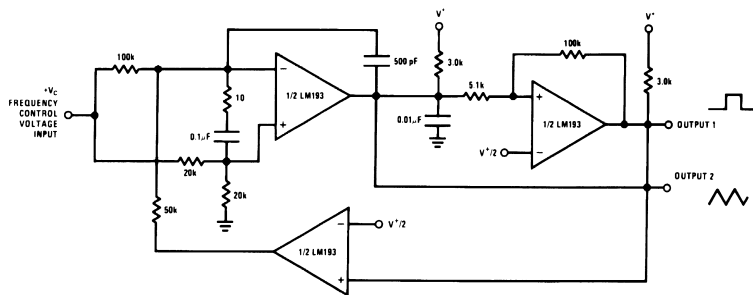
V^* = +30 V_{DC}
+250 mV_{DC} ≤ V_C ≤ +50 V_{DC}
700Hz ≤ f_o ≤ 100kHz

Figure 10. Basic Comparator

Product Folder Links: *LM193A LM193QML*
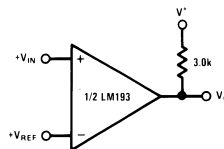
$(V^+ = 5.0\ V_{DC})$

Figure 11. Non-Inverting Comparator with Hysteresis
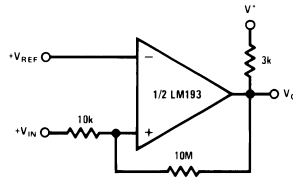
Figure 12. Inverting Comparator with Hysteresis
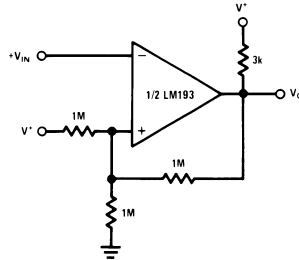
Figure 13. Output Strobing
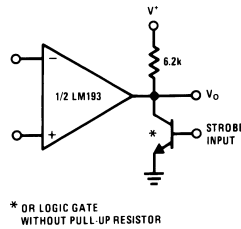
Figure 14. AND Gate
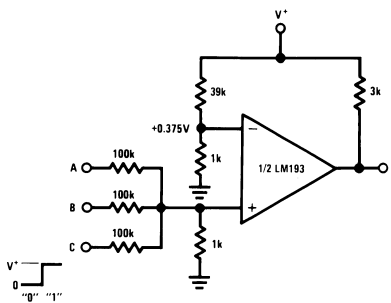
Figure 15. OR Gate
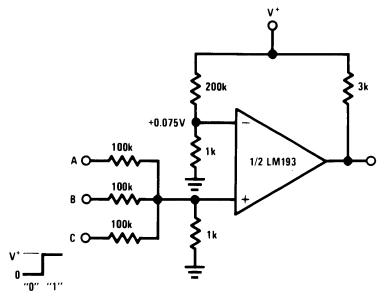
(V^+=5.0 V_{DC})

Figure 16. Large Fan-in AND Gate
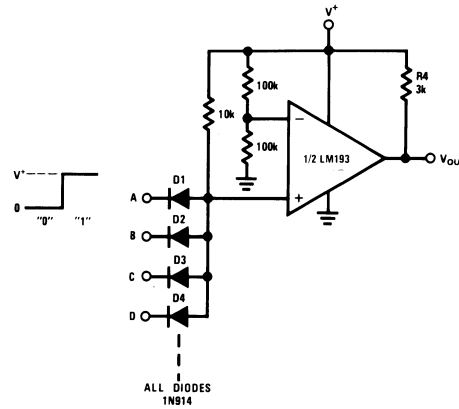
Figure 17. Limit Comparator
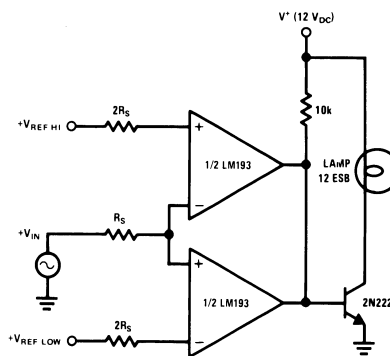
Figure 18. Comparing Input Voltages of Opposite Polarity
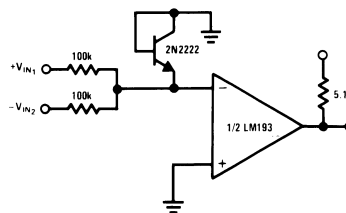
Figure 19. ORing the Outputs

Product Folder Links: *LM193A LM193QML*
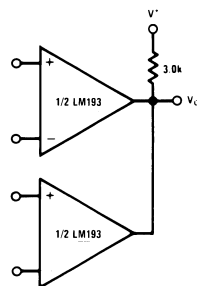
(V^+=5.0 V_{DC})

Figure 20. Zero Crossing Detector (Single Power Supply)
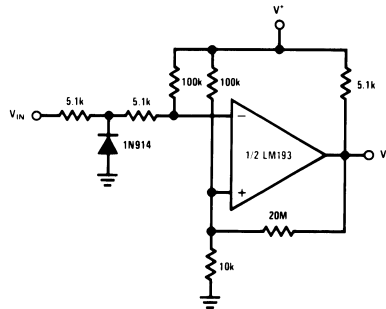
Figure 21. One-Shot Multivibrator
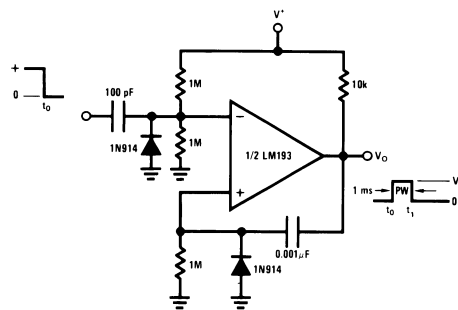
Figure 22. Bi-Stable Multivibrator
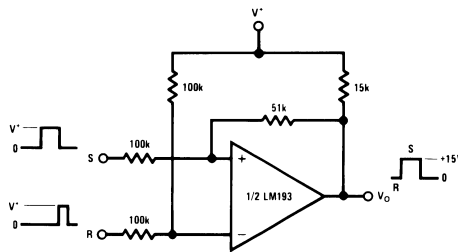
Figure 23. One-Shot Multivibrator with Input Lock Out
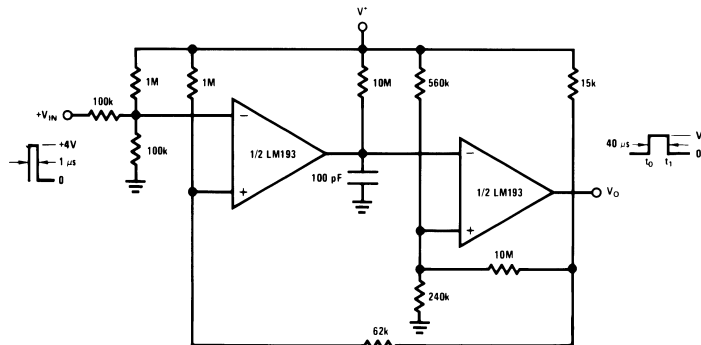
(V^+=5.0 V_{DC})

Figure 24. Zero Crossing Detector
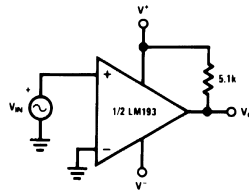
Figure 25. Comparator With a Negative Reference
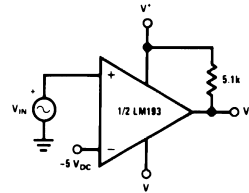
Figure 26. Time Delay Generator
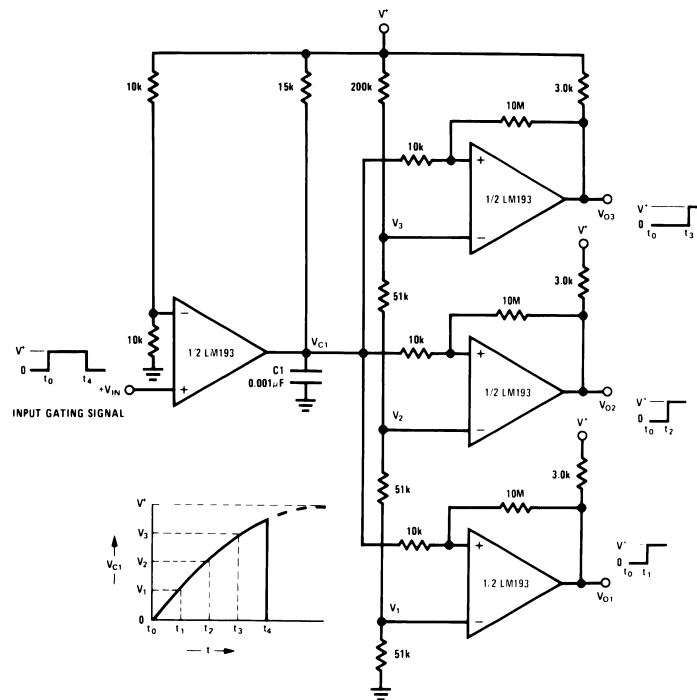
Split-Supply Applications

(V^+=+15 V_{DC} and V^-=−15 V_{DC})

Product Folder Links: *LM193A LM193QML*

(V^+=+15 V_{DC} and V^-=−15 V_{DC})

Figure 27. MOS Clock Driver
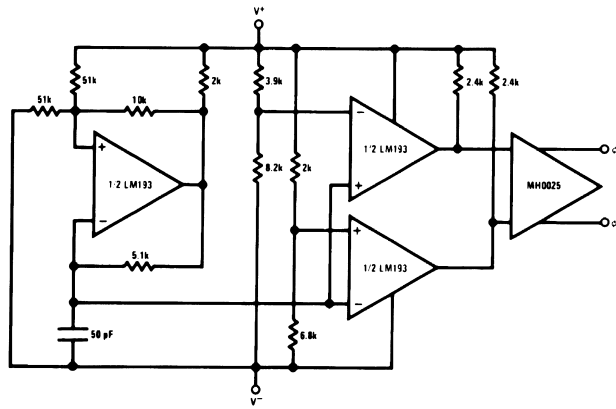
Table 1. Revision History

Date Released	Revision	Section	Originator	Changes
05/09/05	A	New Release. Corporate format	L. Lytle	2 MDS datasheets converted into one Corp. datasheet format. MNLM193A-X Rev 1B3 & MNLM193–X Rev 0E1. The Iout Vsat condition for LM193 was changed to Isink for consistency with the LM193A and JAN electrical conditions. Also, redundant parameters were removed from conditions that were defined at beginning of the table. MDS data sheets will be archived.
05/07/07	B	Features, Ordering Information, LM193A Electricals	Larry McGee	Added Radiation Electrical information for LM193A Device. Revision A will be archived.
10/29/07	C	Features, Ordering Information, Notes	Larry McGee	Added reference to New ELDS NSID and SMD Device 03, ELDRS Note 12. Revision B will be archived.

Product Folder Links: *LM193A LM193QML*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
5962-9452602MGA	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM193AH/883 5962-9452602MGA Q ACO 5962-9452602MGA Q >T	Samples
5962-9452602MPA	ACTIVE	CDIP	NAB	8	40	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM193AJ/883 5962-94526 02MPA Q ACO 02MPA Q >T	Samples
5962-9452602VPA	ACTIVE	CDIP	NAB	8	40	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM193AJ-QMLV 5962-94526 02VPA Q ACO 02VPA Q >T	Samples
5962R9452602VGA	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM193AHRQMLV 5962R9452602VGA Q ACO 5962R9452602VGA Q >T	Samples
5962R9452602VPA	ACTIVE	CDIP	NAB	8	40	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM193AJRQMLV 5962R94526 02VPA Q ACO 02VPA Q >T	Samples
5962R9452603VGA	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM193AHRLQMLV 5962R9452603VGA Q ACO 5962R9452603VGA Q >T	Samples
5962R9452603VPA	ACTIVE	CDIP	NAB	8	40	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM193AJRLV 5962R94526 03VPA Q ACO 03VPA Q >T	Samples
LM193AH/883	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM193AH/883 5962-9452602MGA Q ACO 5962-9452602MGA Q >T	Samples
LM193AHRLQMLV	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM193AHRLQMLV 5962R9452603VGA Q ACO 5962R9452603VGA Q >T	Samples
LM193AHRQMLV	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM193AHRQMLV 5962R9452602VGA Q ACO 5962R9452602VGA Q >T	Samples
LM193AJ-QMLV	ACTIVE	CDIP	NAB	8	40	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM193AJ-QMLV 5962-94526 02VPA Q ACO	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
										02VPA Q >T	
LM193AJ/883	ACTIVE	CDIP	NAB	8	40	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM193AJ/883 5962-94526 02MPA Q ACO 02MPA Q >T	Samples
LM193AJRLQMLV	ACTIVE	CDIP	NAB	8	40	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM193AJRLV 5962R94526 03VPA Q ACO 03VPA Q >T	Samples
LM193AJRQMLV	ACTIVE	CDIP	NAB	8	40	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM193AJRQMLV 5962R94526 02VPA Q ACO 02VPA Q >T	Samples
LM193H/883	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM193H/883 Q ACO LM193H/883 Q >T	Samples
LM193J/883	ACTIVE	CDIP	NAB	8	40	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM193J /883 Q ACO /883 Q >T	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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OTHER QUALIFIED VERSIONS OF LM193QML, LM193QML-SP :

● Military: LM193QML

● Space: LM193QML-SP

NOTE: Qualified Version Definitions:

      ● Military - QML certified for Military and Defense Applications

      ● Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

NAB0008A

.400 MAX
[10.16]

8   5

.310 MAX
[7.87]

R.025
[0.64]

R.010 TYP
[0.25]

1   4
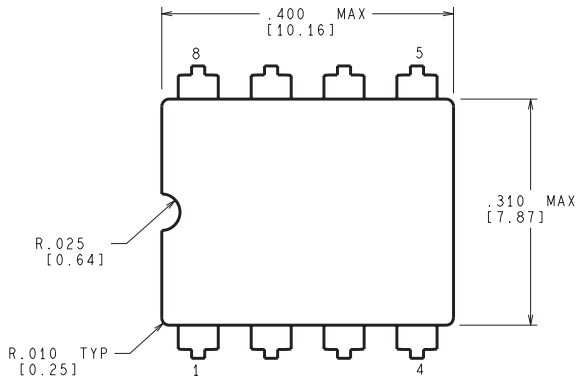
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

8X .055±.010
[1.4±0.25]

.200 MAX TYP
[5.08]

.180 MAX
[4.57]

8X .125-.200
[3.18-5.08]

90°±4°
TYP

.020-.060
[0.51-1.52]
TYP

8X .018±.003
[0.46±0.07]

.055 MAX TYP
[1.40]

6X .100±.010
[2.54±0.25]

.290-.320
[7.37-8.13]

GLASS SEALANT

95°±5°
TYP

8X .010±.002
[0.25±0.05]

.310-.410
[7.87-10.41]

J08A (Rev M)
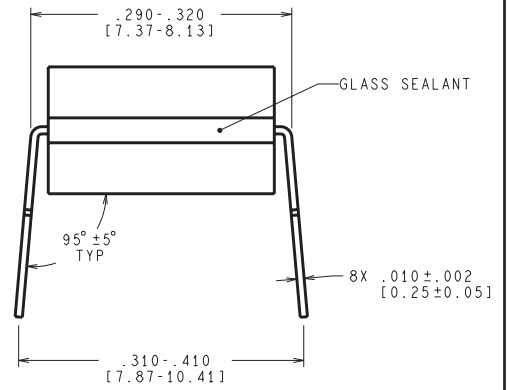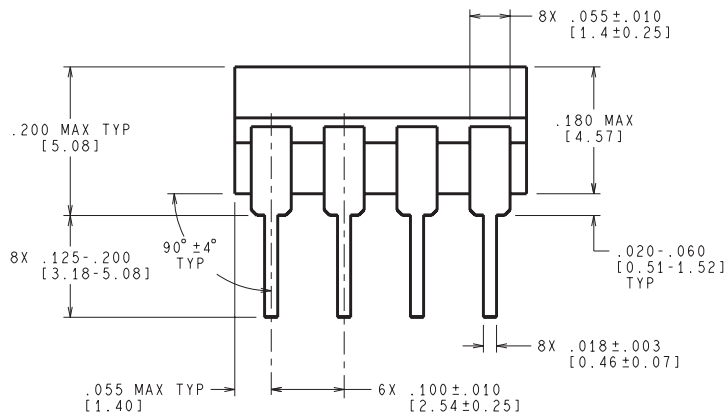
Texas
Instruments
www.ti.com

LMC (O–MBCY–W8)   **METAL CYLINDRICAL PACKAGE**

ϕ $\dfrac{0.370\ (9,40)}{0.335\ (8,51)}$

ϕ $\dfrac{0.335\ (8,51)}{0.305\ (7,75)}$

$\dfrac{0.040\ (1,02)}{0.010\ (0,25)}$

$\dfrac{0.185\ (4,70)}{0.165\ (4,19)}$

0.040 (1,02) MAX

Seating Plane

0.500 (12,70) MIN

ϕ $\dfrac{0.021\ (0,53)}{0.016\ (0,41)}$

$\dfrac{0.105\ (2,67)}{0.095\ (2,41)}$

ϕ $\dfrac{0.160\ (4,06)}{0.110\ (2,79)}$

$\dfrac{0.105\ (2,67)}{0.095\ (2,41)}$

0.200 (5,08)a

45°

$\dfrac{0.034\ (0,86)}{0.028\ (0,71)}$

$\dfrac{0.045\ (1,14)}{0.029\ (0,74)}$

4202483/B 09/07
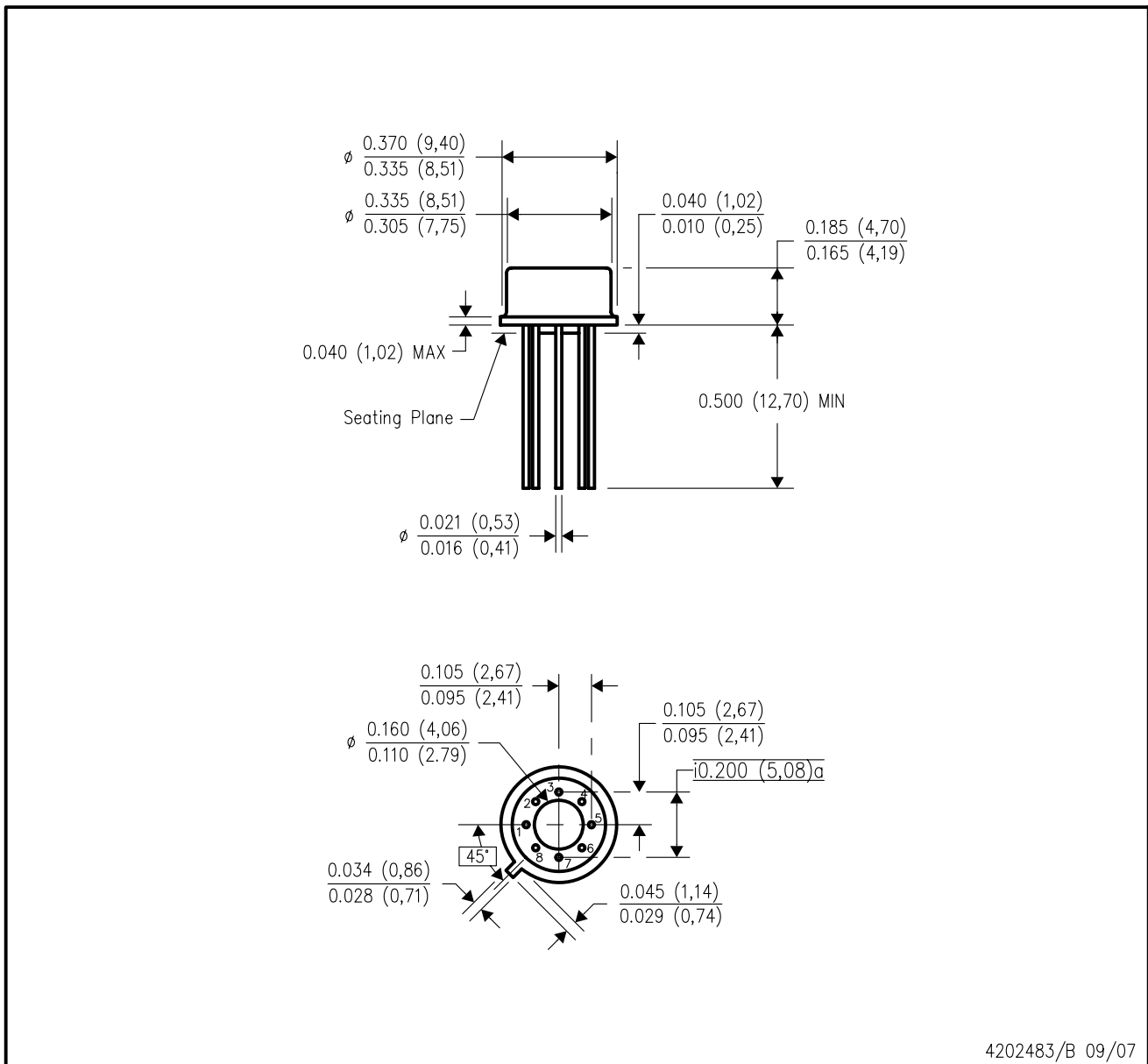
NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
         D.   Pin numbers shown for reference only. Numbers may not be marked on package.
         E.   Falls within JEDEC MO–002/TO–99.

IMPORTANT NOTICE

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DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
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Logic	logic.ti.com	Security	www.ti.com/security
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OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
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