

LMH6622 Dual Wideband, Low Noise, 160MHz, Operational Amplifiers

Check for Samples: [LMH6622](#)

FEATURES

- $V_S = \pm 6V$, $T_A = 25^\circ C$, Typical values unless specified
- Bandwidth ($A_V = +2$) 160MHz
- Supply Voltage Range $\pm 2.5V$ to $\pm 6V + 5V$ to $+12V$
- Slew rate 85V/ μs
- Supply current 4.3mA/amp
- Input common mode voltage $-4.75V$ to $+5.7V$
- Output Voltage Swing ($R_L = 100\Omega$) $\pm 4.6V$
- Input voltage noise $1.6nV/\sqrt{Hz}$

- Input current noise $1.5pA/\sqrt{Hz}$
- Linear output current 90mA
- Excellent harmonic distortion 90dBc

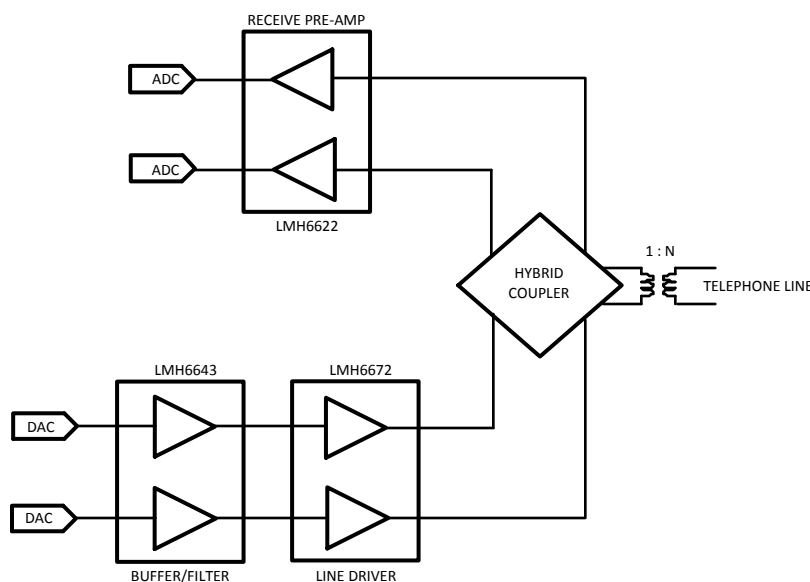
APPLICATIONS

- xDSL receiver
- Low noise instrumentation front end
- Ultrasound preamp
- Active filters
- Cellphone basestation

DESCRIPTION

The LMH6622 is a dual high speed voltage feedback operational amplifier specifically optimized for low noise. A voltage noise specification of $1.6nV/\sqrt{Hz}$, a current noise specification $1.5pA/\sqrt{Hz}$, a bandwidth of 160MHz, and a harmonic distortion specification that exceeds 90dBc combine to make the LMH6622 an ideal choice for the receive channel amplifier in ADSL, VDSL, or other xDSL designs. The LMH6622 operates from $\pm 2.5V$ to $\pm 6V$ in dual supply mode and from $+5V$ to $+12V$ in single supply configuration. The LMH6622 is stable for $A_V \geq 2$ or $A_V \leq -1$. The fabrication of the LMH6622 on National Semiconductor's advanced VIP10 process enables excellent (160MHz) bandwidth at a current consumption of only 4.3mA/amplifier. Packages for this dual amplifier are the 8-lead SOIC and the 8-lead MSOP.

xDSL Analog Front End



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



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Absolute Maximum Ratings ⁽¹⁾

ESD Tolerance	
Human Body Model	2kV ⁽²⁾
Machine Model	200V ⁽²⁾
V _{IN} Differential	±1.2V
Supply Voltage (V ⁺ – V ⁻)	13.2V
Voltage at Input Pins	V ⁺ +0.5V, V ⁻ -0.5V
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering (10 sec)	260°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature ⁽³⁾	+150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

(2) Human body model, 1.5kΩ in series with 100pF. Machine model, 0Ω in series with 200pF.

(3) The maximum power dissipation is a function of T_{J(MAX)}, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} – T_A)/θ_{JA}. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings ⁽¹⁾

Supply Voltage (V ⁺ – V ⁻)	±2.25V to ±6V
Junction Temperature Range ^{(2), (3)}	-40°C to +85°C
Package Thermal Resistance ⁽³⁾ (θ _{JA})	
8-pin SOIC	166°C/W
8-pin MSOP	211°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

(2) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

(3) The maximum power dissipation is a function of T_{J(MAX)}, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} – T_A)/θ_{JA}. All numbers apply for packages soldered directly onto a PC board.

±6V Electrical Characteristics

Unless otherwise specified, $T_J = 25^\circ\text{C}$, $V^+ = 6\text{V}$, $V^- = -6\text{V}$, $V_{CM} = 0\text{V}$, $A_V = +2$, $R_F = 500\Omega$, $R_L = 100\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Dynamic Performance						
f_{CL}	-3dB BW	$V_O = 200\text{mV}_{PP}$		160		MHz
$BW_{0.1dB}$	0.1dB Gain Flatness	$V_O = 200\text{mV}_{PP}$		30		MHz
SR	Slew Rate (3)	$V_O = 2V_{PP}$		85		V/ μs
TS	Settling Time	$V_O = 2V_{PP}$ to $\pm 0.1\%$		40		ns
		$V_O = 2V_{PP}$ to $\pm 1.0\%$		35		
Tr	Rise Time	$V_O = 0.2\text{V}$ Step, 10% to 90%		2.3		ns
Tf	Fall Time	$V_O = 0.2\text{V}$ Step, 10% to 90%		2.3		ns
Distortion and Noise Response						
e_n	Input Referred Voltage Noise	$f = 100\text{kHz}$		1.6		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Referred Current Noise	$f = 100\text{kHz}$		1.5		$\text{pA}/\sqrt{\text{Hz}}$
DG	Differential Gain	$R_L = 150\Omega$, $R_F = 470\Omega$, NTSC		0.03		%
DP	Differential Phase	$R_L = 150\Omega$, $R_F = 470\Omega$, NTSC		0.03		deg
HD2	2 nd Harmonic Distortion	$f_c = 1\text{MHz}$, $V_O = 2V_{PP}$, $R_L = 100\Omega$		-90		dBc
		$f_c = 1\text{MHz}$, $V_O = 2V_{PP}$, $R_L = 500\Omega$		-100		
HD3	3 rd Harmonic Distortion	$f_c = 1\text{MHz}$, $V_O = 2V_{PP}$, $R_L = 100\Omega$		-94		dBc
		$f_c = 1\text{MHz}$, $V_O = 2V_{PP}$, $R_L = 500\Omega$		-100		
MTPR	Upstream	$V_O = 0.6 V_{RMS}$, 26kHz to 132kHz (see test circuit 5)		-78		dBc
	Downstream	$V_O = 0.6 V_{RMS}$, 144kHz to 1.1MHz (see test circuit 5)		-70		
Input Characteristics						
V_{OS}	Input Offset Voltage	$V_{CM} = 0\text{V}$	-1.2 -2	+0.2	+1.2 +2	mV
TC V_{OS}	Input Offset Average Drift	$V_{CM} = 0\text{V}$ (4)		-2.5		$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current	$V_{CM} = 0\text{V}$	-1 -1.5	-0.04	1 1.5	μA
I_B	Input Bias Current	$V_{CM} = 0\text{V}$		4.7	10 15	μA
R_{IN}	Input Resistance	Common Mode		17		M Ω
		Differential Mode		12		k Ω
C_{IN}	Input Capacitance	Common Mode		0.9		pF
		Differential Mode		1.0		pF
CMVR	Input Common Mode Voltage Range	CMRR $\geq 60\text{dB}$		-4.75	-4.5	V
			5.5	+5.7		
CMRR	Common-Mode Rejection Ratio	Input Referred, $V_{CM} = -4.2$ to $+5.2\text{V}$	80 75	100		dB
Transfer Characteristics						
A_{VOL}	Large Signal Voltage Gain	$V_O = 4V_{PP}$	74 70	83		dB
X_t	Crosstalk	$f = 1\text{MHz}$		-75		dB
Output Characteristics						

(1) All limits are guaranteed by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm.

(3) Slew rate is the slowest of the rising and falling slew rates.

(4) Offset voltage average drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

±6V Electrical Characteristics (continued)

Unless otherwise specified, $T_J = 25^\circ\text{C}$, $V^+ = 6\text{V}$, $V^- = -6\text{V}$, $V_{\text{CM}} = 0\text{V}$, $A_V = +2$, $R_F = 500\Omega$, $R_L = 100\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_O	Output Swing	No Load, Positive Swing	4.8 4.6	5.2		V
		No Load, Negative Swing		-5.0	-4.6 -4.4	
		$R_L = 100\Omega$, Positive Swing	4.0 3.8	4.6		
		$R_L = 100\Omega$, Negative Swing		-4.6	-4 -3.8	
R_O	Output Impedance	$f = 1\text{MHz}$		0.08		Ω
I_{SC}	Output Short Circuit Current	Sourcing to Ground $\Delta V_{\text{IN}} = 200\text{mV}$ (5), (6)	100	135		mA
		Sinking to Ground $\Delta V_{\text{IN}} = -200\text{mV}$ (5), (6)	100	130		
I_{OUT}	Output Current	Sourcing, $V_O = +4.3\text{V}$ Sinking, $V_O = -4.3\text{V}$		90		mA
Power Supply						
+PSRR	Positive Power Supply Rejection Ratio	Input Referred, $V_S = +5\text{V}$ to $+6\text{V}$	80 74	95		dB
-PSRR	Negative Power Supply Rejection Ratio	Input Referred, $V_S = -5\text{V}$ to -6V	75 69	90		
I_S	Supply Current (per amplifier)	No Load		4.3	6 6.5	mA

- (5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C .
- (6) Short circuit test is a momentary test. Output short circuit duration is infinite for $V_S \leq \pm 2.5\text{V}$, at room temperature and below. For $V_S > \pm 2.5\text{V}$, allowable short circuit duration is 1.5ms.

±2.5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 2.5\text{V}$, $V^- = -2.5\text{V}$, $V_{CM} = 0\text{V}$, $A_V = +2$, $R_F = 500\Omega$, $R_L = 100\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Dynamic Performance						
f_{CL}	-3dB BW	$V_O = 200\text{mV}_{PP}$		150		MHz
$BW_{0.1dB}$	0.1dB Gain Flatness	$V_O = 200\text{mV}_{PP}$		20		MHz
SR	Slew Rate (3)	$V_O = 2V_{PP}$		80		V/ μs
T_S	Settling Time	$V_O = 2V_{PP}$ to $\pm 0.1\%$		45		ns
		$V_O = 2V_{PP}$ to $\pm 1.0\%$		40		
T_r	Rise Time	$V_O = 0.2\text{V}$ Step, 10% to 90%		2.5		ns
T_f	Fall Time	$V_O = 0.2\text{V}$ Step, 10% to 90%		2.5		ns
Distortion and Noise Response						
e_n	Input Referred Voltage Noise	$f = 100\text{kHz}$		1.7		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Referred Current Noise	$f = 100\text{kHz}$		1.5		$\text{pA}/\sqrt{\text{Hz}}$
HD2	2 nd Harmonic Distortion	$f_c = 1\text{MHz}$, $V_O = 2V_{PP}$, $R_L = 100\Omega$		-88		dBc
		$f_c = 1\text{MHz}$, $V_O = 2V_{PP}$, $R_L = 500\Omega$		-98		
HD3	3 rd Harmonic Distortion	$f_c = 1\text{MHz}$, $V_O = 2V_{PP}$, $R_L = 100\Omega$		-92		dBc
		$f_c = 1\text{MHz}$, $V_O = 2V_{PP}$, $R_L = 500\Omega$		-100		
MTPR	Upstream	$V_O = 0.4V_{RMS}$, 26kHz to 132kHz (see test circuit 5)		-76		dBc
	Downstream	$V_O = 0.4V_{RMS}$, 144kHz to 1.1MHz (see test circuit 5)		-68		
Input Characteristics						
V_{OS}	Input Offset Voltage	$V_{CM} = 0\text{V}$	-1.5 -2.3	+0.3	+1.5 +2.3	mV
TC V_{OS}	Input Offset Average Drift	$V_{CM} = 0\text{V}$ (4)		-2.5		$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current	$V_{CM} = 0\text{V}$	-1.5 -2.5	+0.01	1.5 2.5	μA
I_B	Input Bias Current	$V_{CM} = 0\text{V}$		4.6	10 15	μA
R_{IN}	Input Resistance	Common Mode		17		M Ω
		Differential Mode		12		k Ω
C_{IN}	Input Capacitance	Common Mode		0.9		pF
		Differential Mode		1.0		pF
CMVR	Input Common Mode Voltage Range	CMRR $\geq 60\text{dB}$		-1.25	-1	V
			2	+2.2		
CMRR	Common Mode Rejection Ratio	Input Referred, $V_{CM} = -0.7$ to $+1.7\text{V}$	80 75	100		dB
Transfer Characteristics						
A_{VOL}	Large Signal Voltage Gain	$V_O = 1V_{PP}$	74	82		dB
X_t	Crosstalk	$f = 1\text{MHz}$		-75		dB
Output Characteristics						

(1) All limits are guaranteed by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm.

(3) Slew rate is the slowest of the rising and falling slew rates.

(4) Offset voltage average drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

±2.5V Electrical Characteristics (continued)

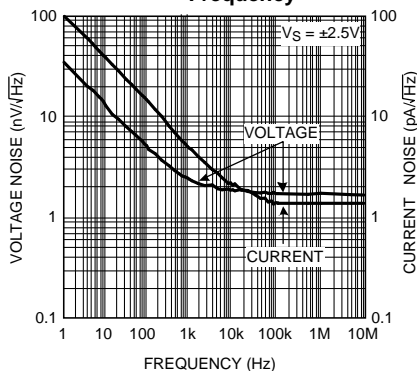
Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 2.5\text{V}$, $V^- = -2.5\text{V}$, $V_{\text{CM}} = 0\text{V}$, $A_V = +2$, $R_F = 500\Omega$, $R_L = 100\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_O	Output Swing	No Load, Positive Swing	1.4 1.2	1.7		V
		No Load, Negative Swing		-1.5	-1.2 -1	
		$R_L = 100\Omega$, Positive Swing	1.2 1	1.5		
		$R_L = 100\Omega$, Negative Swing		-1.4	-1.1 -0.9	
R_O	Output Impedance	$f = 1\text{MHz}$		0.1		Ω
I_{SC}	Output Short Circuit Current	Sourcing to Ground $\Delta V_{\text{IN}} = 200\text{mV}$ (5), (6)	100	137		mA
		Sinking to Ground $\Delta V_{\text{IN}} = -200\text{mV}$ (5), (6)	100	134		
I_{OUT}	Output Current	Sourcing, $V_O = +0.8\text{V}$ Sinking, $V_O = -0.8\text{V}$		90		mA
Power Supply						
+PSRR	Positive Power Supply Rejection Ratio	Input Referred, $V_S = +2.5\text{V}$ to $+3\text{V}$	78 72	93		dB
-PSRR	Negative Power Supply Rejection Ratio	Input Referred, $V_S = -2.5\text{V}$ to -3V	75 70	88		dB
I_S	Supply Current (per amplifier)	No Load		4.1	5.8 6.4	mA

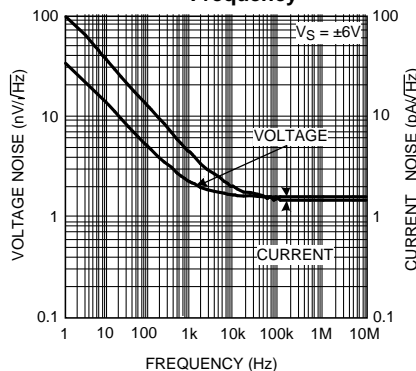
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- (6) Short circuit test is a momentary test. Output short circuit duration is infinite for $V_S \leq \pm 2.5\text{V}$, at room temperature and below. For $V_S > \pm 2.5\text{V}$, allowable short circuit duration is 1.5ms.

Typical Performance Characteristics

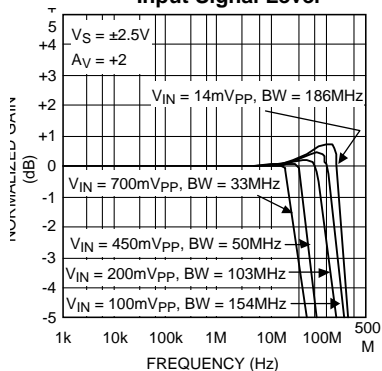
Current and Voltage Noise vs. Frequency



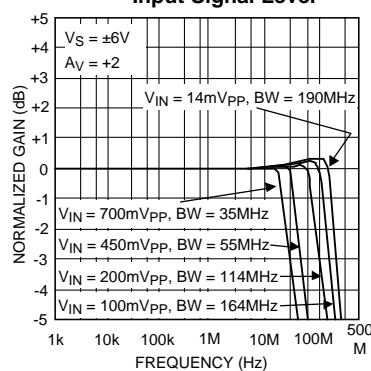
Current and Voltage Noise vs. Frequency



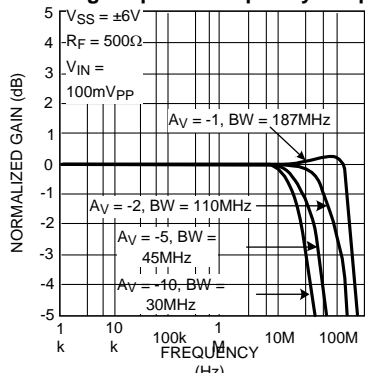
Frequency Response vs. Input Signal Level



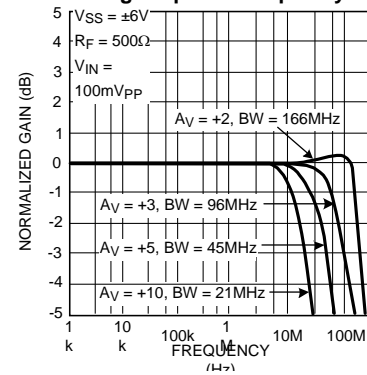
Frequency Response vs. Input Signal Level



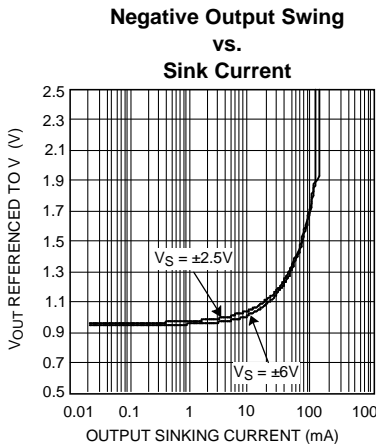
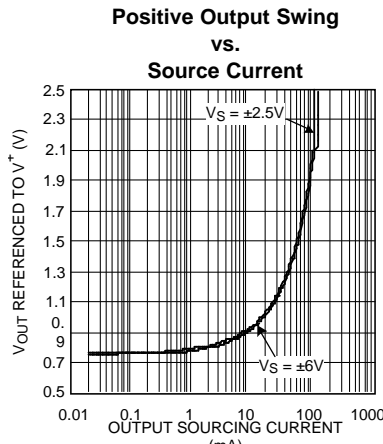
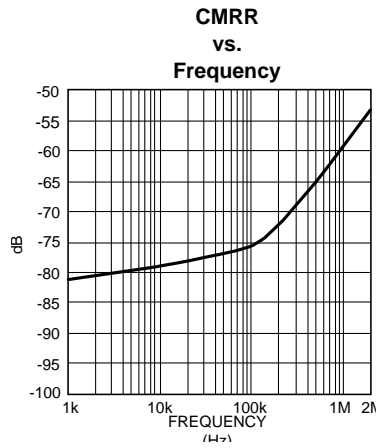
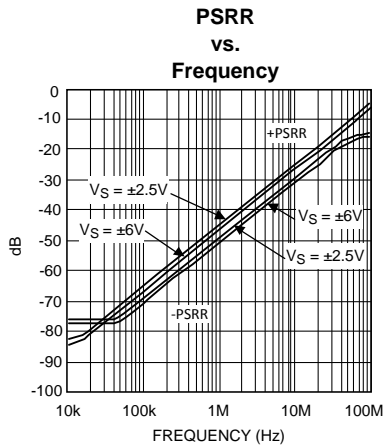
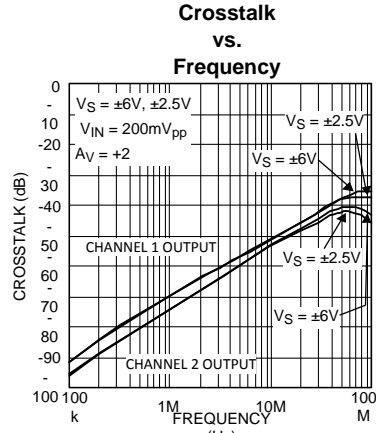
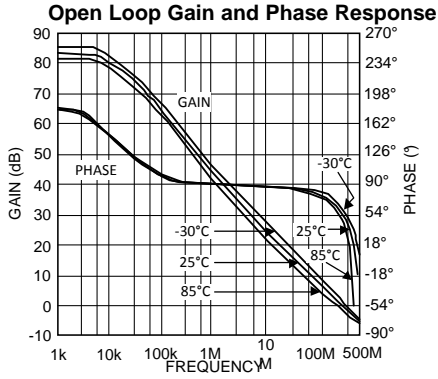
Inverting Amplifier Frequency Response



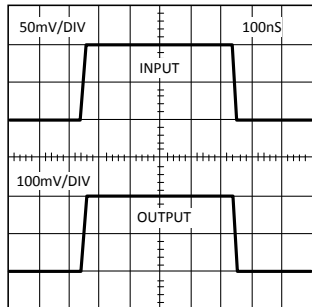
Non-Inverting Amplifier Frequency Response



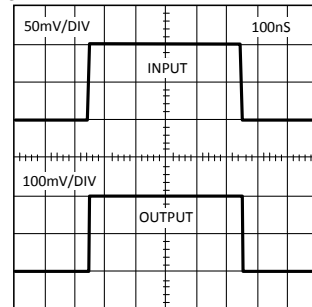
Typical Performance Characteristics (continued)



Non-Inverting Small Signal Pulse Response
 $V_S = \pm 2.5V, R_L = 100\Omega, A_V = +2, R_F = 500\Omega$

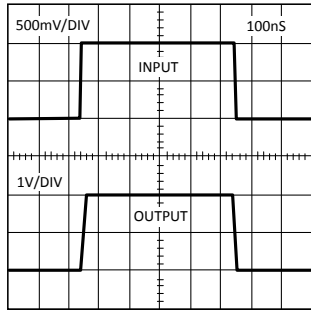


Non-Inverting Small Signal Pulse Response
 $V_S = \pm 6V, R_L = 100\Omega, A_V = +2, R_F = 500\Omega$

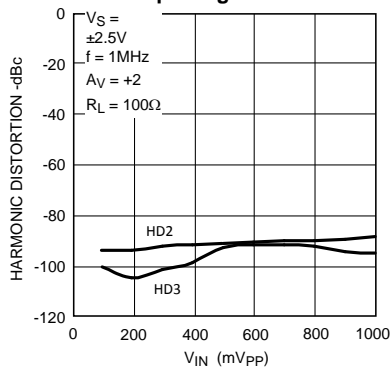


Typical Performance Characteristics (continued)

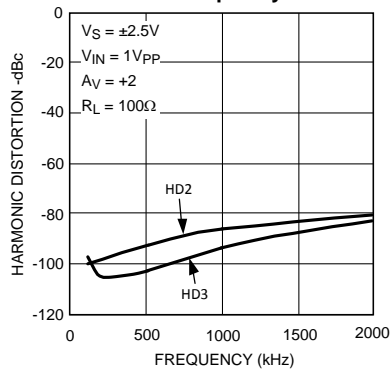
Non-Inverting Large Signal Pulse Response
 $V_S = \pm 2.5V$, $R_L = 100\Omega$, $A_V = +2$, $R_F = 500\Omega$



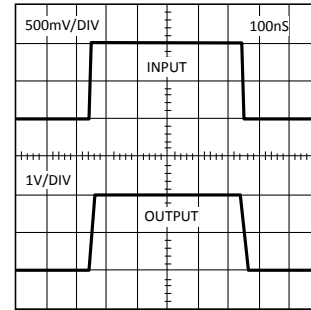
Harmonic Distortion
 vs.
 Input Signal Level



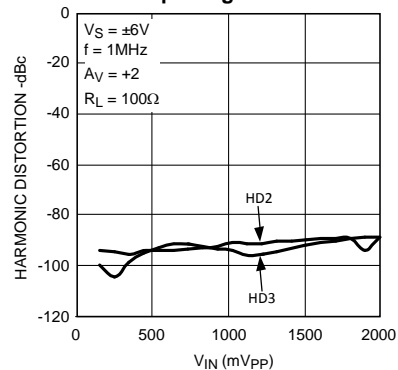
Harmonic Distortion
 vs.
 Frequency



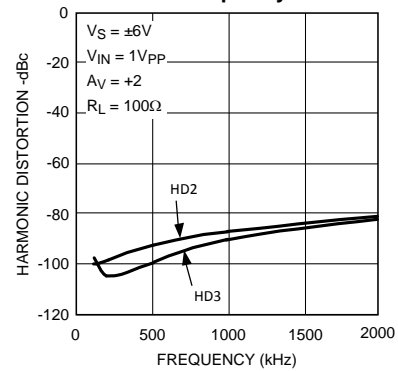
Non-Inverting Large Signal Pulse Response
 $V_S = \pm 6V$, $R_L = 100\Omega$, $A_V = +2$, $R_F = 500\Omega$



Harmonic Distortion
 vs.
 Input Signal Level

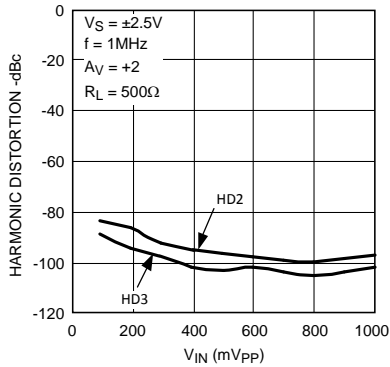


Harmonic Distortion
 vs.
 Frequency

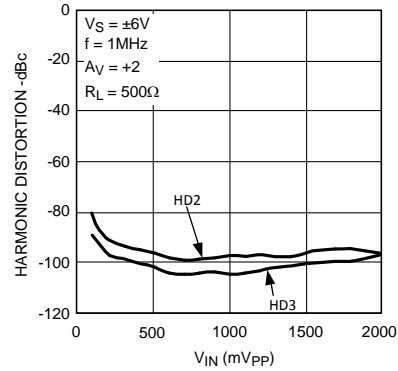


Typical Performance Characteristics (continued)

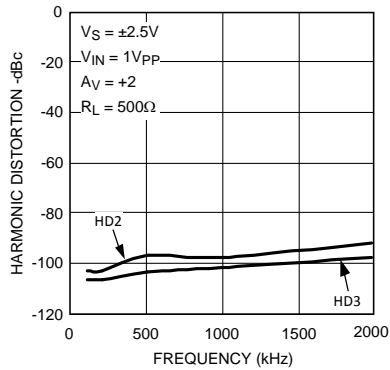
Harmonic Distortion vs. Input Signal Level



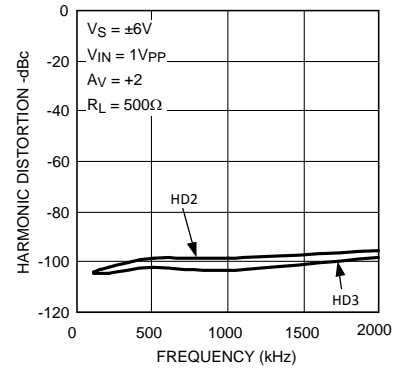
Harmonic Distortion vs. input Signal Level



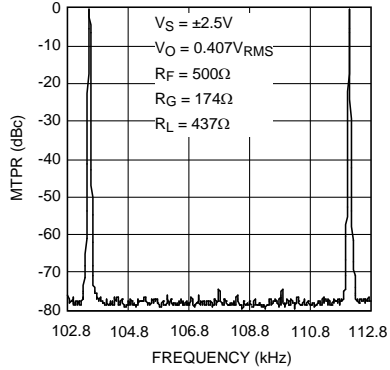
Harmonic Distortion vs. Input Frequency



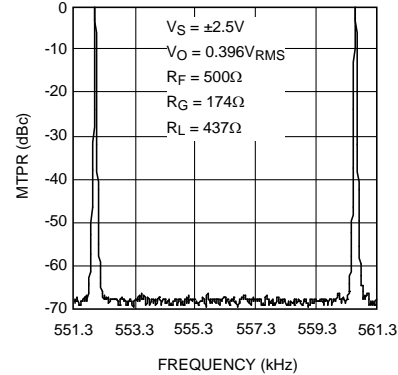
Harmonic Distortion vs. Input Frequency



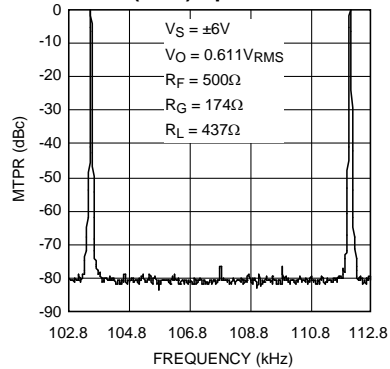
Full Rate ADSL (DMT) Upstream MTPR @ VS = ±2.5V



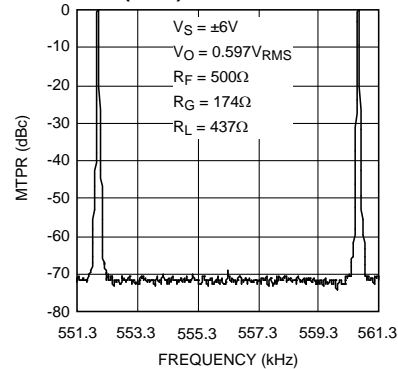
Full Rate ADSL (DMT) Downstream MTPR @ VS = ±2.5V



Full Rate ADSL (DMT) Upstream MTPR @ VS = ±6V



Full Rate ADSL (DMT) Downstream MTPR @ VS = ±6V



Connection Diagram

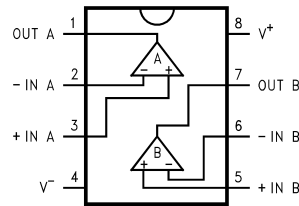


Figure 1. 8-Pin SOIC/MSOP (Top View)

Test Circuits

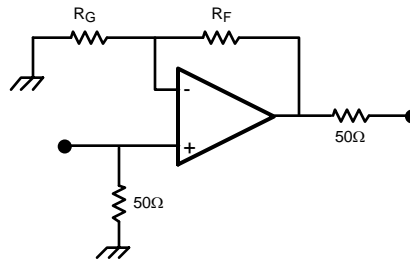


Figure 2. Non-Inverting Amplifier

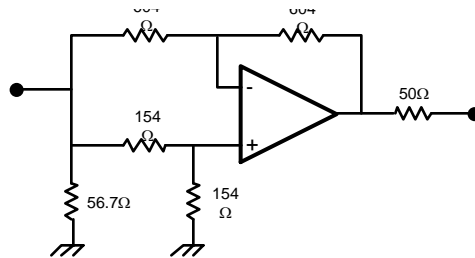


Figure 3. CMRR

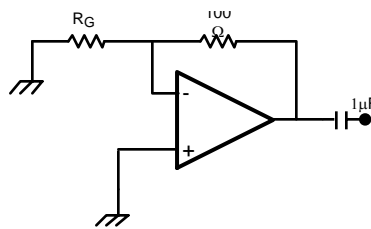


Figure 4. Voltage Noise
 $R_G = 1\Omega$ for $f \leq 100\text{kHz}$, $R_G = 20\Omega$ for $f > 100\text{kHz}$

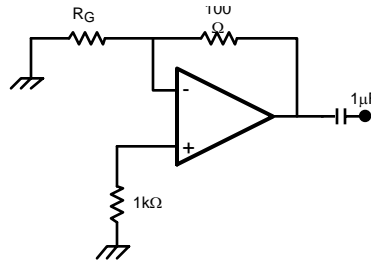


Figure 5. Current Noise
 $R_G = 1\Omega$ for $f \leq 100\text{kHz}$, $R_G = 20\Omega$ for $f > 100\text{kHz}$

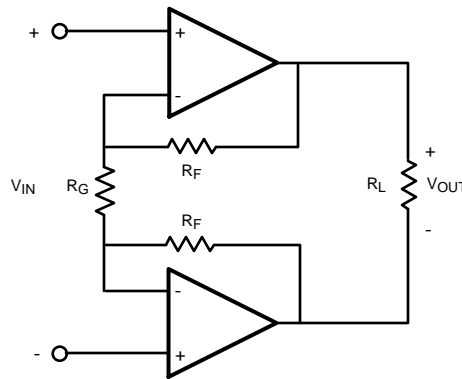


Figure 6. Multitone Power Ratio, $R_F = 500\Omega$, $R_G = 174\Omega$, $R_L = 437\Omega$

DSL Receive Channel Applications

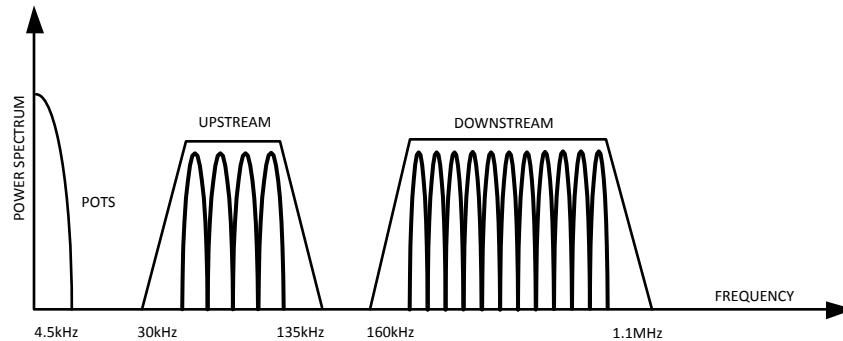


Figure 7. ADSL Signal Description

The LMH6622 is a dual, wideband operational amplifier designed for use as a DSL line receiver. In the receive band of a Customer Premises Equipment (CPE) ADSL modem it is possible that as many as 255 Discrete Multi-Tone (DMT) QAM signals will be present, each with its own carrier frequency, modulation, and signal level. The ADSL standard requires a line referred noise power density of -140dBm/Hz within the CPE receive band of 100KHz to 1.1MHz. The CPE driver output signal will leak into the receive path because of full duplex operation and the imperfections of the hybrid coupler circuit. The DSL analog front end must incorporate a receiver pre-amp which is both low noise and highly linear for ADSL-standard operation. The LMH6622 is designed for the twin performance parameters of low noise and high linearity.

Applications ranging from +5V to +12V or $\pm 2.5\text{V}$ to $\pm 6\text{V}$ are fully supported by the LMH6622. In [Figure 8](#), the LMH6622 is used as an inverting summing amplifier to provide both received pre-amp channel gain and driver output signal cancellation, i.e., the function of a hybrid coupler.

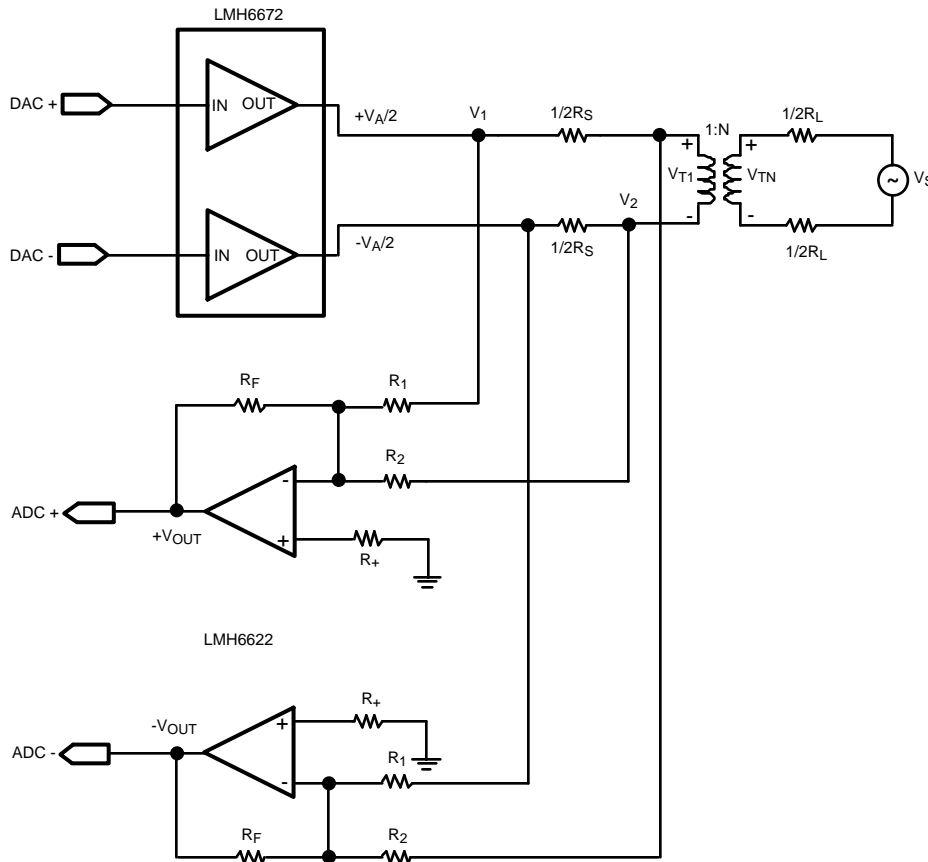


Figure 8. ADSL Receive Applications Circuit

The two R_S resistors are used to provide impedance matching through the 1:N transformer.

$$R_S = \frac{R_L}{N^2} \tag{1}$$

Where R_L is the impedance of the twisted pair line.

N is the turns ratio of the transformer.

The resistors R_2 and R_F are used to set the receive gain of the pre-amp. The receive gain is selected to meet the ADC full-scale requirement of a DSL chipset.

Resistor R_1 and R_2 along with R_F are used to achieve cancellation of the output driver signal at the output of the receiver.

Since the LMH6622 is configured as an inverting summing amplifier, V_{OUT} is found to be,

$$V_{OUT} = -R_F \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} \right] \tag{2}$$

The expression for V_1 and V_2 can be found by using superposition principle.

When $V_S = 0$,

$$V_1 = \frac{1}{2}V_A \text{ and } V_2 = -\frac{1}{4}V_A \tag{3}$$

When $V_A = 0$,

$$V_1 = 0 \text{ and } V_2 = -\frac{1}{2}V_{T1} \tag{4}$$

Therefore,

$$V_1 = \frac{1}{2}V_A \quad \text{and} \quad V_2 = -\frac{1}{4}V_A \cdot \frac{1}{2}V_{T1} \quad (5)$$

And then,

$$V_{OUT} = -R_F \left[\frac{V_A}{2R_1} - \frac{V_A}{4R_2} - \frac{V_{T1}}{2R_2} \right] \quad (6)$$

Setting $R_1 = 2 \cdot R_2$ to cancel unwanted driver signal in the receive path, then we have

$$V_{OUT} = \frac{R_F}{2R_2} V_{T1} \quad (7)$$

We can also find that,

$$V_{TN} = \frac{1}{2}V_S \quad \text{and} \quad V_{T1} = \frac{1}{N} V_{TN} = \frac{1}{2N} V_S \quad (8)$$

And then

$$V_{OUT} = \frac{R_F}{4NR_2} V_S \quad (9)$$

In conclusion, the peak-to-peak voltage to the ADC would be,

$$2 V_{OUT} = \frac{R_F}{2NR_2} V_S \quad (10)$$

RECEIVE CHANNEL NOISE CALCULATION

The circuit of [Figure 8](#) also has the characteristic that it cancels noise power from the drive channel.

The noise gain of the receive pre-amp is found to be:

$$A_N = 1 + \frac{R_F}{R_1 // R_2} \quad (11)$$

Noise power at each of the output of LMH6622:

$$e_o^2 = A_n^2 [V_n^2 + i_{non-inv}^2 R_+^2 + 4kT R_+] + i_{inv}^2 R_F^2 + 4kT R_F A_n \quad (12)$$

where

V_n	Input referred voltage noise
i_n	Input referred current noise
$i_{non-inv}$	Input referred non-inverting current noise
i_{inv}	Input referred inverting current noise
k	Boltzmann's constant, $K = 1.38 \times 10^{-23}$
T	Resistor temperature in k
R_+	Source resistance at the non-inverting input to balance offset voltage, typically very small for this inverting summing applications

For a voltage feedback amplifier,

$$i_{inv} = i_{non-inv} = i_n \quad (13)$$

Therefore, total output noise from the differential pre-amp is:

$$e_{TotalOutput}^2 = 2 e_o^2 \quad (14)$$

The factor '2' appears here because of differential output.

DIFFERENTIAL ANALOG-TO-DIGITAL DRIVER

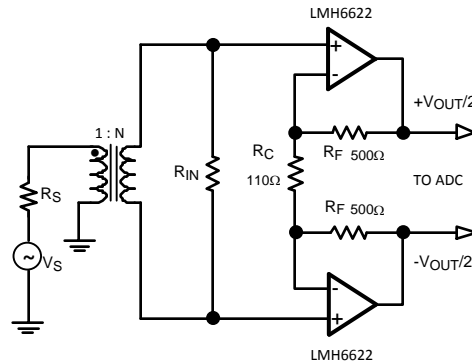


Figure 9. Circuit for Differential A/D Driver

The LMH6622 is a low noise, low distortion high speed operational amplifier. The LMH6622 comes in either SOIC-8 or MSOP-8 packages. Because two channels are available in each package the LMH6622 can be used as a high dynamic range differential amplifier for the purpose of driving a high speed analog-to-digital converter. Driving a 1kΩ load, the differential amplifier of Figure 9 provides 20dB gain, a flat frequency response up to 6MHz, and harmonic distortion that is lower than 80dBc. This circuit makes use of a transformer to convert a single-ended signal to a differential signal. The input resistor R_{IN} is chosen by the following equation,

$$R_{IN} = \frac{1}{N^2} R_S \tag{15}$$

The gain of this differential amplifier can be adjusted by R_C and R_F ,

$$A_V = 2 \frac{R_F}{R_C} \tag{16}$$

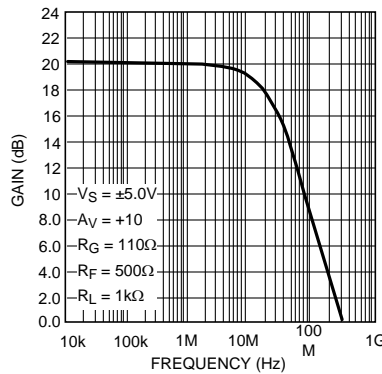


Figure 10. Frequency Response

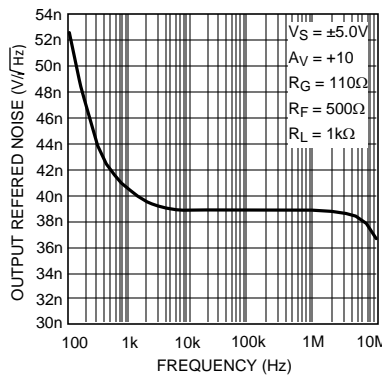


Figure 11. Total Output Referred Noise Density

CIRCUIT LAYOUT CONSIDERATIONS

National Semiconductor suggests the copper patterns on the evaluation boards listed below as a guide for high frequency layout. These boards are also useful as an aid in device testing and characterization. As is the case with all high-speed amplifiers, accepted-practice R_F design technique on the PCB layout is mandatory. Generally, a good high frequency layout exhibits a separation of power supply and ground traces from the inverting input and output pins. Parasitic capacitances between these nodes and ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). High quality chip capacitors with values in the range of 1000pF to 0.1 μ F should be used for power supply bypassing. One terminal of each chip capacitor is connected to the ground plane and the other terminal is connected to a point that is as close as possible to each supply pin as allowed by the manufacturer's design rules. In addition, a tantalum capacitor with a value between 4.7 μ F and 10 μ F should be connected in parallel with the chip capacitor. Signal lines connecting the feedback and gain resistors should be as short as possible to minimize inductance and microstrip line effect. Input and output termination resistors should be placed as close as possible to the input/output pins. Traces greater than 1 inch in length should be impedance matched to the corresponding load termination.

Symmetry between the positive and negative paths in the layout of differential circuitry should be maintained so as to minimize the imbalance of amplitude and phase of the differential signal.

Device	Package	Evaluation Board P/N
LMH6622MA	SOIC-8	CLC730036
LMH6622MM	MSOP-8	CLC730123

These free evaluation boards are shipped when a device sample request is placed with National Semiconductor.

Component value selection is another important parameter in working with high speed/high performance amplifiers. Choosing external resistors that are large in value compared to the value of other critical components will affect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These parasitic capacitors could either be inherent to the device or be a by-product of the board layout and component placement. Moreover, a large resistor will also add more thermal noise to the signal path. Either way, keeping the resistor values low will diminish this interaction. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation and worse distortion.

DRIVING CAPACITIVE LOAD

Capacitive Loads decrease the phase margin of all op amps. The output impedance of a feedback amplifier becomes inductive at high frequencies, creating a resonant circuit when the load is capacitive. This can lead to overshoot, ringing and oscillation. To eliminate oscillation or reduce ringing, an isolation resistor can be placed between the load and the output. In general, the bigger the isolation resistor, the more damped the pulse response becomes. For initial evaluation, a 50 Ω isolation resistor is recommended.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LMH6622MA	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	
LMH6622MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMH6622MAX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	
LMH6622MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMH6622MM	ACTIVE	VSSOP	DGK	8	1000	TBD	CU SNPB	Level-1-260C-UNLIM	
LMH6622MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMH6622MMX	ACTIVE	VSSOP	DGK	8	3500	TBD	CU SNPB	Level-1-260C-UNLIM	
LMH6622MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6622MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6622MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6622MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6622MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6622MMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6622MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

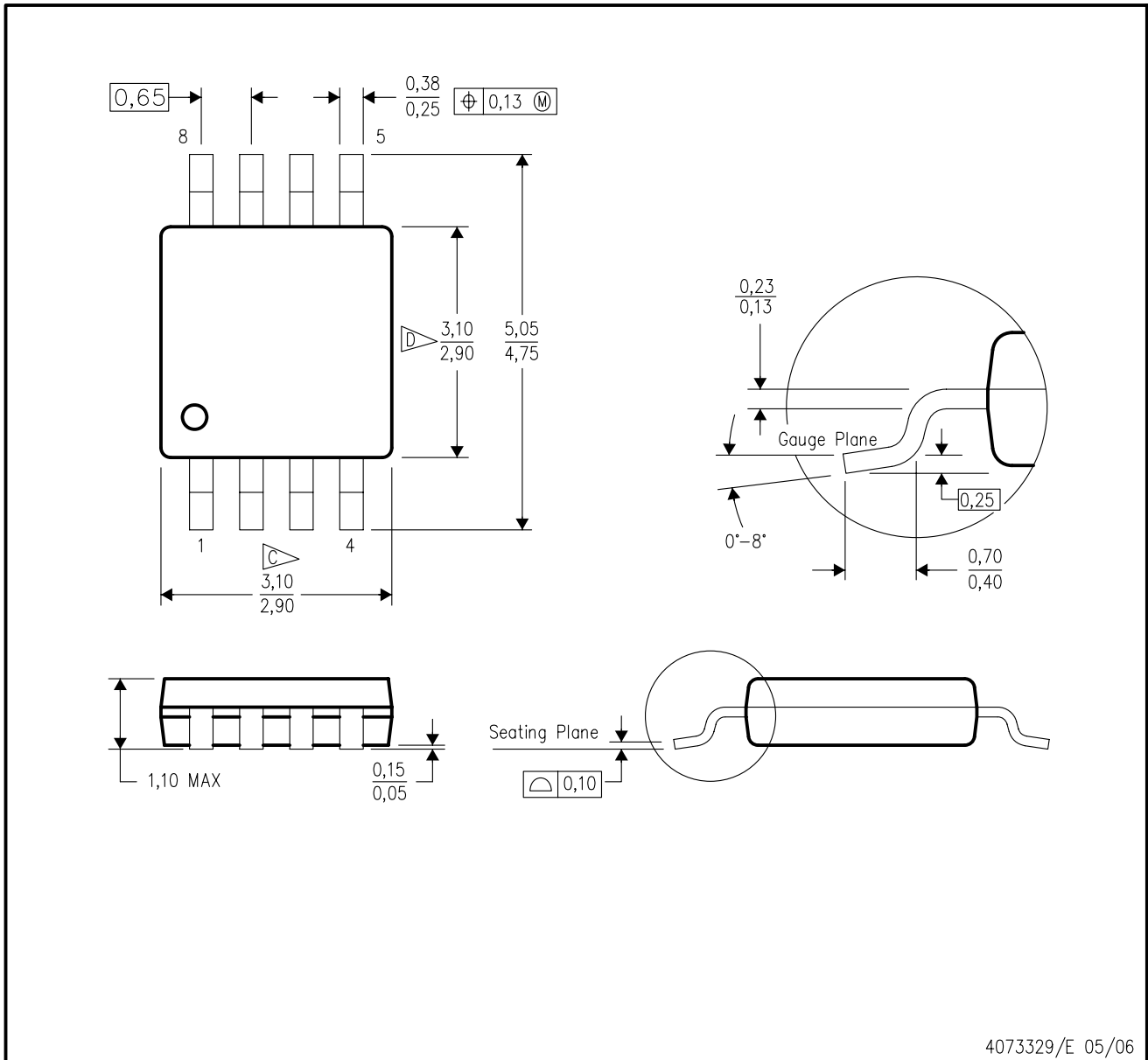
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6622MAX	SOIC	D	8	2500	349.0	337.0	45.0
LMH6622MAX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LMH6622MM	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMH6622MM/NOPB	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMH6622MMX	VSSOP	DGK	8	3500	349.0	337.0	45.0
LMH6622MMX/NOPB	VSSOP	DGK	8	3500	349.0	337.0	45.0

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



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 B. This drawing is subject to change without notice.
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 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 E. Reference JEDEC MS-012 variation AA.

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