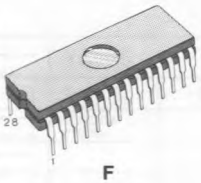
SGS-THOMSON MICROELECTRONICS

M27128A

128K (16K x 8) NMOS UV ERASABLE PROM

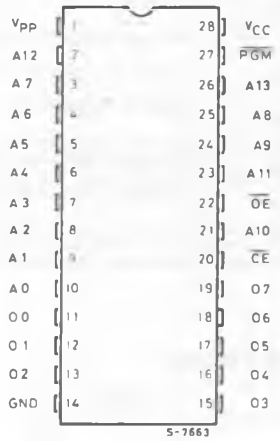
- FAST ACCESS TIME:
  150ns MAX M27128A-1F1
  200ns MAX M27128A-2F1/M27128A-20F1
  250ns MAX M27128AF1/M27128AF6/M27128A-25F1
  300ns MAX M27128A-3F1/M27128A-30F1
  450ns MAX M27128A-4F1/M27128A-4F6/M27128A-45F1
- 0 to +70°C STANDARD TEMPERATURE RANGE
- −40 to +85°C EXTENDED TEMPERATURE RANGE
- SINGLE +5V POWER SUPPLY
- ±10% V_{CC} TOLERANCE AVAILABLE
- LOW STANDBY CURRENT (40mA MAX)
- TTL COMPATIBLE DURING READ AND PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE



F
DIP-28
(Ceramic Bull's Eye)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS



DESCRIPTION

The M27128A is a 131,072-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 16,384 words by 8 bits and manufactured using SGS-THOMSON' NMOS-E3 process.

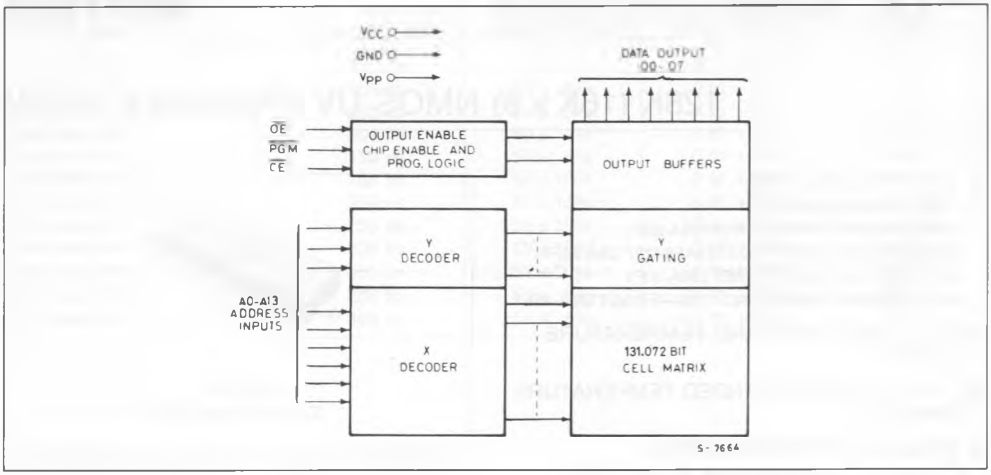
The M27128A with its single +5V power supply and with an access time of 200ns, is ideal for use with high performance +5V microprocessor such as Z8, Z80 and Z8000. The M27128A has an important feature which is to separate the output control, Ouptut Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems.

The M27128A also features a standby mode which reduces the power dissipation without increasing access time. The active current is 85mA while the maximum standby current is only 40 mA, a 53% saving. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input. The M27128A has an "Electronic Signature" that allows programmers to automatically identify device type and pinout. The M27128A is available in a 28-lead dual in-line ceramic package (frit-seal) glass lens.

PIN NAMES

A0-A13	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
$\overline{PGM}$	PROGRAM
O0-O7	DATA INPUT/OUTPUT

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Values	Unit
V_I	All Input or Output voltages with respect to ground	+6.25 to −0.6	V
V_{PP}	Supply voltage with respect to ground	+14 to −0,6	V
T_{amb}	Ambient temperature under bias /F1 /F6	−10 to +80 − 50 to +95	°C °C
T_{stg}	Storage temperature range	− 65 to +125	°C
	Voltage on pin 24 with respect to ground	+13.5 to −0.6	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
READ	V_{IL}	V_{IL}	X	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	V_{IH}	V_{CC}	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	HIGH Z
FAST PROGRAMMING	V_{IL}	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
VERIFY	V_{IL}	V_{IL}	X	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	X	X	X	V_{PP}	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE	V_{IL}	V_{IL}	V_H	V_{IH}	V_{CC}	V_{CC}	CODES

NOTE: X can be V_{IH} or V_{IL} V_H = 12V ±0.5V

READ OPERATION

DC AND AC CONDITIONS

Selection Code	F1/ – 1F1/ – 2F1/ – 3F1/ – 4F1	– 20F1/ – 25F1/ – 30F1/ – 45F1	F6/ – 4F6
Operating Temperature Range	0 to 70°C	0 to 70°C	– 40 to 85°C
V_{CC} Power Supply (1,2)	5V ±5%	5V ±10%	5V ±5%
V_{PP} Voltage (2)	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ. (3)	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	µA
I_{PP1}(2)	V_{PP} Current Read Standby	$V_{PP} = 5.5V$			5	mA
I_{CC1}(2)	V_{CC} Current Standby	$\overline{CE} = V_{IH}$			40	mA
I_{CC2}(2)	V_{CC} Current Active	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{PP} = V_{CC}$			85	mA
V_{IL}	Input Low Voltage		– 0.1		+ 0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA	2.4			V
V_{PP}(2)	V_{PP} Read Voltage	$V_{CC} = 5V \pm 0.25V$	3.8		V_{CC}	V

AC CHARACTERISTICS

Symbol	Parameter	V_{CC} ± 5% V_{CC} ± 10%	27128A-1		27128A-2 27128A-20		27128A 27128A-25		27128A-3 27128A-30		27128A-4 27128A-45		Unit
		Test Conditions	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200		250		300		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200		250		300		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		65		75		100		120		150	ns
t_{DF}(4)	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$		55	0	55	0	60	0	105	0	130	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		0		ns

CAPACITANCE(5) ($T_{amb} = 25°C$, f = 1 MHz)

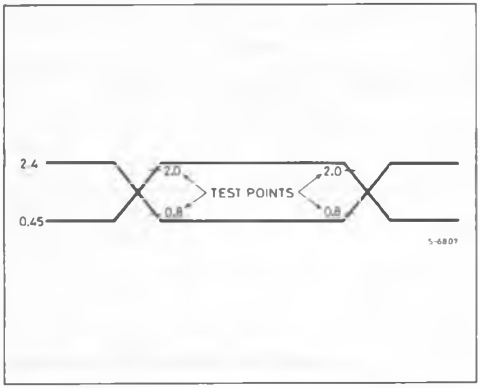
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven. (See timing diagram).
5. This parameter is only sampled and is not 100% tested.

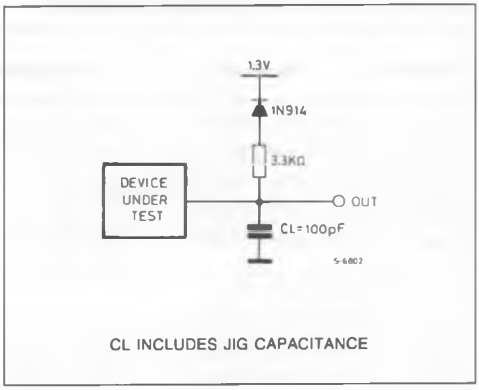
READ OPERATION (Continued)

AC TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: ≤20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs 0.8 and 2V
Outputs 0.8 and 2V

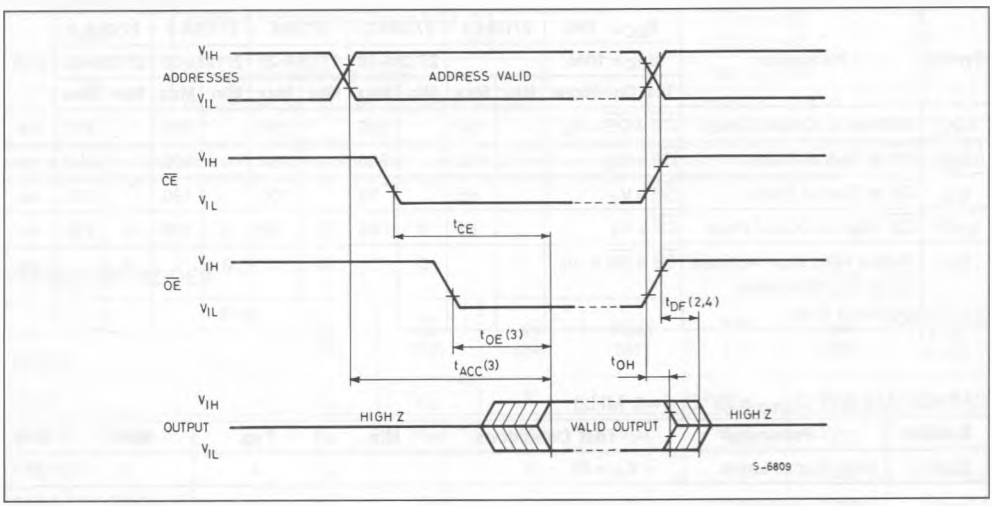
AC TESTING INPUT/OUTPUT WAVEFORM



AC TESTING LOAD CIRCUIT



AC WAVEFORMS



Notes:
1. Typical values are for T_{amb} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The seven modes of operations of the M27128A are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

READ MODE

The M27128A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that addresses are stable, address access time (t_{ACC}) is equal to delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27128A has a standby mode which reduces the maximum active power current from 85 mA to 40 mA. The M27128A is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a) the lowest possible memory power dissipation
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors.

It is recommended that a 1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution: exceeding 13V on pin 1 (V_{PP}) will damage the M27128A.

When delivered, and after each erasure, all bits of the M27128A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M27128A is in the programming mode when V_{PP} input is at 12.5V and $\overline{CE}$ and $\overline{PGM}$ are at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs M27128A EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each bytes is continually monitored to determine when it has been successfully programmed. A flowchart of the M27128A Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types: initial and over-program.

The duration of the initial $\overline{PGM}$ pulse (s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3Xmsec. (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M27128A location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied.

DEVICE OPERATION (Continued)

The entire sequence of program pulses and byte verifications is performed at $V_{CC} = 6V$ and $V_{PP} = 12.5V$. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5V$.

PROGRAM INHIBIT

Programming of multiple M27128As in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel M27128A may be common. A TTL low pulse applied to a M27128A's $\overline{CE}$ input, with V_{PP} at 12.5V, will program that M27128A. A high level $\overline{CE}$ input inhibits the other M27128A from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} at 12.5V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the M27128A. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the M27128A. Two identifier bytes may than be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the SGS-THOMSON M27128A, these two identifier bytes are given below. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (07) defined as the parity bit.

ERASURE OPERATION

The erasure characteristic of the M27128A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000–4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27128A in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the M27128A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27128A window to prevent unintentional erasure. The recommended erasure procedure for the M27128A is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27128A should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

PINS / IDENTIFIER	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	1	0	0	0	1	0	0	1	89

PROGRAMMING OPERATION (T_{amb} = 25°C ±5°C, V_{CC}(1) = 6V ±0.25V, V_{PP}(1) = 12.5V ±0.3V)

DC AND OPERATING CHARACTERISTIC

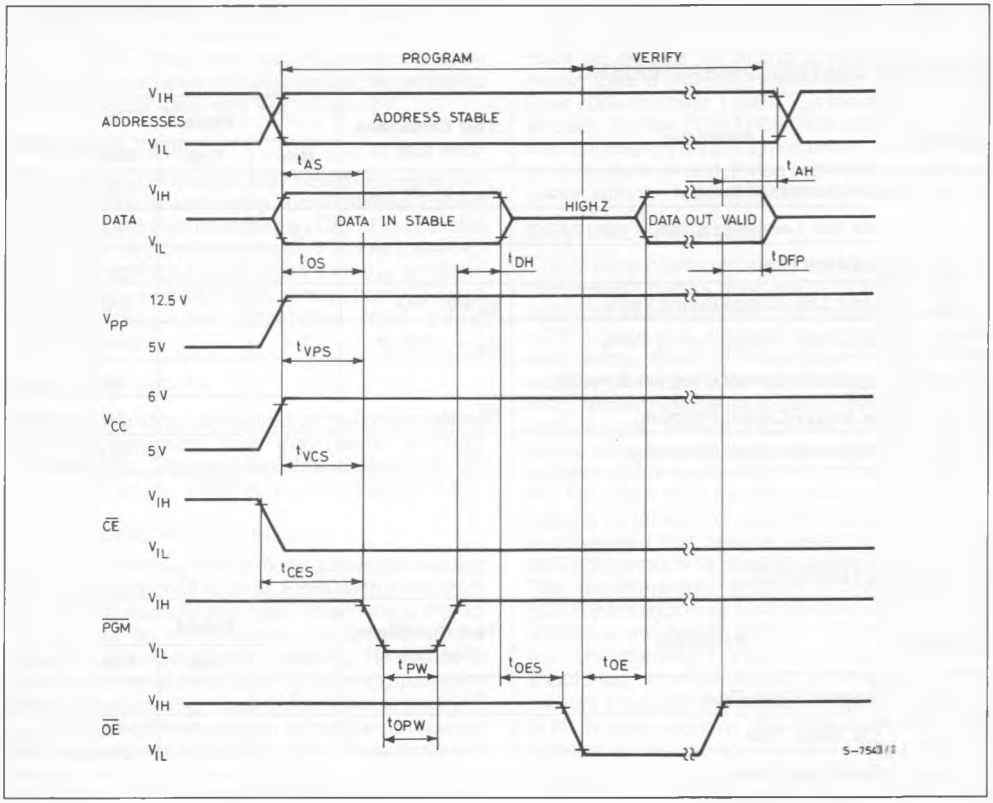
Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	µA
V_{IL}	Input Low Level (All Inputs)		−0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = −400 µA	2.4			V
I_{CC2}	V_{CC} Supply Current (Program & Verify)				100	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DFP}(4)	Output Enable Output Float Delay		0		130	ns
t_{VPS}	V_{PP} Setup Time		2			µs
t_{VCS}	V_{CC} Setup Time		2			µs
t_{CES}	$\overline{CE}$ Setup Time		2			µs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	(see Note 3)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	(see Note 2)	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$				150	ns

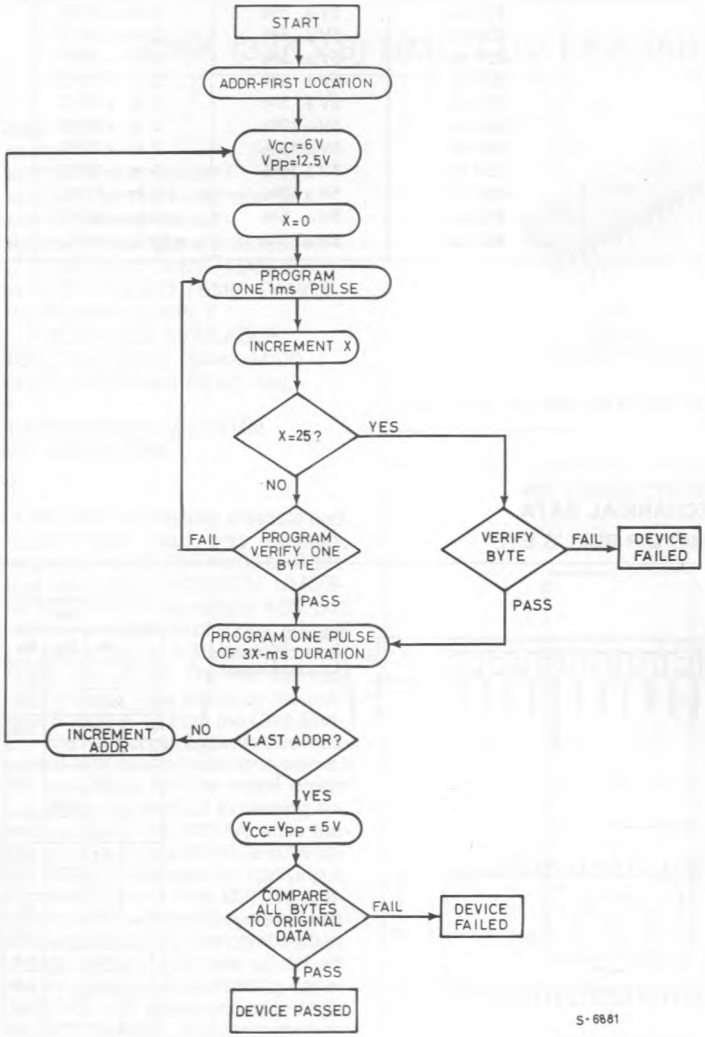
Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1msec ±5%.
4. This parameter is only sampled and not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING WAVEFORMS



Notes:
1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27128A a 0.1μF capacitor is required across V_{PP} and GROUND to suppress spurious voltage transients which can damage the device.

FAST PROGRAMMING FLOWCHART

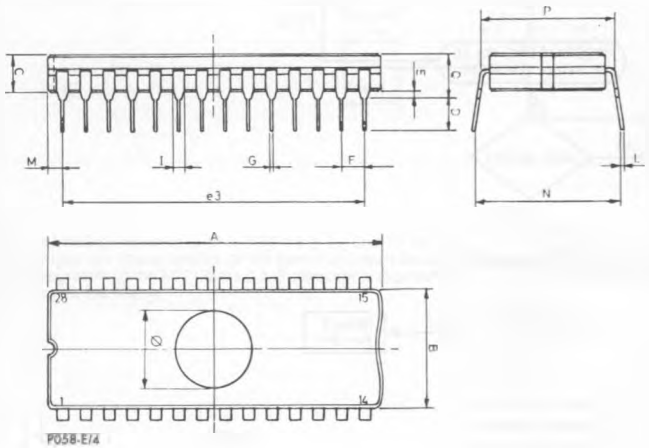


ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27128A-1F1	150 ns	5V ± 5%	0 to +70°C	DIP-28
M27128A-2F1	200 ns	5V ± 5%	0 to +70°C	DIP-28
M27128AF1	250 ns	5V ± 5%	0 to +70°C	DIP-28
M27128A-3F1	300 ns	5V ± 5%	0 to +70°C	DIP-28
M27128A-4F1	450 ns	5V ± 5%	0 to +70°C	DIP-28
M27128A-20F1	200 ns	5V ± 10%	0 to +70°C	DIP-28
M27128A-25F1	250 ns	5V ± 10%	0 to +70°C	DIP-28
M27128A-30F1	300 ns	5V ± 10%	0 to +70°C	DIP-28
M27128A-45F1	450 ns	5V ± 10%	0 to +70°C	DIP-28
M27128AF6	250 ns	5V ± 5%	−40 to +85°C	DIP-28
M27128A-4F6	450 ns	5V ± 5%	−40 to +85°C	DIP-28

PACKAGE MECHANICAL DATA

28-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.200
D	3.00			0.118		
E	0.50		1.78	0.020		0.070
e3		33.02			13.00	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	16.51		18.00	0.650		0.709
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	6.86		7.36	0.270		0.290