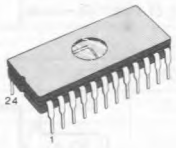
SGS-THOMSON MICROELECTRONICS

ET2716
M2716

16K (2K x 8) NMOS UV ERASABLE PROM

- 2048 x 8 ORGANIZATION
- 525 MW MAX ACTIVE POWER, 132 MW MAX STANDBY POWER
- LOW POWER DURING PROGRAMMING
- ACCESS TIME M/ET2716-1, 350ns; M/ET2716, 450ns
- SINGLE 5V POWER SUPPLY
- STATIC-NO CLOCKS REQUIRED
- INPUTS AND OUTPUTS TTL COMPATIBLE DURING BOTH READ AND PROGRAM MODES
- THREE-STATE OUTPUT WITH OR-TIE CAPABILITY
- EXTENDED TEMPERATURE RANGE (F6)



Q/F
DIP-24
(Ceramic Bull's Eye)

(Ordering Information at the end of the datasheet)

DESCRIPTION

The M/ET2716 is high speed 16K UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn around and pattern experimentation are important requirements.

The M/ET2716 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

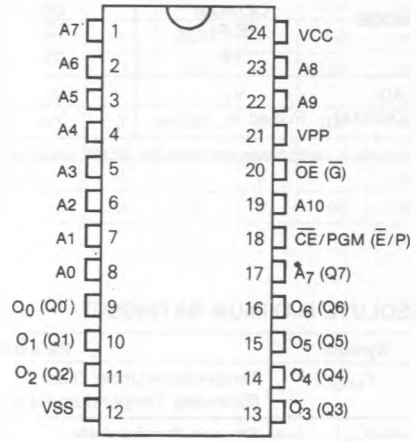
This EPROM is fabricated with the reliable, high volume, time proven, N-channel silicon gate technology X-MOS.

PIN NAMES

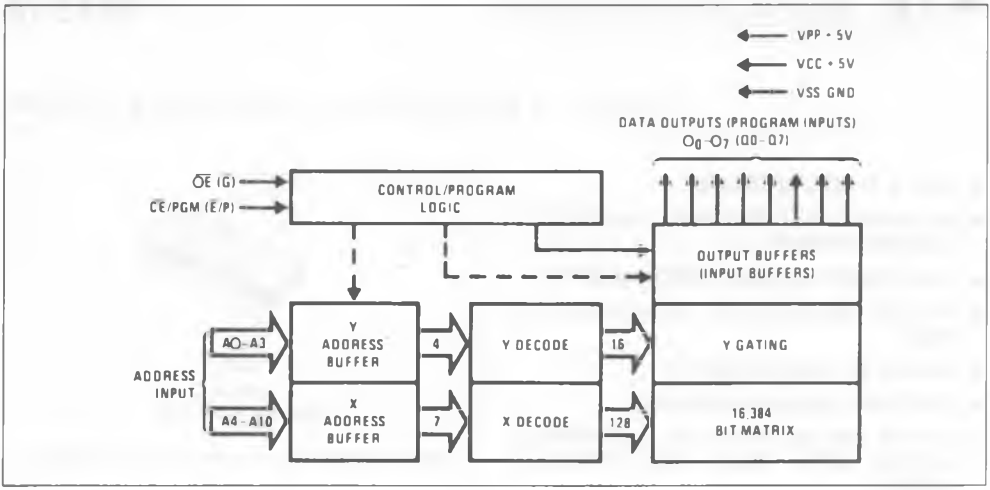
A0—A10	ADDRESS INPUTS
O_0—O_7 (Q0—Q7)	DATA OUTPUTS
$\overline{CE}$/PGM ($\overline{E}$/P)	CHIP ENABLE/PROGRAM
$\overline{OE}$ ($\overline{G}$)	OUTPUT ENABLE
V_{PP}	READ 5V, PROGRAM 25V
V_{CC}	POWER (5V)
V_{SS}	GROUND

Note: Symbols in parentheses are proposed JEDEC standard

PIN CONNECTIONS



BLOCK DIAGRAM



PIN CONNECTION DURING READ OR PROGRAM

MODE	PIN NAME/NUMBER				
	$\overline{CE}/PGM$ ($\overline{E}/P$) 18	$\overline{OE}$ ($\overline{G}$) 20	V_{PP} 21	V_{CC} 24	OUTPUTS 9—11, 13-17
READ	V_{IL}	V_{IL}	5	5	D_{OUT}
PROGRAM	Pulsed V_{IL} to V_{IH}	V_{IH}	25	5	D_{IN}

* Symbols in parentheses are proposed JEDEC standard.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
T_{amb}	Temperature Under Bias (Extended Temperature Range)	−10 to +80 (−50 to +95)	°C °C
T_{stg}	Storage Temperature	−65 to +125	°C
V_{PP}	V_{PP} Supply Voltage with Respect to V_{SS}	26.5V to −0.3	V
V_{in}	All Input or Output Voltages with Respect to V_{SS}	6V to −0.3	V
P_D	Power Dissipation	1.5	W
	Lead Temperature (Soldering 10 seconds)	+300	°C

Note 1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are, not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

READ OPERATION

DC CHARACTERISTICS[1] $T_A = 0°C$ to $+ 70°C$[6], $V_{CC} = 5V \pm 5\%$ for M/ET2716, $V_{CC} = 5V \pm 10\%$ for M/ET2716-1 $V_{PP} = V_{CC}$[3], $V_{SS} = 0V$, (Unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current	$V_{IN} = 5.25V$ ORVIN $= V_{IL}$	—	—	10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.25V$, $\overline{CE}/PGM = 5V$	—	—	10	μA
I_{PP1}	V_{PP} Supply Current	$V_{PP} = 5.25V$	—	—	5	mA
I_{CC1}	V_{CC} Supply Current (Standby)	$\overline{CE}/PGM = V_{IH}$, $\overline{OE} = V_{IL}$	—	10	25	mA
I_{CC2}	V_{CC} Supply Current (Active)	$\overline{CE}/PGM = \overline{OE} = V_{IL}$	—	57	100	mA
V_{IL}	Input Low Voltage		−0.1	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ μA	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA	—	—	0.45	V

AC CHARACTERISTICS $T_A = 0°C$ to $+70°C$ C[6], $V_{CC} = 5V \pm 5\%$ for M/ET2716, $V_{CC} = 5V \pm 10\%$ for M/ET2716-1 $V_{PP} = V_{CC}$[3], $V_{SS} = 0V$, (Unless otherwise specified).

Symbol		Parameter	Test Conditions	M/ET2716-1		M/ET2716		Unit
Standard	Jedec			Min.	Max.	Min.	Max.	
t_{ACC}	TAVQV	Address to Output Delay	$\overline{CE}/PGM = \overline{OE} = V_{IL}$	—	350	—	450	ns
t_{CE}	TELQV	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$	—	350	—	450	ns
t_{OE}	TGLQV	Output Enable to Output Delay	$\overline{CE}/PGM = V_{IL}$	—	120	—	120	ns
t_{DF} (Note 5)	TGHQZ	$\overline{OE}$ or $\overline{CE}$ High to Output Hi-Z	$\overline{CE}/PGM = V_{IL}$	0	100	0	100	ns
t_{OH}	TAXQX	Address to Output Hold	$\overline{CE}/PGM = \overline{OE} = V_{IL}$	0	—	0	—	ns
t_{OD}	TEHQZ	$\overline{CE}$ to Output Hi-Z	$\overline{OE} = V_{IL}$	0	100	0	100	ns

CAPACITANCE [4] $T_A = 25°C$, $f = 1$ MHz

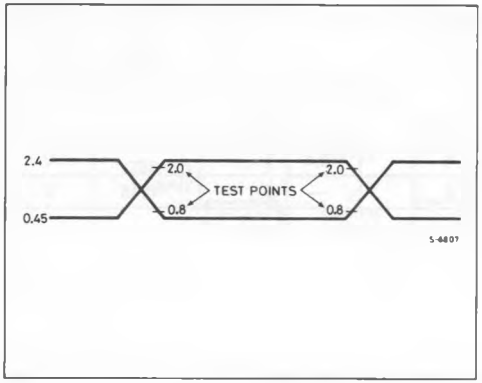
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes 1. VCC must be applied at the same time or before VPP and removed after or at the same time as VPP
2. Typical conditions are for operation at: T_A = 25°C, VCC = 5V, VPP = VCC, and VSS = OV
3. VPP may be connected to VCC except during program
4. Capacitance is guaranteed by periodic testing. T_A = 25°C, f = 1 MHz.
5. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ wich ever occurs first. This parameter as only sampled and not 100% tested.
6. T_A = − 40°C To + 85°C for the F6 version (extended To range)

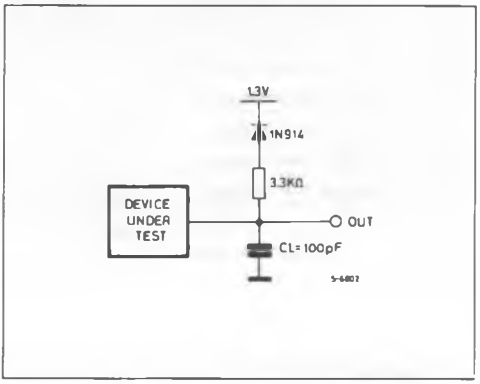
AC TEST CONDITIONS

Output Load: 1 TTL gate and CL = 100 pF
Input Rise and Fall Times ≤ 20 ns
Input pulse levels: 0.45V to 2.4V
Timing Measurement Reference Level
Inputs, Outputs 0.8V and 2V

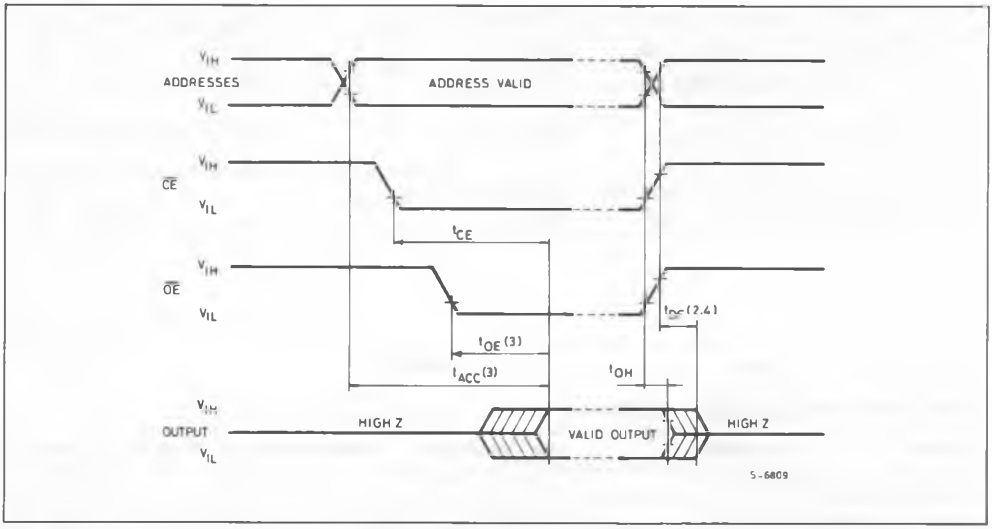
AC TESTING INPUT/OUTPUT WAVEFORM



AC TESTING LOAD CIRCUIT



AC WAVEFORMS



Notes:
1. Typical values are for T_{amb} = 25°C and nominal supply voltage
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{ACC}
4. t_{DF} is specified form $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The M/ET2716 has 3 modes of operation in the normal system environment. These are shown in Table 1.

READ MODE

The M/ET2716 read operation requires that $\overline{OE}$ = VIL, $\overline{CE}$/PCM = VIL and that addresses A0 – A10 have been stabilized. Valid data will appear on the output pins after t_{ACC}, t_{OE} or t_{CE} times (see Swithching Time Waveforms) depending on wich is limiting.

DESELECT MODE

The M/ET2716 is deselected by making $\overline{OE}$ = VIH. This mode is independent of $\overline{CE}$/PGM and the condition of the adresses. The outputs are Hi-Z when $\overline{OE}$ = VIH. This allows OR-tying 2 or more M/ET2716's for memory expansion.

STANDBY MODE (Power Down)

The M/ET2716 may be powered down to the standby mode by making $\overline{CE}$/PGM = VIH. This is independent of $\overline{OE}$ and automatically puts the outputs in their Hi-Z state. The power is reduced to 25% (132 mW max) of the normal operating power. VCC and VPP must be maintened at 5V. Access time at power up remains either t_{ACC} or t_{CE} (see Switching Time Waveforms).

PROGRAMMING

The M/ET2716 is shipped from SGS-THOMSON-completely erased. All bits will be at "1" level (output high) in this initial state and after any full erasure. Table II shows the 3 programming modes.

PROGRAM MODE

The M/ET2716 is programmed by introducing "0" s into the desidered locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the chip enable pin. All input voltage levels including the program pulse on chip enable are TTL compatible. The programming sequence is:

TABLE I. OPERATING MODES ($V_{CC} = V_{PP} = 5V$)

MODE	PIN NAME/NUMBER		
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	OUTPUTS 9—11, 13-17
READ	V_{IL}	V_{IL}	D_{OUT}
DESELECT	Don't Care	V_{IH}	Hi-Z
STANDBY	V_{IH}	Don't Care	Hi-Z

With V_{PP} = 25V, VCC = 5V, $\overline{OE}$ = V_{IH} and $\overline{CE}$/PGM = V_{IL}, an address is selected and the desired data word is applied to the output pins. (V_{IL} = "0" and V_{IL} = "1" for both address and data). After the address and data signals are stable the program pin is pulsed from V_{IL} to V_{IH} with a pulse width between 45 ms and 55 ms. Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (V_{IH} or higher) must not be maintained longer than $t_{PW(MAX)}$ on the program pin during programming. M/ET2716's may be programmed in parallel with the same data in this mode.

PROGRAM VERIFY MODE

The programming of the M/ET2716 may be verified either 1 word at a time during the programming (as shown in the timing diagram) or by reading all of the words out at the end of the programming sequence. This can be done with V_{PP} = 25V (or 5V) in either case. V_{PP} must be at 5V for all operating modes and can be maintained at 25V for all programming modes.

PROGRAM INHIBIT MODE

The program inhibit mode allows programming several M/ET2716's simultaneously with different data for each one by controlling wich ones receive the program pulse. All similar inputs of the M/ET2716 may be paralleled. Pulsing the program pin (from V_{IL} to V_{IH}) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{OE}$ = V_{IH} will put its outputs in the Hi-Z state.

TABLE II. PROGRAMMING MODES ($V_{CC} = 5V$)

MODE	PIN NAME/NUMBER			
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	V_{PP} 21	OUTPUTS 9—11, 13-17
PROGRAM	Pulsed V_{IL} to V_{IH}	V_{IH}	25	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	25(5)	D_{OUT}
PROGRAM INHIBIT	V_{IL}	V_{IH}	25	Hi-Z

ERASING

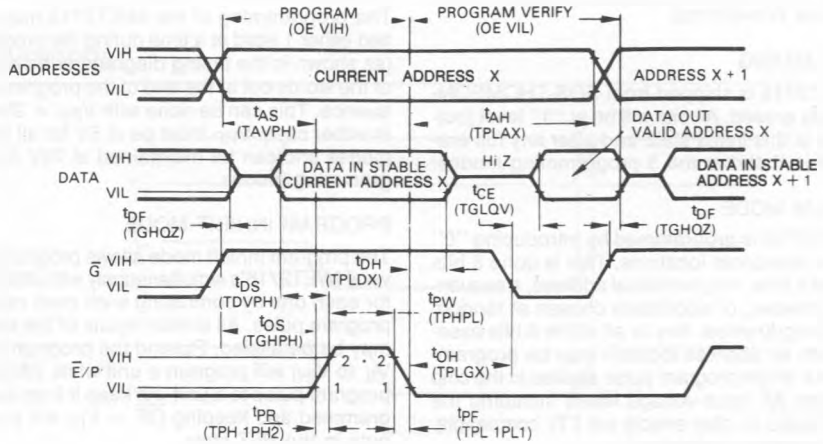
The M/ET2716 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the M/ET2716 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time.

An ultraviolet source of 2537 A yelding a total integrated dosage of 15 watt-seconds/cm² power rating is used. The M/ET2716 to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occuring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

TIMING DIAGRAM

PROGRAM MODE



Note: Symbols in parentheses are proposed JEDEC standard

PROGRAMMING OPERATION

DC AND OPERATING CHARACTERISTICS ($T_A = 25°C \pm 5°C$) ($V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$) Notes 1 and 2

Symbol	Parameter	Min.	Max.	Units
I_{LI}	Input Leakage Current (Note 3)	—	10	μA
V_{IL}	Input Low Level	−0.1	0.8	V
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V
I_{CC}	V_{CC} Power Supply Current	–	100	mA
I_{PP1}	V_{PP} Supply Current	—	5	mA
I_{PP2}	V_{PP} Supply Current During Programming Pulse (Note 5)	—	30	mA

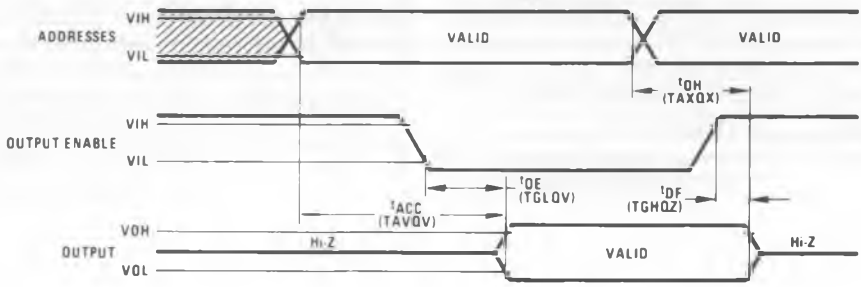
AC CHARACTERISTICS ($T_A = 25°C \pm 5°C$) ($V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$) Notes 1, 2 and 6

Symbol		Parameter	Min.	Typ.	Max.	Units
Standard	Jedec					
t_{AS}	TAVPH	Address Setup Time	2	—	—	μs
t_{OS}	TGHPH	$\overline{OE}$ Setup Time	2	—	—	μs
t_{DS}	TDVPH	Data Setup Time	2	—	—	μs
t_{AH}	TPLAX	Address Hold Time	2			μs
t_{OH}	TPLGX	$\overline{OE}$ Hold Time	2	—	—	μs
t_{DH}	TPLDX	Data Hold Time	2	—	—	μs
t_{DF}	TGHQZ	Chip Disable to Output Float Delay (Note 4)	0	—	100	ns
t_{OE}	TGLQV	Output Enable to Output Delay (Note 4)	—	—	120	ns
t_{PW}	TPHPL	Program Pulse Width	45	50	55	ms
t_{PR}	TPH1PH2	Program Pulse Rise Time	5	—	—	ns
t_{PF}	TPL2PL1	Program Pulse Fall Time	5	—	—	ns

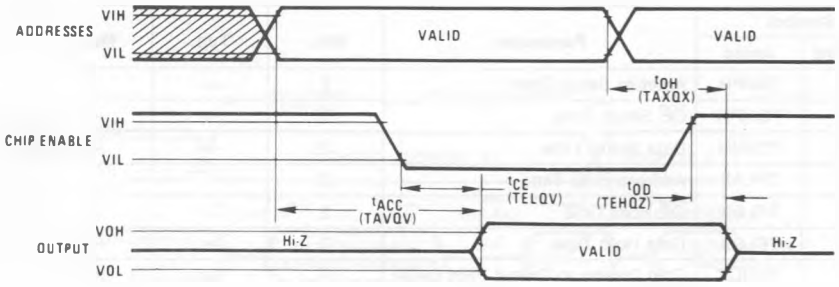
Notes 1. VCC must be applied at the same time of before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be insereted into a board with power applied.
2. Care must be taken to prevent overshoot of the VPP supply when switching + 25V
3. $0.45V \leq VIN < 5.25V$
4. CE/PGM = VIL, VPP = VCC
5. VPP = 26 V
6. Transition times ≤ 20 ns unless otherwise noted

SWITCHING TIME WAVEFORMS

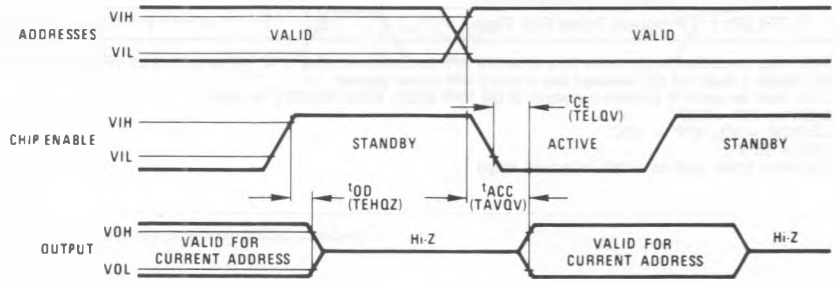
Read Cycle ($\overline{CE}$/PGM = VIL)



Read Cycle ($\overline{OE}$ = VIL)



Standby Power Down Mode ($\overline{OE}$ = VIL)



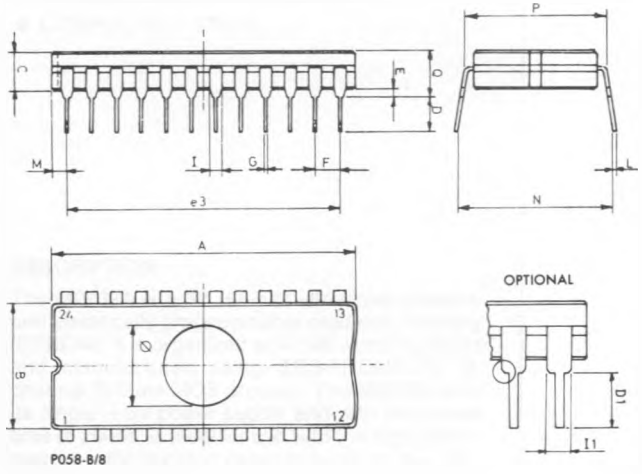
Symbols in parentheses are proposed JEDEC standard

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
ET2716Q	450 ns	5V ± 5%	0 to +70°C	DIP-24
ET2716-Q1	350 ns	5V ± 10%	0 to +70°C	DIP-24
M2716F1	450 ns	5V ± 5%	0 to +70°C	DIP-24
M2716-1F1	350 ns	5V ± 10%	0 to +70°C	DIP-24
M2716F6	450 ns	5V ± 5%	−40 to +85°C	DIP-24
M2716-1F6	350 ns	5V ± 10%	−40 to +85°C	DIP-24

PACKAGE MECHANICAL DATA

24-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			32.30			1.272
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.200
D	3.00			0.118		
D1(1)	3.40			0.134		
E	0.50		1.78	0.020		0.070
e 3		27.94			1.100	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
I1(1)	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	16.51		18.00	0.650		0.709
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	6.86		7.36	0.270		0.290

Note: 1. Optional see drawing