# M27C800

## 8 Mbit (1Mb x8 or 512Kb x16) UV EPROM and OTP EPROM

- 5V ± 10% SUPPLY VOLTAGE in READ OPERATION
- ACCESS TIME: 50ns
- BYTE-WIDE or WORD-WIDE CONFIGURABLE
- 8 Mbit MASK ROM REPLACEMENT
- LOW POWER CONSUMPTION
  - Active Current 70mA at 8MHz
  - Stand-by Current 50µA
- PROGRAMMING VOLTAGE: 12.5V ± 0.25V
- PROGRAMMING TIME: 50µs/word
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Device Code: B2h

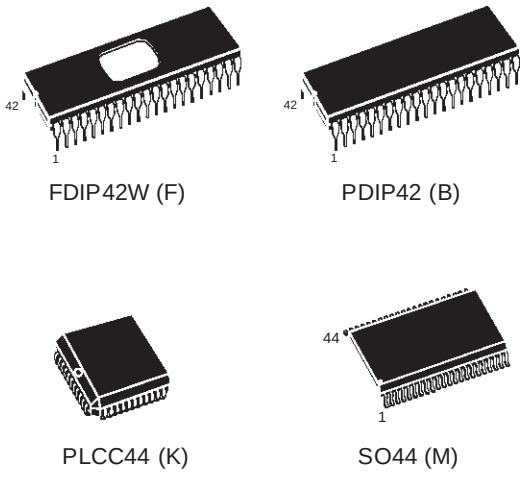
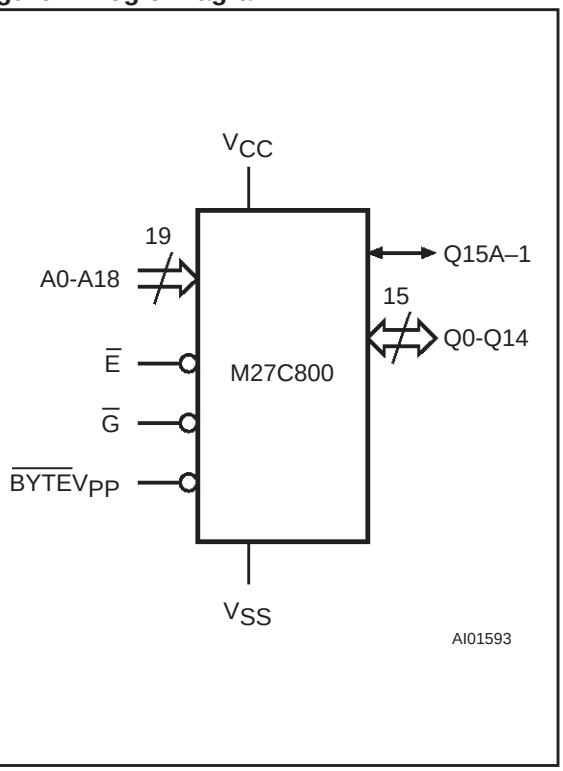



**Figure 1. Logic Diagram**




### DESCRIPTION

The M27C800 is an 8 Mbit EPROM offered in the two ranges UV (ultra violet erase) and OTP (one time programmable). It is ideally suited for microprocessor systems requiring large data or program storage. It is organised as either 1 Mwords of 8 bit or 512 Kwords of 16 bit. The pin-out is compatible with the most common 8 Mbit Mask ROM.

The FDIP42W (window ceramic frit-seal package) has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern.

A new pattern can then be written rapidly to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C800 is offered in PDIP42, PLCC44 and SO44 packages.

**Figure 2A. DIP Connections**

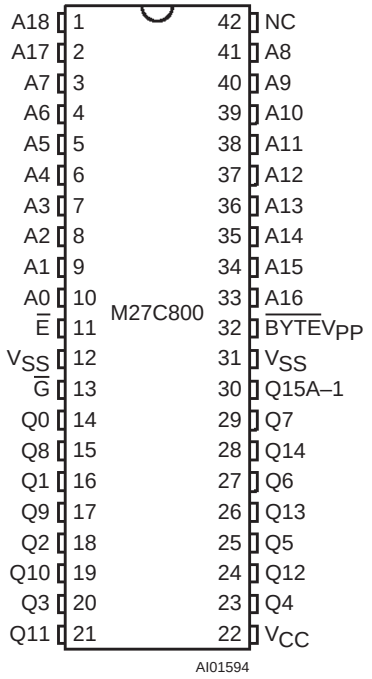



**Figure 2B. LCC Connections**

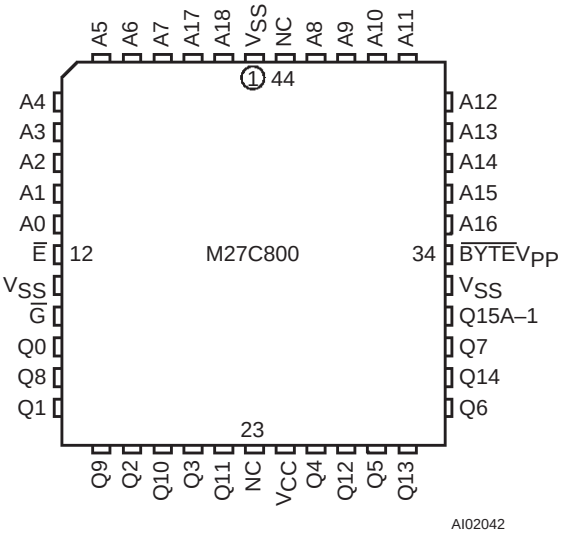



**Figure 2C. SO Connections**

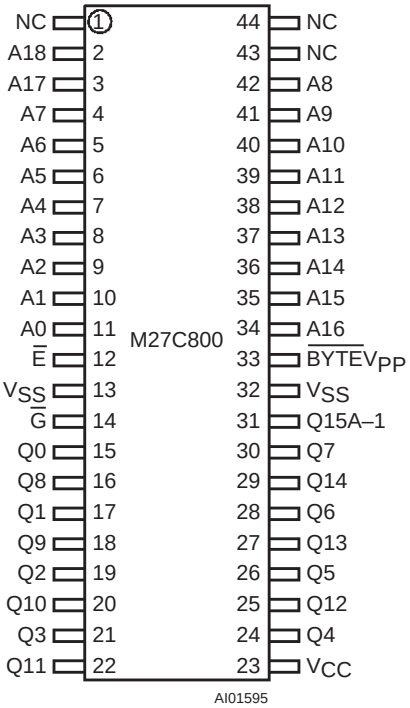



**Table 1. Signal Names**

| | |
|---|---|
| A0-A18 | Address Inputs |
| Q0-Q7 | Data Outputs |
| Q8-Q14 | Data Outputs |
| Q15A–1 | Data Output / Address Input |
| $\overline{E}$ | Chip Enable |
| $\overline{G}$ | Output Enable |
| $\overline{BYTE}V_{PP}$ | Byte Mode / Program Supply |
| $V_{CC}$ | Supply Voltage |
| $V_{SS}$ | Ground |
| NC | Not Connected Internally |

**Table 2. Absolute Maximum Ratings (1)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient Operating Temperature (3) | –40 to 125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –50 to 125 | °C |
| $T_{STG}$ | Storage Temperature | –65 to 150 | °C |
| $V_{IO}$ (2) | Input or Output Voltage (except A9) | –2 to 7 | V |
| $V_{CC}$ | Supply Voltage | –2 to 7 | V |
| $V_{A9}$ (2) | A9 Voltage | –2 to 13.5 | V |
| $V_{PP}$ | Program Supply Voltage | –2 to 14 | V |

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is $V_{CC}$ +0.5V with possible overshoot to $V_{CC}$ +2V for a period less than 20ns.
3. Depends on range.

**Table 3. Operating Modes**

| Mode | $\overline{E}$ | $\overline{G}$ | $\overline{BYTE}V_{PP}$ | A9 | Q15A–1 | Q14-Q8 | Q7-Q0 |
|---|---|---|---|---|---|---|---|
| Read Word-wide | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | Data Out | Data Out | Data Out |
| Read Byte-wide Upper | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | X | $V_{IH}$ | Hi-Z | Data Out |
| Read Byte-wide Lower | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | X | $V_{IL}$ | Hi-Z | Data Out |
| Output Disable | $V_{IL}$ | $V_{IH}$ | X | X | Hi-Z | Hi-Z | Hi-Z |
| Program | $V_{IL}$ Pulse | $V_{IH}$ | $V_{PP}$ | X | Data In | Data In | Data In |
| Verify | $V_{IH}$ | $V_{IL}$ | $V_{PP}$ | X | Data Out | Data Out | Data Out |
| Program Inhibit | $V_{IH}$ | $V_{IH}$ | $V_{PP}$ | X | Hi-Z | Hi-Z | Hi-Z |
| Standby | $V_{IH}$ | X | X | X | Hi-Z | Hi-Z | Hi-Z |
| Electronic Signature | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{ID}$ | Code | Codes | Codes |

Note: X = $V_{IH}$ or $V_{IL}$, $V_{ID}$ = 12V ± 0.5V.

**Table 4. Electronic Signature**

| Identifier | A0 | Q15 and Q7 | Q14 and Q6 | Q13 and Q5 | Q12 and Q4 | Q11 and Q3 | Q10 and Q2 | Q9 and Q1 | Q8 and Q0 | Hex Data |
|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer's Code | $V_{IL}$ | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20h |
| Device Code | $V_{IH}$ | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | B2h |

**Table 5. AC Measurement Conditions**

| | High Speed | Standard |
|---|---|---|
| Input Rise and Fall Times | ≤ 10ns | ≤ 20ns |
| Input Pulse Voltages | 0 to 3V | 0.4V to 2.4V |
| Input and Output Timing Ref. Voltages | 1.5V | 0.8V and 2V |

**Figure 3. AC Testing Input Output Waveform**

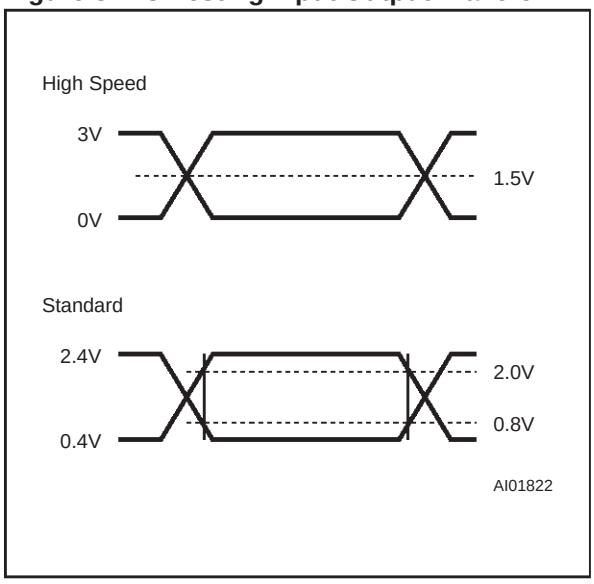
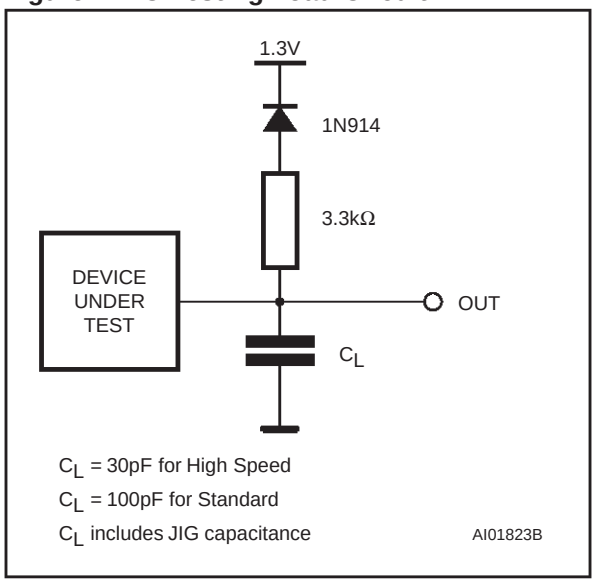



**Figure 4. AC Testing Load Circuit**




## DEVICE OPERATION

The operating modes of the M27C800 are listed in the Operating Modes Table. A single power supply is required in the read mode. All inputs are TTL compatible except for $V_{PP}$ and 12V on A9 for the Electronic Signature.

### Read Mode

The M27C800 has two organisations, Word-wide and Byte-wide. The organisation is selected by the signal level on the $\overline{BYTE}V_{PP}$ pin. When $\overline{BYTE}V_{PP}$ is at $V_{IH}$ the Word-wide organisation is selected and the Q15A–1 pin is used for Q15 Data Output. When the $\overline{BYTE}V_{PP}$ pin is at $V_{IL}$ the Byte-wide organisation is selected and the Q15A–1 pin is used for the Address Input A–1. When the memory is logically regarded as 16 bit wide, but read in the Byte-wide organisation, then with A–1 at $V_{IL}$ the lower 8 bits of the 16 bit data are selected and with A–1 at $V_{IH}$ the upper 8 bits of the 16 bit data are selected.

The M27C800 has two control functions, both of which must be logically active in order to obtain data at the outputs. In addition the Word-wide or Byte- wide organisation must be selected.

Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins independent of device selection. Assuming that the addresses are stable, the address access time ($t_{AVQV}$) is equal to the delay from $\overline{E}$ to output ($t_{ELQV}$). Data is available at the output after a delay of $t_{GLQV}$ from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least $t_{AVQV}$-$t_{GLQV}$.

**Table 6. Capacitance** (1) ($T_A$ = 25 °C, f = 1 MHz)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance (except $\overline{BYTE}/V_{PP}$) | $V_{IN}$ = 0V | | 10 | pF |
| | Input Capacitance ($\overline{BYTE}/V_{PP}$) | $V_{IN}$ = 0V | | 120 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | | 12 | pF |

Note: 1. Sampled only, not 100% tested.

**Table 7. Read Mode DC Characteristics** (1)
($T_A$ = 0 to 70 °C or –40 to 85 °C; $V_{CC}$ = 5V ± 5% or 5V ± 10%; $V_{PP}$ = $V_{CC}$)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | 0V ≤ $V_{IN}$ ≤ $V_{CC}$ | | ±1 | µA |
| $I_{LO}$ | Output Leakage Current | 0V ≤ $V_{OUT}$ ≤ $V_{CC}$ | | ±10 | µA |
| $I_{CC}$ | Supply Current | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$, $I_{OUT}$ = 0mA, f = 8MHz | | 70 | mA |
| | | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$, $I_{OUT}$ = 0mA, f = 5MHz | | 50 | mA |
| $I_{CC1}$ | Supply Current (Standby) TTL | $\overline{E}$ = $V_{IH}$ | | 1 | mA |
| $I_{CC2}$ | Supply Current (Standby) CMOS | $\overline{E}$ > $V_{CC}$ – 0.2V | | 50 | µA |
| $I_{PP}$ | Program Current | $V_{PP}$ = $V_{CC}$ | | 10 | µA |
| $V_{IL}$ | Input Low Voltage | | –0.3 | 0.8 | V |
| $V_{IH}$ (2) | Input High Voltage | | 2 | $V_{CC}$ + 1 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | 0.4 | V |
| $V_{OH}$ | Output High Voltage TTL | $I_{OH}$ = –400µA | 2.4 | | V |

Note: 1. $V_{CC}$ must be applied simultaneously with or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. Maximum DC voltage on Output is $V_{CC}$ + 0.5V.

### Standby Mode

The M27C800 has a standby mode which reduces the supply current from 50mA to 100µA. The M27C800 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

**Table 8A. Read Mode AC Characteristics (1)**
($T_A$ = 0 to 70 °C or –40 to 85 °C; $V_{CC}$ = 5V ± 5% or 5V ± 10%; $V_{PP}$ = $V_{CC}$)

| Symbol | Alt | Parameter | Test Condition | M27C800 | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | -50 (3) | | -70 | | -90 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{AVQV}$ | $t_{ACC}$ | Address Valid to Output Valid | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$ | | 50 | | 70 | | 90 | ns |
| $t_{BHQV}$ | $t_{ST}$ | BYTE High to Output Valid | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$ | | 50 | | 70 | | 90 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable Low to Output Valid | $\overline{G}$ = $V_{IL}$ | | 50 | | 70 | | 90 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable Low to Output Valid | $\overline{E}$ = $V_{IL}$ | | 30 | | 35 | | 45 | ns |
| $t_{BLQZ}$ (2) | $t_{STD}$ | BYTE Low to Output Hi-Z | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$ | | 30 | | 30 | | 30 | ns |
| $t_{EHQZ}$ (2) | $t_{DF}$ | Chip Enable High to Output Hi-Z | $\overline{G}$ = $V_{IL}$ | 0 | 30 | 0 | 30 | 0 | 30 | ns |
| $t_{GHQZ}$ (2) | $t_{DF}$ | Output Enable High to Output Hi-Z | $\overline{E}$ = $V_{IL}$ | 0 | 30 | 0 | 30 | 0 | 30 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Address Transition to Output Transition | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$ | 5 | | 5 | | 5 | | ns |
| $t_{BLQX}$ | $t_{OH}$ | BYTE Low to Output Transition | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$ | 5 | | 5 | | 5 | | ns |

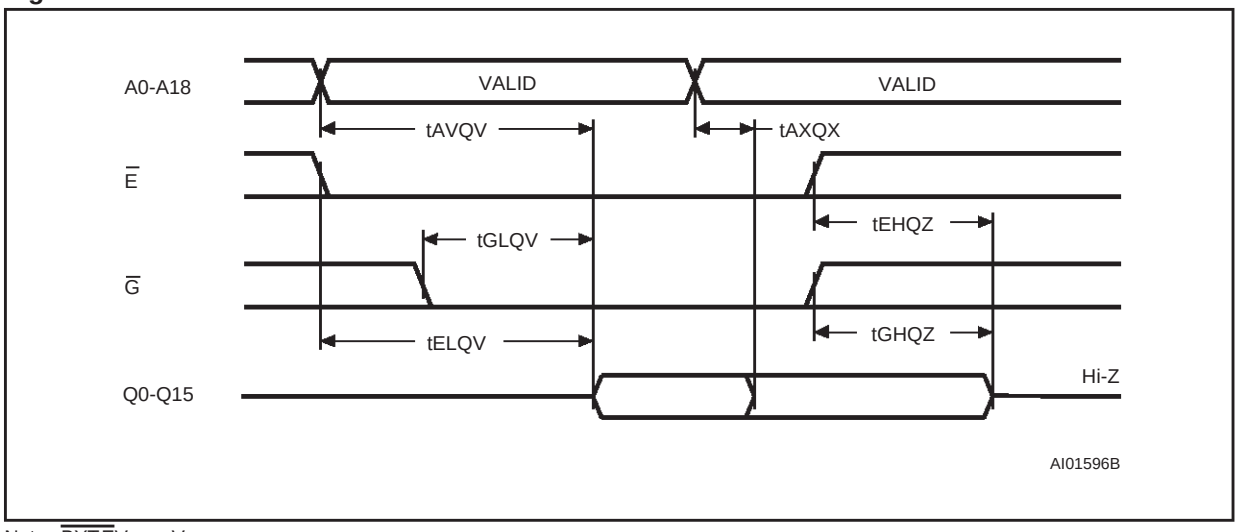
Note: 1. $V_{CC}$ must be applied simultaneously with or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. Sampled only, not 100% tested.
3. Speed obtained with High Speed AC measurement conditions.

**Table 8B. Read Mode AC Characteristics (1)**
($T_A$ = 0 to 70 °C or –40 to 85 °C; $V_{CC}$ = 5V ± 5% or 5V ± 10%; $V_{PP}$ = $V_{CC}$)

| Symbol | Alt | Parameter | Test Condition | M27C800 | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | -100 | | -120/150 | | |
| | | | | Min | Max | Min | Max | |
| $t_{AVQV}$ | $t_{ACC}$ | Address Valid to Output Valid | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$ | | 100 | | 120 | ns |
| $t_{BHQV}$ | $t_{ST}$ | BYTE High to Output Valid | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$ | | 100 | | 120 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable Low to Output Valid | $\overline{G}$ = $V_{IL}$ | | 100 | | 120 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable Low to Output Valid | $\overline{E}$ = $V_{IL}$ | | 50 | | 60 | ns |
| $t_{BLQZ}$ (2) | $t_{STD}$ | BYTE Low to Output Hi-Z | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$ | | 40 | | 50 | ns |
| $t_{EHQZ}$ (2) | $t_{DF}$ | Chip Enable High to Output Hi-Z | $\overline{G}$ = $V_{IL}$ | 0 | 40 | 0 | 50 | ns |
| $t_{GHQZ}$ (2) | $t_{DF}$ | Output Enable High to Output Hi-Z | $\overline{E}$ = $V_{IL}$ | 0 | 40 | 0 | 50 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Address Transition to Output Transition | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$ | 5 | | 5 | | ns |
| $t_{BLQX}$ | $t_{OH}$ | BYTE Low to Output Transition | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$ | 5 | | 5 | | ns |

Note: 1. $V_{CC}$ must be applied simultaneously with or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. Sampled only, not 100% tested.

**Figure 5. Word-Wide Read Mode AC Waveforms**




Note: $\overline{BYTE}V_{PP} = V_{IH}$.

### Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2-line control function which accommodates the use of multiple memory connection. The two-line control function allows:

a. the lowest possible memory power dissipation

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

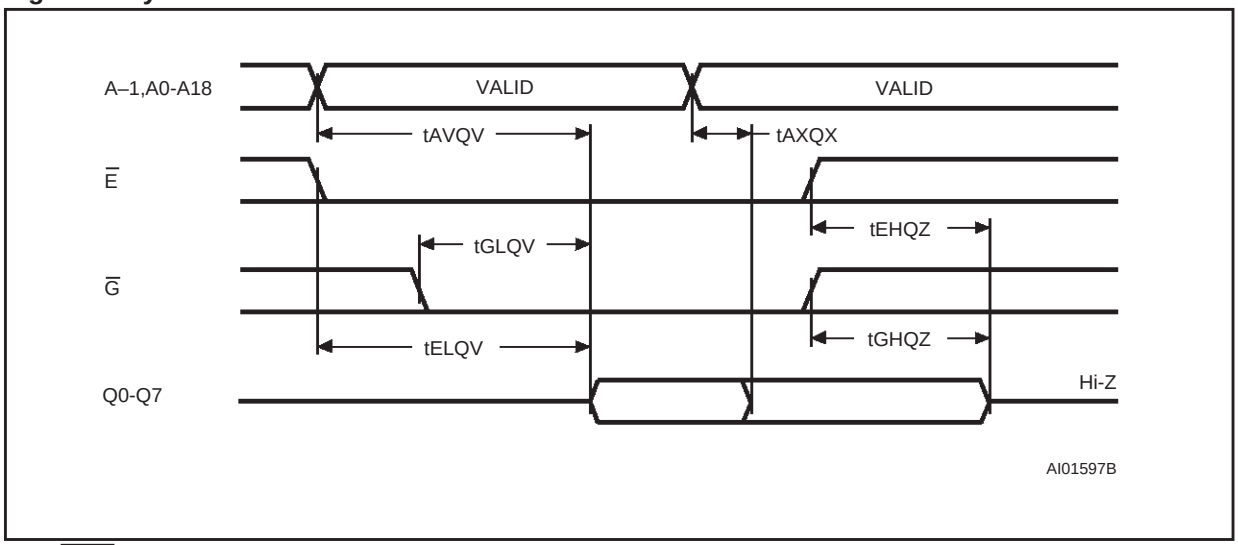
### System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the supplies to the devices. The supply current $I_{CC}$ has three segments of importance to the system designer: the standby current, the active current and the transient peaks that are produced by the falling and rising edges of $\overline{E}$.

The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device outputs. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor is used on every device between $V_{CC}$ and $V_{SS}$.

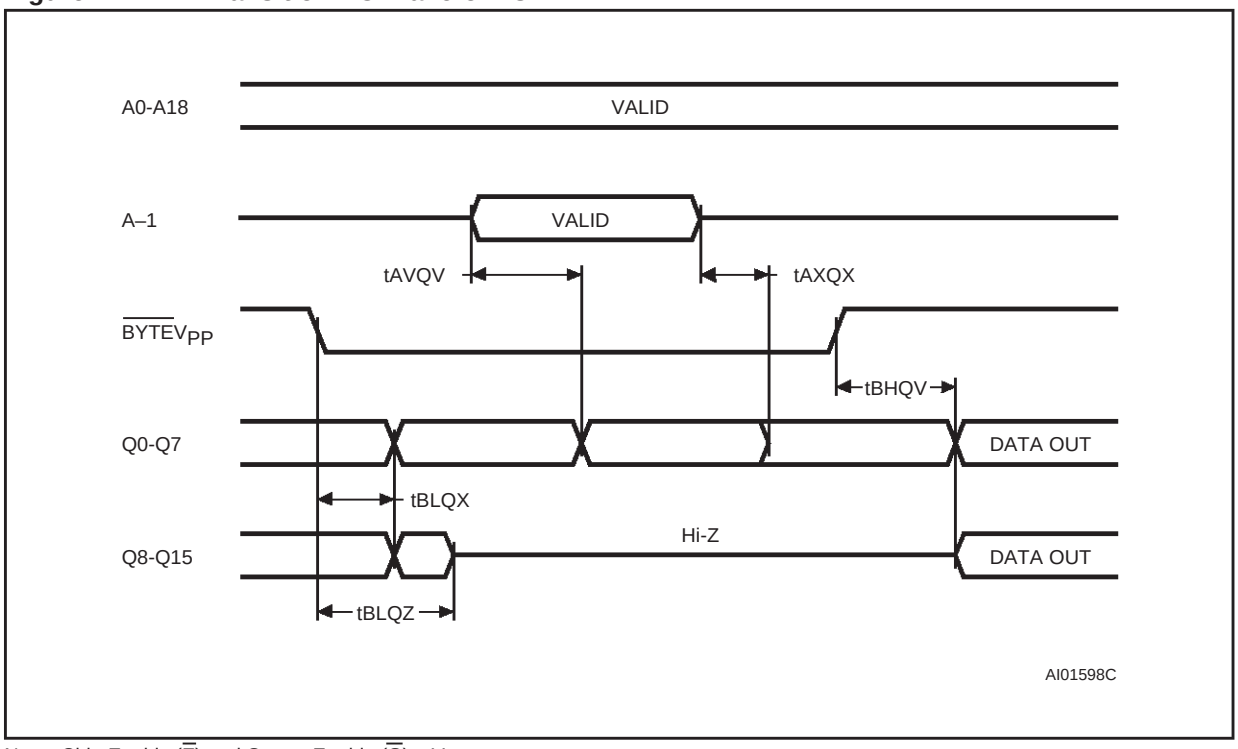
This should be a high frequency type of low inherent inductance and should be placed as close as possible to the device. In addition, a 4.7µF electrolytic capacitor should be used between $V_{CC}$ and $V_{SS}$ for every eight devices. This capacitor should be mounted near the power supply connection point. The purpose of this capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

**Figure 6. Byte-Wide Read Mode AC Waveforms**




Note: $\overline{BYTE}V_{PP} = V_{IL}$.

**Figure 7. $\overline{BYTE}$ Transition AC Waveforms**




Note: Chip Enable ($\overline{E}$) and Output Enable ($\overline{G}$) = $V_{IL}$.

**Table 9. Programming Mode DC Characteristics (1)**
($T_A$ = 25 °C; $V_{CC}$ = 6.25V ± 0.25V; $V_{PP}$ = 12.5V ± 0.25V)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $0 \le V_{IN} \le V_{CC}$ | | ±1 | µA |
| $I_{CC}$ | Supply Current | | | 50 | mA |
| $I_{PP}$ | Program Current | $\overline{E} = V_{IL}$ | | 50 | mA |
| $V_{IL}$ | Input Low Voltage | | –0.3 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.4 | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | 0.4 | V |
| $V_{OH}$ | Output High Voltage TTL | $I_{OH}$ = –2.5mA | 3.5 | | V |
| $V_{ID}$ | A9 Voltage | | 11.5 | 12.5 | V |

Note: 1. $V_{CC}$ must be applied simultaneously with or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.

**Table 10. Programming Mode AC Characteristics (1)**
($T_A$ = 25 °C; $V_{CC}$ = 6.25V ± 0.25V; $V_{PP}$ = 12.5V ± 0.25V)

| Symbol | Alt | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{AVEL}$ | $t_{AS}$ | Address Valid to Chip Enable Low | | 2 | | µs |
| $t_{QVEL}$ | $t_{DS}$ | Input Valid to Chip Enable Low | | 2 | | µs |
| $t_{VPHAV}$ | $t_{VPS}$ | $V_{PP}$ High to Address Valid | | 2 | | µs |
| $t_{VCHAV}$ | $t_{VCS}$ | $V_{CC}$ High to Address Valid | | 2 | | µs |
| $t_{ELEH}$ | $t_{PW}$ | Chip Enable Program Pulse Width | | 45 | 55 | µs |
| $t_{EHQX}$ | $t_{DH}$ | Chip Enable High to Input Transition | | 2 | | µs |
| $t_{QXGL}$ | $t_{OES}$ | Input Transition to Output Enable Low | | 2 | | µs |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable Low to Output Valid | | | 120 | ns |
| $t_{GHQZ}$ (2) | $t_{DFP}$ | Output Enable High to Output Hi-Z | | 0 | 130 | ns |
| $t_{GHAX}$ | $t_{AH}$ | Output Enable High to Address Transition | | 0 | | ns |

Note: 1. $V_{CC}$ must be applied simultaneously with or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. Sampled only, not 100% tested.

## Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C800 are in the '1' state. Data is introduced by selectively programming '0's into the desired bit locations. Although only '0's will be programmed, both '1's and '0's can be present in the data word. The only way to change a '0' to a '1' is by die exposition to ultraviolet light (UVEPROM). The M27C800 is in the programming mode when $V_{PP}$ input is at 12.5V, $\overline{G}$ is at $V_{IH}$ and $\overline{E}$ is pulsed to $V_{IL}$. The data to be programmed is applied to 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. $V_{CC}$ is specified to be 6.25V ± 0.25V.

**Figure 8. Programming and Verify Modes AC Waveforms**

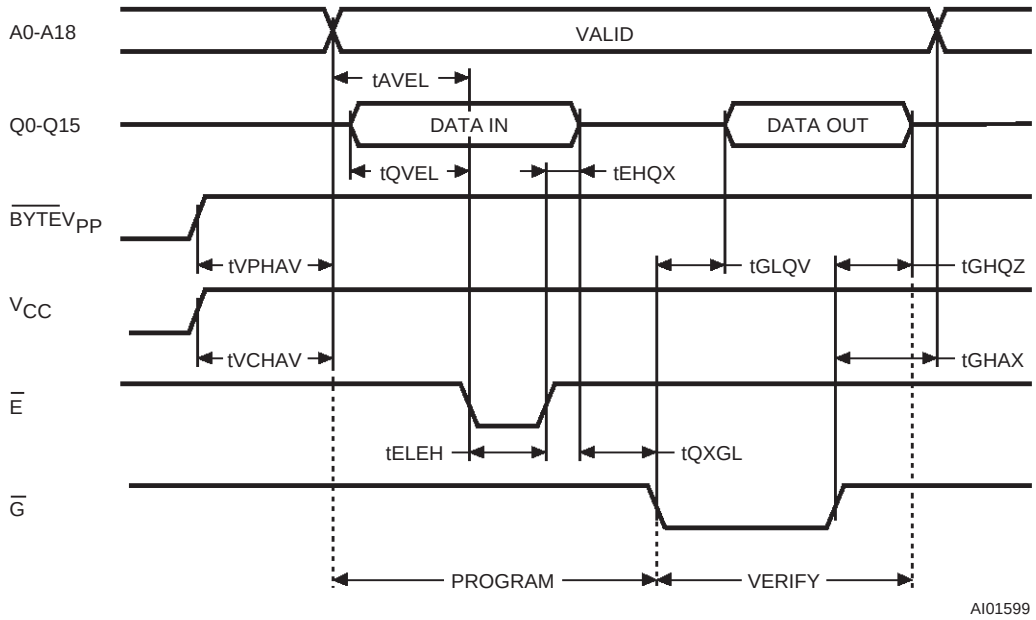
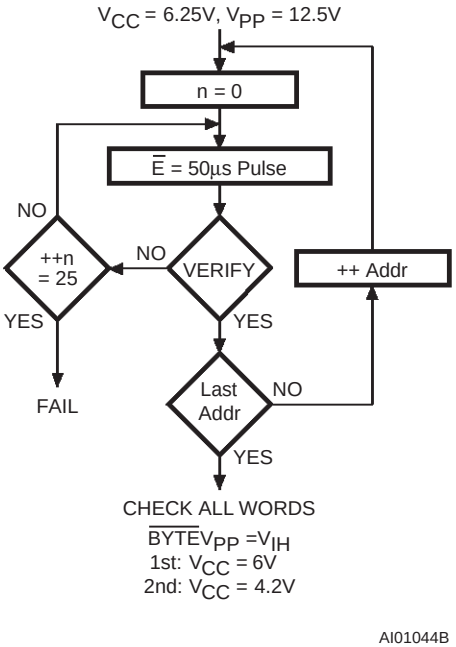



**Figure 9. Programming Flowchart**




### PRESTO III Programming Algorithm

The PRESTO III Programming Algorithm allows the whole array to be programed with a guaranteed margin in a typical time of 26 seconds. Programming with PRESTO III consists of applying a sequence of 50µs program pulses to each word until a correct verify occurs (see Figure 9). During programing and verify operation a MARGIN MODE circuit is automatically activated to guarantee that each cell is programed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

### Program Inhibit

Programming of multiple M27C800s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C800 may be common. A TTL low level pulse applied to a M27C800's $\overline{E}$ input and $V_{PP}$ at 12.5V, will program that M27C800. A high level $\overline{E}$ input inhibits the other M27C800s from being programmed.

### Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ at $V_{IH}$ and $\overline{G}$ at $V_{IL}$, $V_{PP}$ at 12.5V and $V_{CC}$ at 6.25V.

### Electronic Signature

The Electronic Signature (ES) mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C800. To activate the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C800, with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from $V_{IL}$ to $V_{IH}$. All other address lines must be held at $V_{IL}$ during Electronic Signature mode.

Byte 0 (A0 = $V_{IL}$) represents the manufacturer code and byte 1 (A0 = $V_{IH}$) the device identifier code. For the STMicroelectronics M27C800, these two identifier bytes are given in Table 4 and can be read-out on outputs Q7 to Q0.

### ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C800 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C800 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C800 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C800 window to prevent unintentional erasure. The recommended erasure procedure for M27C800 is exposure to short wave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 30 W-sec/cm$^2$. The erasure time with this dosage is approximately 30 to 40 minutes using an ultraviolet lamp with 12000 µW/cm$^2$ power rating. The M27C800 should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

**Table 11. Ordering Information Scheme**

Example: M27C800 -50 X M 1 TR

**Device Type**
M27

**Supply Voltage**
C = 5V

**Device Function**
800 = 8 Mbit (1Mb x8 or 512Kb x16)

**Speed**
-50 (1) = 50 ns
-70 = 70 ns
-90 = 90 ns
-100 = 100 ns
-120 = 120 ns
-150 = 150 ns

**$V_{CC}$ Tolerance**
blank = ± 10%
X = ± 5%

**Package**
F = FDIP42W
B = PDIP42
K = PLCC44
M = SO44

**Temperature Range**
1 = 0 to 70 °C
6 = –40 to 85 °C

**Options**
TR = Tape & Reel Packing

Note: 1. High Speed, see AC Characteristics section for further information.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

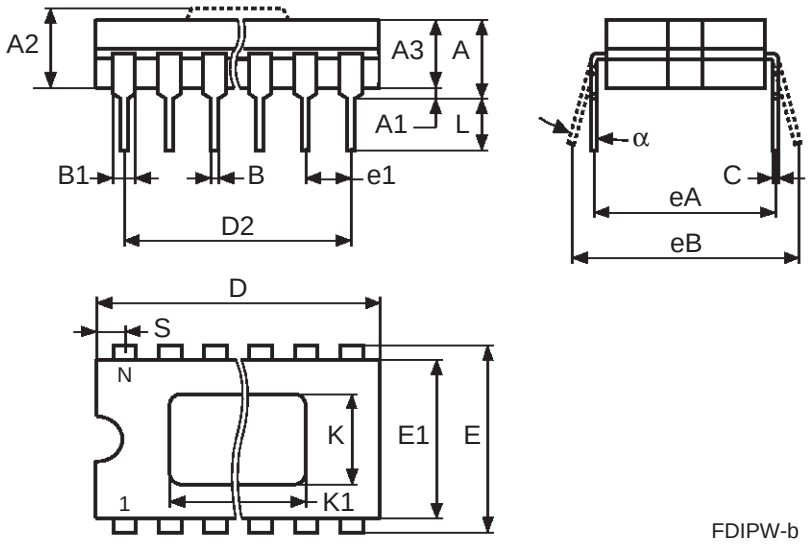
**Table 1. Revision History**

| Date | Revision Details |
|---|---|
| March 1999 | First Issue |
| 25-Jan-2000 | 50ns speed class addes (Tables 8A and 11)<br>Electronic Signature change (Table 4)<br>FDIP42W Package Dimension, L Max added (Table 12) |
| 25-Sep-2000 | AN620 Reference removed |
| 10-Dec-2001 | Ordering Information Scheme (Table 11) clarified |

**Table 12. FDIP42W - 42 pin Ceramic Frit-seal DIP, with window, Package Mechanical Data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 5.72 | | | 0.225 |
| A1 | | 0.51 | 1.40 | | 0.020 | 0.055 |
| A2 | | 3.91 | 4.57 | | 0.154 | 0.180 |
| A3 | | 3.89 | 4.50 | | 0.153 | 0.177 |
| B | | 0.41 | 0.56 | | 0.016 | 0.022 |
| B1 | 1.45 | – | – | 0.057 | – | – |
| C | | 0.23 | 0.30 | | 0.009 | 0.012 |
| D | | 54.41 | 54.86 | | 2.142 | 2.160 |
| D2 | 50.80 | – | – | 2.000 | – | – |
| E | 15.24 | – | – | 0.600 | – | – |
| E1 | | 14.50 | 14.90 | | 0.571 | 0.587 |
| e | 2.54 | – | – | 0.100 | – | – |
| eA | 14.99 | – | – | 0.590 | – | – |
| eB | | 16.18 | 18.03 | | 0.637 | 0.710 |
| L | | 3.18 | 4.10 | | 0.125 | 0.161 |
| S | | 1.52 | 2.49 | | 0.060 | 0.098 |
| K | 9.40 | – | – | 0.370 | – | – |
| K1 | 11.43 | – | – | 0.450 | – | – |
| α | | 4° | 11° | | 4° | 11° |
| N | 42 | | | 42 | | |

**Figure 10. FDIP42W - 42 pin Ceramic Frit-seal DIP, with window, Package Outline**

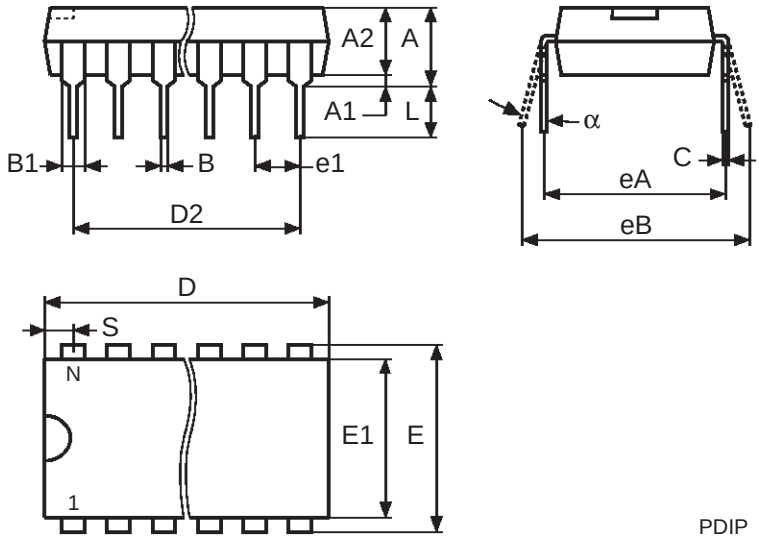



Drawing is not to scale.

**Table 13. PDIP42 - 42 pin Plastic DIP, 600 mils width, Package Mechanical Data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | – | 5.08 | | – | 0.200 |
| A1 | | 0.25 | – | | 0.010 | – |
| A2 | | 3.56 | 4.06 | | 0.140 | 0.160 |
| B | | 0.38 | 0.53 | | 0.015 | 0.021 |
| B1 | | 1.27 | 1.65 | | 0.050 | 0.065 |
| C | | 0.20 | 0.36 | | 0.008 | 0.014 |
| D | | 52.20 | 52.71 | | 2.055 | 2.075 |
| D2 | 50.80 | – | – | 2.000 | – | – |
| E | 15.24 | – | – | 0.600 | – | – |
| E1 | | 13.59 | 13.84 | | 0.535 | 0.545 |
| e1 | 2.54 | – | – | 0.100 | – | – |
| eA | 14.99 | – | – | 0.590 | – | – |
| eB | | 15.24 | 17.78 | | 0.600 | 0.700 |
| L | | 3.18 | 3.43 | | 0.125 | 0.135 |
| S | | 0.86 | 1.37 | | 0.034 | 0.054 |
| α | | 0° | 10° | | 0° | 10° |
| N | 42 | | | 42 | | |

**Figure 11. PDIP42 - 42 pin Plastic DIP, 600 mils width, Package Outline**

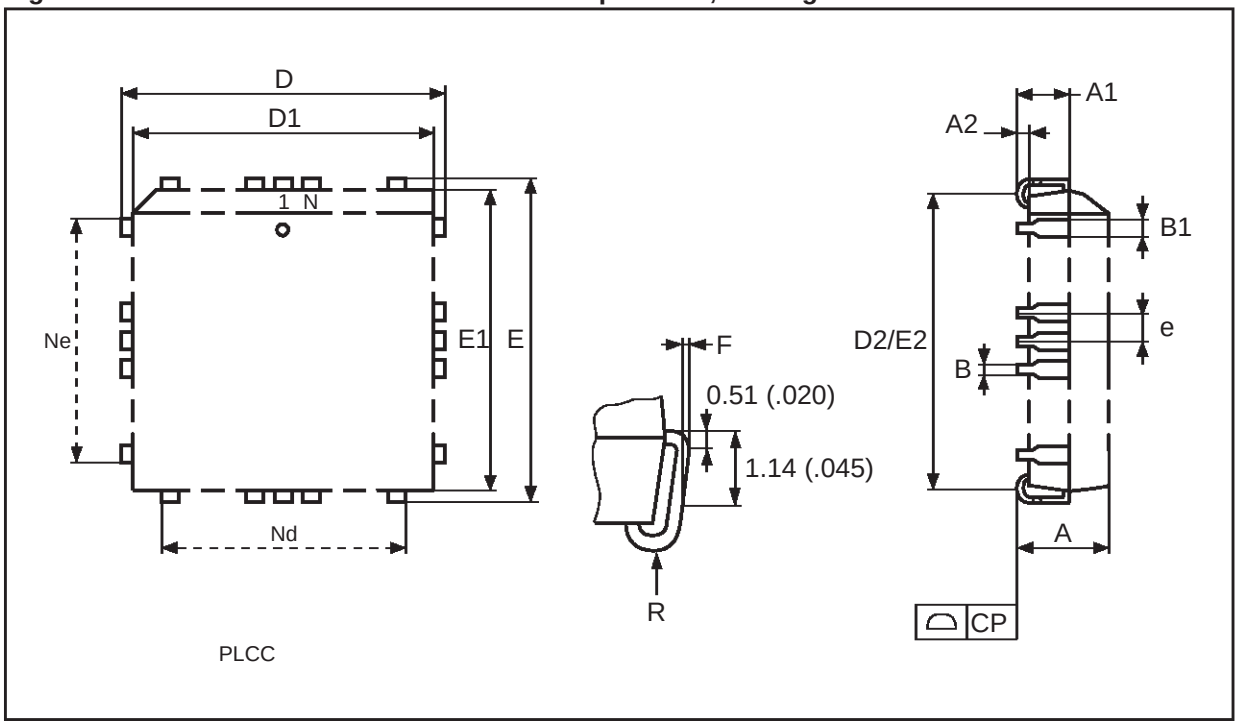



Drawing is not to scale.

**Table 14. PLCC44 - 44 lead Plastic Leaded Chip Carrier, Package Mechanical Data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | 4.20 | 4.70 | | 0.165 | 0.185 |
| A1 | | 2.29 | 3.04 | | 0.090 | 0.120 |
| A2 | | – | 0.51 | | – | 0.020 |
| B | | 0.33 | 0.53 | | 0.013 | 0.021 |
| B1 | | 0.66 | 0.81 | | 0.026 | 0.032 |
| D | | 17.40 | 17.65 | | 0.685 | 0.695 |
| D1 | | 16.51 | 16.66 | | 0.650 | 0.656 |
| D2 | | 14.99 | 16.00 | | 0.590 | 0.630 |
| E | | 17.40 | 17.65 | | 0.685 | 0.695 |
| E1 | | 16.51 | 16.66 | | 0.650 | 0.656 |
| E2 | | 14.99 | 16.00 | | 0.590 | 0.630 |
| e | 1.27 | – | – | 0.050 | – | – |
| F | | 0.00 | 0.25 | | 0.000 | 0.010 |
| R | 0.89 | – | – | 0.035 | – | – |
| N | 44 | | | 44 | | |
| CP | | | 0.10 | | | 0.004 |

**Figure 12. PLCC44 - 44 lead Plastic Leaded Chip Carrier, Package Outline**

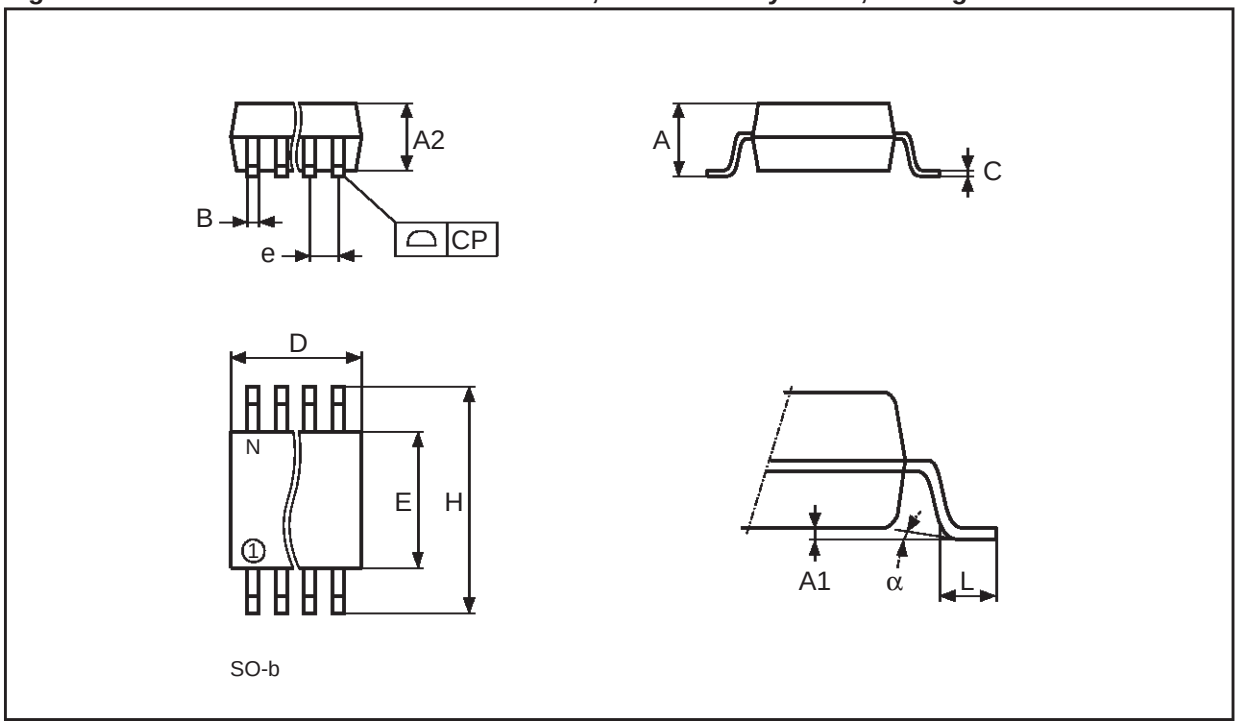



Drawing is not to scale.

**Table 15. SO44 - 44 lead Plastic Small Outline, 525 mils body width, Package Mechanical Data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | 2.42 | 2.62 | | 0.095 | 0.103 |
| A1 | | 0.22 | 0.23 | | 0.009 | 0.010 |
| A2 | | 2.25 | 2.35 | | 0.089 | 0.093 |
| B | | | 0.50 | | | 0.020 |
| C | | 0.10 | 0.25 | | 0.004 | 0.010 |
| D | | 28.10 | 28.30 | | 1.106 | 1.114 |
| E | | 13.20 | 13.40 | | 0.520 | 0.528 |
| e | 1.27 | – | – | 0.050 | – | – |
| H | | 15.90 | 16.10 | | 0.626 | 0.634 |
| L | 0.80 | – | – | 0.031 | – | – |
| α | 3° | – | – | 3° | – | – |
| N | 44 | | | 44 | | |
| CP | | | 0.10 | | | 0.004 |

**Figure 13. SO44 - 44 lead Plastic Small Outline, 525 mils body width, Package Outline**




Drawing is not to scale.