M52334FP

PLL-SPLIT VIF/SIF IC

DESCRIPTION

The M52334FP is IF signal-processing IC for VCRs and TVs. It enable the PLL detection system despite size as small as that of conventional quasi-synchronous VIF/SIF detector, IF/RF AGC, SIF limiter and FM detector.

FEATURES

- Video detection output is $2V_{P-P}$. It has built-in EQ AMP.
- The package is a 20-pin flat package, suitable for space saving.
- The video detector uses PLL for full synchronous detection circuit. It produces excellent characteristics of DG, DP, 920kHz beat, and cross color.
- Dynamic AGC realizes high speed response with only single filter.
- Video IF and sound IF signal processings are separated from each other. VCO output is used to obtain intercarrier.
- As AFT output voltage uses the APC output voltage, VCO coil is not used.
- Audio FM demodulation uses PLL system, so it has wide frequency range with no external parts and no adjustment.
- This IC corresponds to only inter of NTSC system.

APPLICATION

TV sets, VCR tuners

RECOMMENDED OPERATING CONDITION

In case of V_{CC} and Vreg. out short

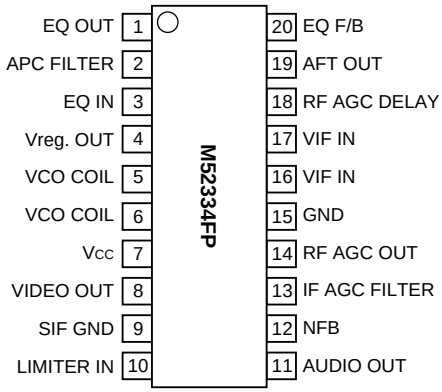
Supply voltage range.....4.75 to 5.25V

Recommended supply voltage.....5.0V

Incase of Vreg. out open

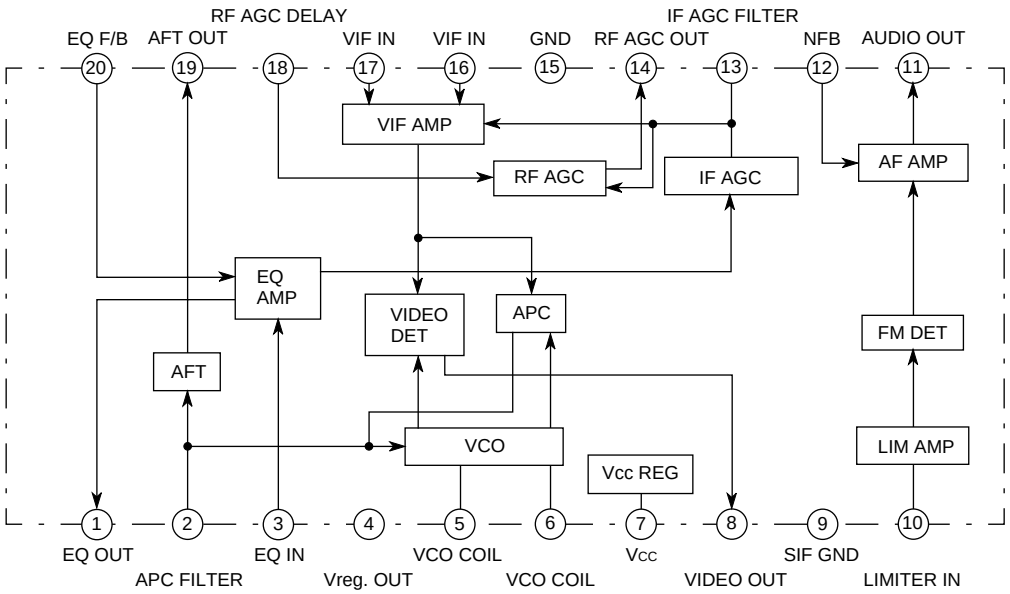
Supply voltage range.....8.5 to 12.5V

PIN CONFIGURATION (TOP VIEW)



Outline 20P2N-A

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage1	V_{CC} and Vreg. out is not connected to each other.	13.2	V
Vreg. OUT	Supply voltage Vreg. OUT	V_{CC} and Vreg. out is not connected to each other.	6.0	V
P_d	Power dissipation		1225	mW
T_{opr}	Operating temperature		-20 to +85	°C
T_{stg}	Storage temperature		-40 to +150	°C
Surge	Surge voltage resistance	Surge protection capacitance 200pF resistance 0Ω	±200	V

ELECTRICAL CHARACTERISTICS (V_{CC}=9V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test circuit	Test point	Input point	Input SG	Measurement condition	Limits			Unit
						switches set to position 1 unless otherwise indicated	Min.	Typ.	Max.	
VIF section										
I_{CC1}	Circuit current1 V_{CC}=5V	1	A	–	–	V_{CC}=5V SW4=2, SW7=2	33	40.5	47	mA
I_{CC2}	Circuit current2 V_{CC}=12V	1	A	–	–	V_{CC}=12V SW7=2	31	40.5	49	mA
V_{CC2}	Vreg voltage2	1	TP4	–	–	V_{CC}=12V	4.7	5.00	5.3	V
V1	Video output DC voltage1	1	TP1A	–	–	SW13=2 V13=0V	3.45	3.9	4.35	V
Vo det8	Video output voltage8	1	TP8	VIF IN	SG1		0.85	1.1	1.35	V_{P-P}
Vo det	Video output voltage1	1	TP1A	VIF IN	SG1		1.85	2.2	2.55	V_{P-P}
Video S/N	Video S/N	1	TP1B	VIF IN	SG2	SW1=2	51	56	–	dB
BW	Video band width	1	TP1A	VIF IN	SG3	SW13=2 V13=variable	5.0	7.0	–	MHz
VIN MIN	Input sensitivity	1	TP1A	VIF IN	SG4		–	48	52	dBμ
VIN MAX	Maximum allowable input	1	TP1A	VIF IN	SG5		101	105	–	dBμ
GR	AGC control range input	–	–	–	–		50	57	–	dB
V13	IF AGC voltage	1	TP13	VIF IN	SG6		2.85	3.15	3.45	V
V13H	Maximum IF AGC voltage	1	TP13	–	–		4.0	4.4	–	V
V13L	Minimum IF AGC voltage	1	TP13	VIF IN	SG7		2.2	2.4	2.6	V
V14H	Maximum RF AGC voltage	1	TP14	VIF IN	SG2	SW13=2 V13=4V	8.0	8.7	–	V
V14L	Minimum RF AGC voltage	1	TP14	VIF IN	SG2	SW13=2 V13=1V	–	0.1	0.5	V
V14	RF AGC operation voltage	1	TP14	VIF IN	SG8		86	89	92	dBμ
CL-U	Capture range U	1	TP1A	VIF IN	SG9		0.8	1.3	–	MHz
CL-L	Capture range L	1	TP1A	VIF IN	SG9		1.4	2.0	–	MHz
CL-T	Capture range T	1	–	–	–		2.5	3.3	–	MHz
μ	AFT sensitivity	1	TP19	VIF IN	SG10		20	30	70	mV/kHz
V19H	AFT maximum voltage	1	TP19	VIF IN	SG10		7.7	8.2	–	V
V19L	AFT minimum voltage	1	TP19	VIF IN	SG10		–	0.7	1.2	V
AFT def1	AFT defeat 1	1	TP19	VIF IN	–		4.2	4.5	4.8	V
IM	Inter modulation	1	TP3A	VIF IN	SG11	SW13=2 V13=variable	35	42	–	dB
DG	Differential gain	1	TP3A	VIF IN	SG12		–	2	5	%
DP	Differential phase	1	TP3A	VIF IN	SG12		–	2	5	deg
V3 SYNC	Sync. tip level	1	TP3A	VIF IN	SG2		1.0	1.4	1.8	V
RINV	VIF input resister	2	TP17				–	1.2	–	kΩ
CINV	VIF input capacitance	2	TP17				–	5	–	pF

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test circuit	Test point	Input point	Input SG	Measurement condition switches set to position 1 unless otherwise indicated	Limits Min.	Limits Typ.	Limits Max.	Unit
SIF section										
V1	AF output DC voltage	1	TP11	–	–		3.5	4.4	5.3	V
VoAF	AF output	1	TP11	SIF IN	SG16		565	790	1125	mVrms
THD AF	AF output distortion	1	TP11	SIF IN	SG16		–	0.4	0.9	%
LIM	Limiting sensitivity	1	TP11	SIF IN	SG17		–	42	55	dBμ
AMR	AM rejection	1	TP11	SIF IN	SG18		55	65	–	dB
AF S/N	AF S/N	1	TP11	SIF IN	SG19		55	65	–	dB

ELECTRICAL CHARACTERISTICS TEST METHOD

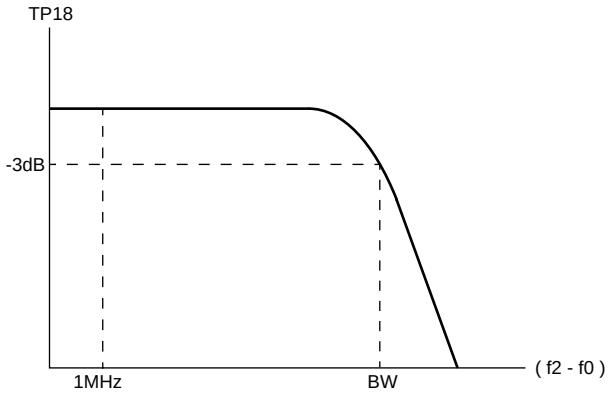
Video S/N

Input SG2 into VIF IN and measure the video out (Pin 3) noise in r.m.s at TP3-B through a 5MHz (-3dB) L.P.F.

$$S/N=20\log\left(\frac{0.7\times Vo\ det}{NOISE}\right)(dB)$$

BW Video band width

1. Measure the 1MHz component level of EQ output TP3A with a spectrum analyzer when SG3 (f2=44.75MHz) is input into VIF IN. At that time, measure the voltage at TP13 with SW13, set to position 2, and then fix V13 at that voltage.
2. Reduce f2 and measure the value of (f2-f0) when the (f2-f0) component level reaches -3dB from the 1MHz component level as shown below.



VIN MIN Input sensitivity

Input SG4 (Vi=90dBμ) into VIF IN, and then gradually reduce Vi and measure the input level when the 20kHz component of EQ output TP3A reaches -3dB from Vo det level.

VIN MAX Maximum allowable input

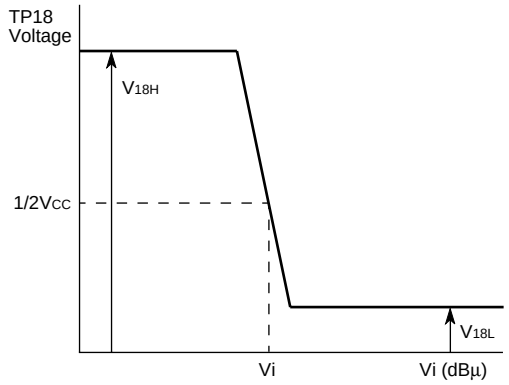
1. Input SG5 (Vi=90dBμ) into VIF IN, and measure the level of the 20kHz component of EQ output.
2. Gradually increase the Vi of SG and measure the input level when the output reaches -3dB.

GR AGC control range

GR=VIN MAX-VIN MIN (dB)

V18 RF AGC operating voltage

Input SG8 into VIF IN, and gradually reduce Vi and then measure the input level when RF AGC output TP14 reaches 1/2 V_{CC}, as shown below.



CL-U Capture range

1. Increase the frequency of SG9 until the VCO is out of locked-oscillation.
2. Decrease the frequency of SG9 and measure the frequency fU when the VCO locks.

CL-U=fU-45.75 (MHz)

CL-L Capture range

1. Decrease the frequency of SG9 until the VCO is out of locked-oscillation.
2. Increase the frequency of SG9 and measure the frequency fL when the VCO locks.

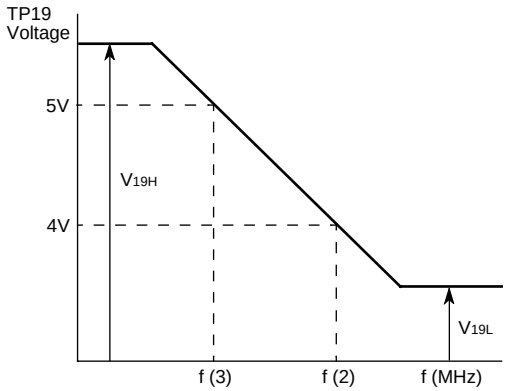
CL-L=45.75-fL (MHz)

CL-T Capture range

CL-T=CL-U+CL-L (MHz)

μ AFT sensitivity, V_{19H} AFT maximum voltage, V_{19L} AFT minimum voltage

1. Input SG10 into VIF IN, and set the frequency of SG10 so that the voltage of AFT output TP19 is 5V. This frequency is named f(3).
2. Set the frequency of SG10 so that the AFT output voltage is 4V. This frequency is named f (2)
3. IN the graph, maximum and minimum DC voltage are V_{19H} and V_{19L}, respectively.



$$\mu = \frac{1000\ (mV)}{f\ (2) - f\ (3)\ (kHz)}\ (mV/kHz)$$

IM Intermodulation

1. Input SG11 into VIF IN, and measure EQ output TP3A with an oscilloscope.
2. Adjust AGC filter voltage V13 so that the minimum DC level of the output waveform is 1.0V.
3. At this time, measure, TP3A with a spectrum analyzer. The intermodulation is defined as a difference between 0.92MHz and 3.58MHz frequency components.

LIM Limiting sensitivity

1. Input SG17 (Vi=90dBμ) into SIF input, and measure the 400Hz component level of AF output TP11.
2. Lower the input level of SG17, and measure the level of SG17 when the VoAF level reaches -3dB.

AMR AM Rejection

1. Input SG18 into SIF input, and measure the output level of AF output TP11. This level is named VAM.
2. AMR is;

$$AMR=20\log\left(\frac{VoAF\ (mVr.m.s)}{VAM\ (mVr.m.s)}\right)(dB)$$

AF S/N

1. Input SG19 into SIF input, and measure the output noise level of AF output TP11. This level is named VN.
2. S/N is;

$$S/N=20\log\left(\frac{VoAF\ (mVr.m.s)}{VN\ (mVr.m.s)}\right)(dB)$$

THE NOTE IN THE SYSTEM SETUP

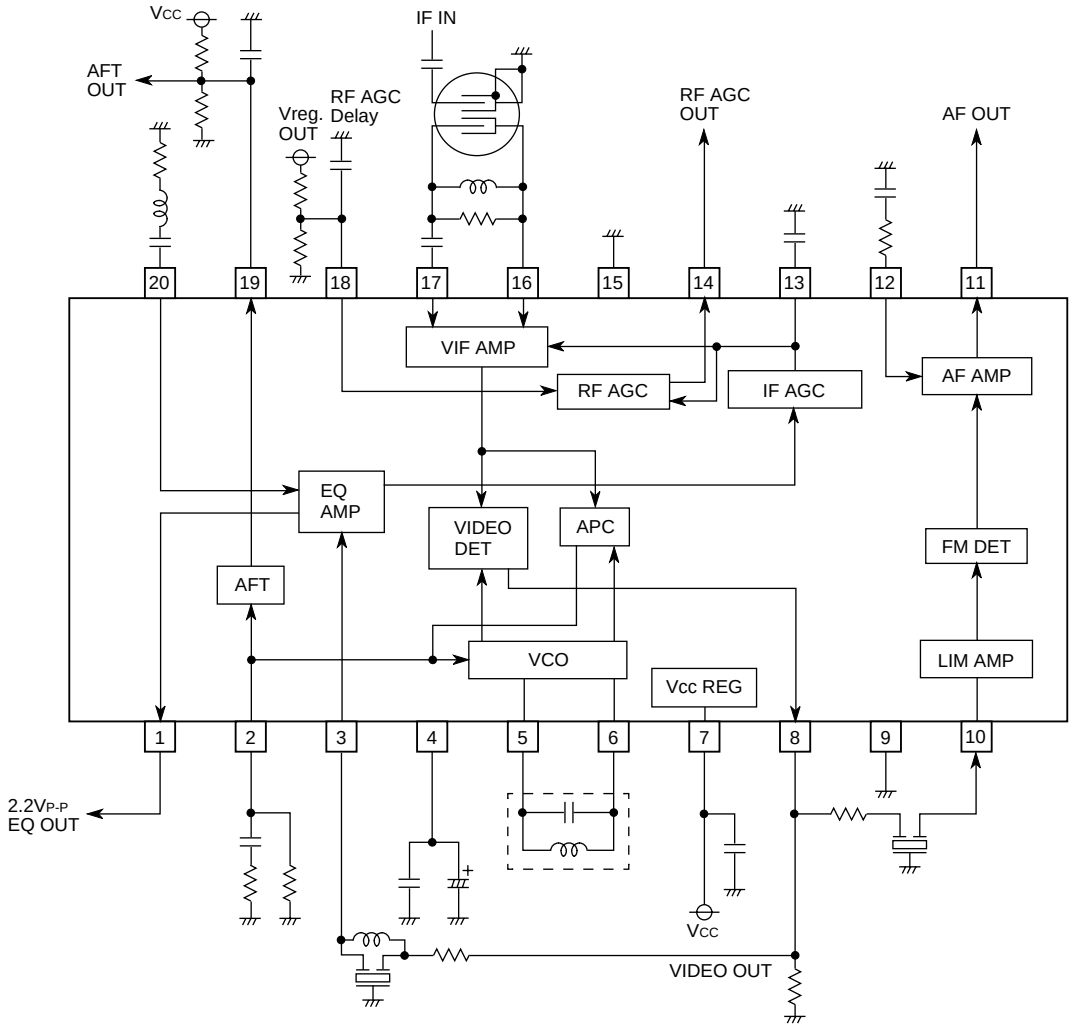
M52334FP has 2 power supply pins of Vcc (pin 7) and Vreg. OUT (pin 4). Pin 7 is for AFT output, RF AGC output circuits and 5V regulated power supply circuit and Pin 4 is for the other circuit blocks. In case M52334FP is used together with other ICs like VIF operating at more than 5V, the same supply voltage as that of connected ICs is applied to Vcc and Vreg. Out is opened. The other circuit blocks, connected to Vreg. OUT are powered by internal 5V regulated power supply.

In case the connecting ICs are operated at 5V, 5V is supplied to both Vcc and Vreg.OUT.

INPUT SIGNAL

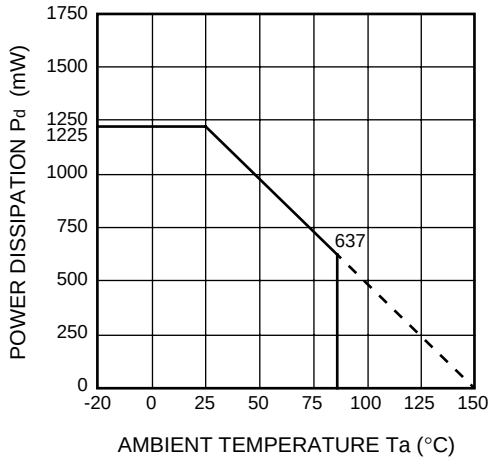
SG No.	Signals (50Ω termination)
1	f_0=45.75MHz AM20kHz 77.8% 90dBμ
2	f_0=45.75MHz 90dBμ CW
3	f_1=45.75MHz 90dBμ CW (Mixed signal) f_2=Frequency variable 70dBμ CW (Mixed signal)
4	f_0=45.75MHz AM20kHz 77.8% level variable
5	f_0=45.75MHz AM20kHz 14.0% level variable
6	f_0=45.75MHz 80dBμ CW
7	f_0=45.75MHz 110dBμ CW
8	f_0=45.75MHz CW level variable
9	f_0=Variable AM20kHz 77.8% 90dBμ
10	f_0=Variable 90dBμ CW
11	f_1=45.75MHz 90dBμ CW (Mixed signal) f_2=42.17MHz 80dBμ CW (Mixed signal) f_3=41.25MHz 80dBμ CW (Mixed signal)
12	f_0=45.75MHz 87.5% TV modulation ten-step waveform Sync tip level 90dBμ
13	f_1=41.25MHz 103dBμ CW
14	f_1=41.25MHz 70dBμ CW
15	f_1=45.75MHz 90dBμ CW (Mixed signal) f_2=41.25MHz 70dBμ CW (Mixed signal)
16	f_0=4.5MHz 90dBμ FM400Hz±25kHz dev
17	f_0=4.5MHz FM400Hz±25kHz dev level variable
18	f_0=4.5MHz 90dBμ AM400Hz 30%
19	f_0=4.5MHz 90dBμ CW

TEST CIRCUIT

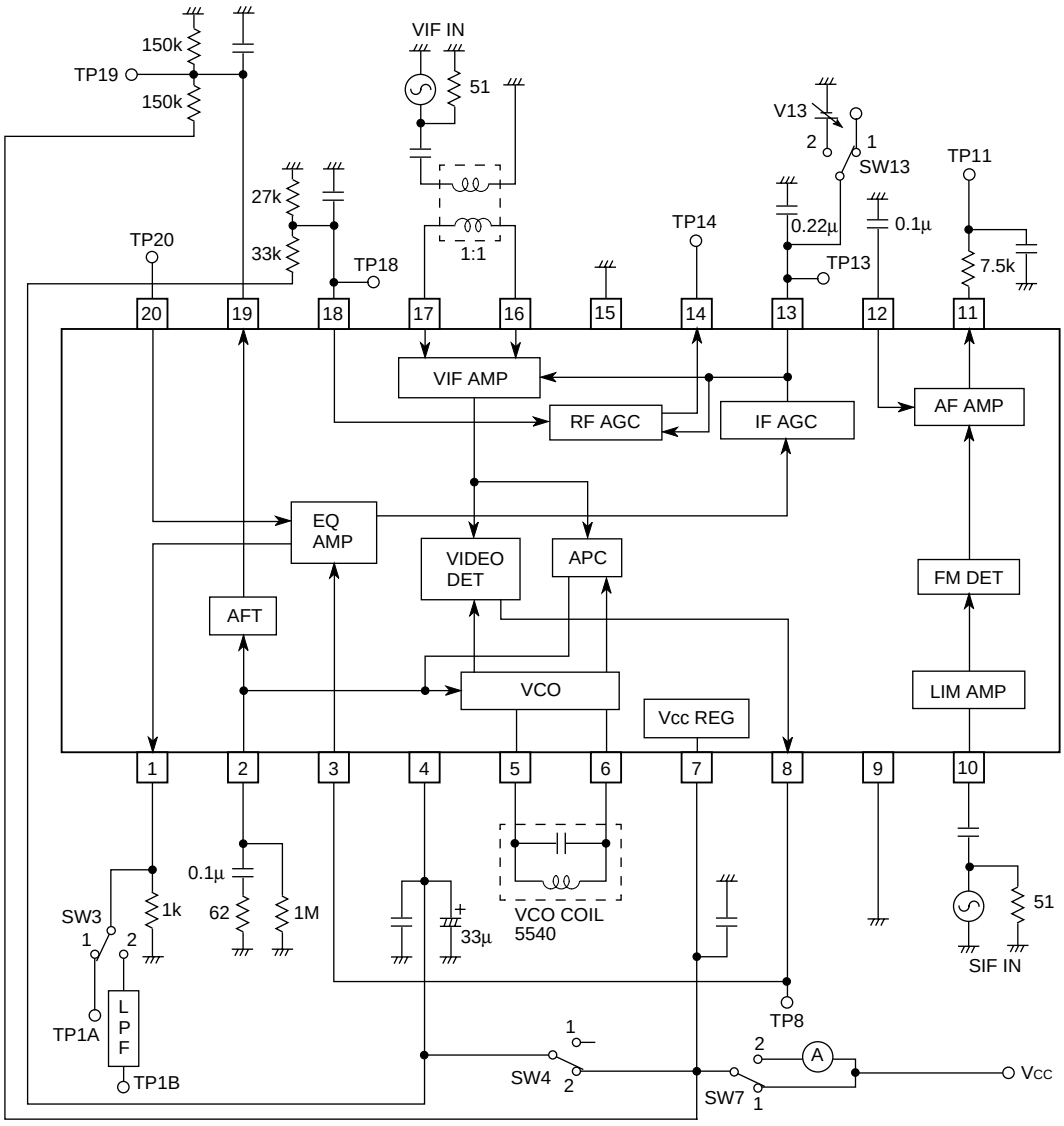


TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)



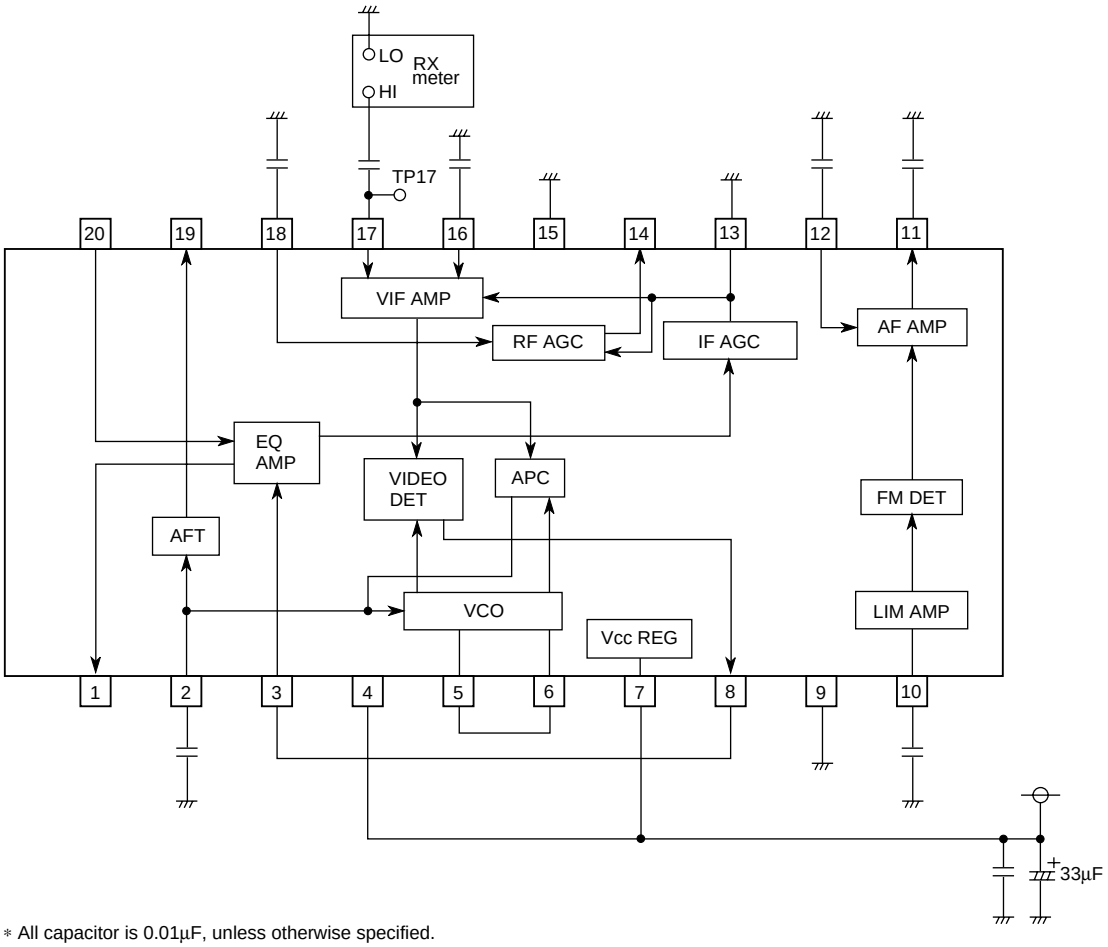
APPLICATION EXAMPLE 1



∗ All capacitor is 0.01µF, unless otherwise specified.
∗ The Measuring Circuit 1 is Mitsubishi standard evaluation fixture.

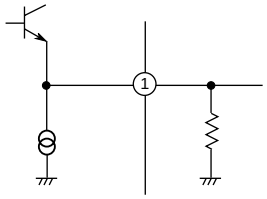
Units Resistance : Ω
Capacitance : F

APPLICATION EXAMPLE 2



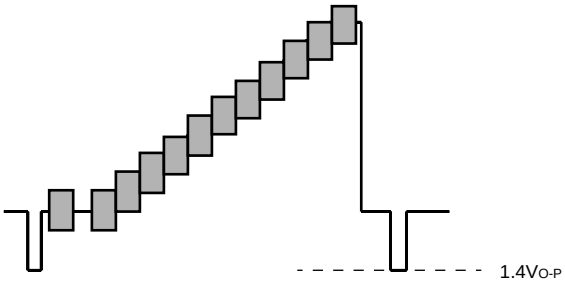
∗ All capacitor is 0.01µF, unless otherwise specified.

Pin 1 (RF AGC DELAY)

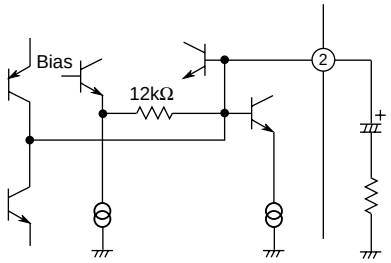


internal
driving current : 3mA

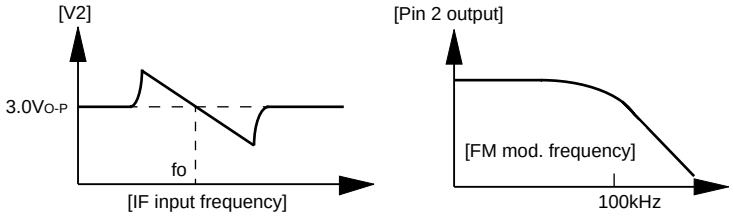
An output amplitude is positive 2.2V_{P-P} in the case of 87.5% video modulation.



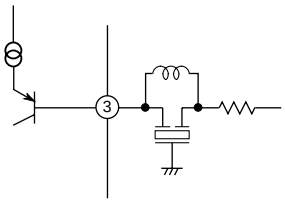
Pin 2 (APC FILTER)



In the locked state, the cut-off frequency of the filter is adjusted effectively by an external resistor so that it will be in the range of around 30 to 200kHz.
In case the cut-off frequency is lower, the pull-in speed becomes slow. On the other hand, a higher cut-off frequency widen the pull-in range and band width, which results in a degradation in the S/N ratio. So, in the actual TV system design, the appropriate constant should be chosen for getting desirable performance considering above conditions.

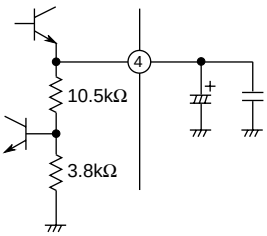


Pin 3 (EQ INPUT)



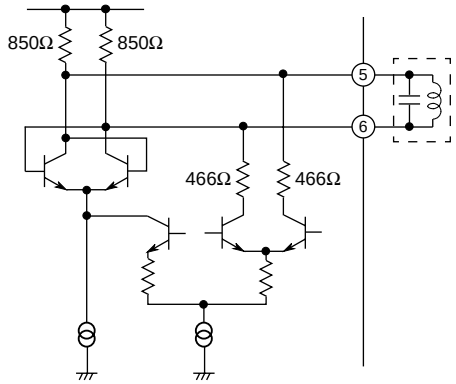
It is an open-base input.
The IF AGC does not work correctly, unless a DC element of pin 8 output is applied to it.

Pin 4 (REG. OUTPUT)



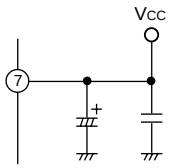
It is a regulated 5V output which has current drive capability of approximately 10mA.

Pin 5, Pin 6 (VCO COIL)



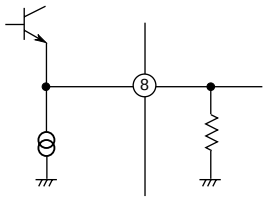
Connecting a tuning coil and capacitor to these pins enables an oscillation.
The tuning capacitor of about 30pF is recommended.
The oscillation frequency is tuned in f0.
In the actual adjustment, the coil is tuned so that the AFT voltage is reached to Vcc/2 with f0 as an input.
The printed pattern around these pins should be designed carefully to prevent an pull-in error of VCO, caused by the leakage interference from the large signal level oscillator to adjacent pins.
The interconnection should be designed as short as possible.
In case the printed pattern has the interference problem, a capacitor of about 1pF is connected between pin 5 or 6 and GND so as to cancel the interference and keep enough pull-in range even in a weak electric field.

Pin 7 (Vcc)



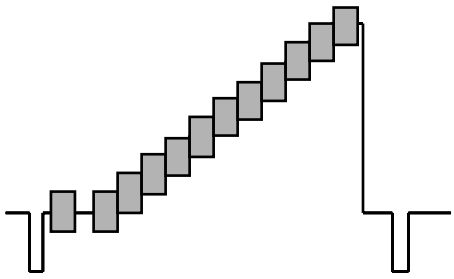
The recommended supply voltage is 5V or 9 to 12V.
In the case of 5V supply, it should be tied to pin 17.
In the case of 9 to 12V supply, a regulated output of 5V are available in pin 17.

Pin 8 (VIDEO OUTPUT)

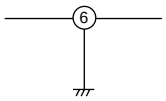


internal
driving current : 2mA

An output amplitude is positive $2V_{P-P}$ in the case of 87.5% video modulation.



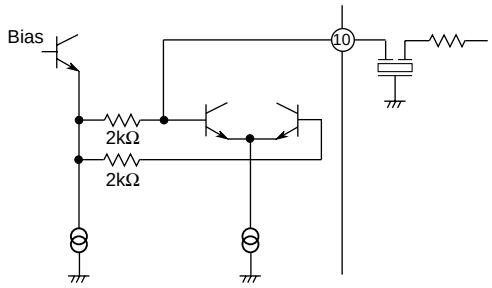
Pin 9 (GND)



It is ground (GND) for the SIF.

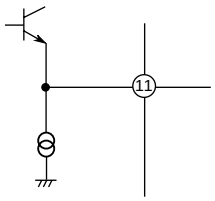
Pin 10 (LIMITER INPUT)

Terminal voltage : 2.2V



The input impedance is 2kΩ.

Pin 11 (AF OUTPUT)

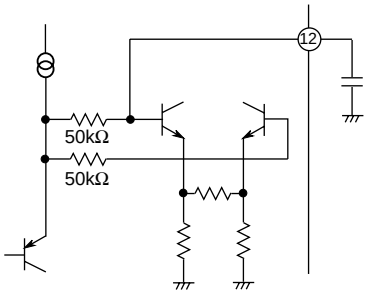


internal
driving current : 1mA

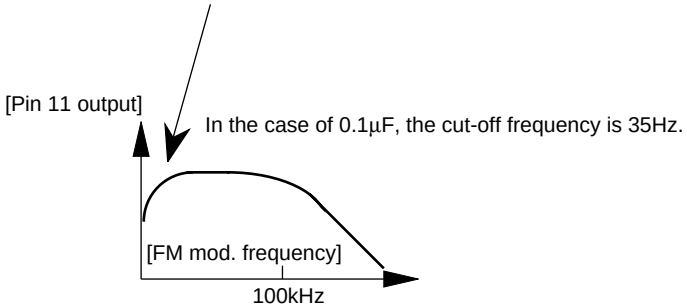
The FM detector can respond to the 4.5MHz intercarrier signal without an adjustment and external components by adopting the PLL technique.
The output DC voltages of $4.4V_{0\text{-}P}$ and $2.4V_{0\text{-}P}$ are in the Vcc of 9V and 5V, respectively.
Since its output frequency is more than 100kHz in no loading condition, it can also respond to the multi audio broadcasting.

Pin 12 (AUDIO F/B)

Terminal voltage : 3.0V

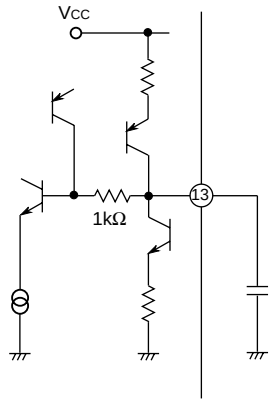


The frequency response of the audio output is set by the external capacitor of pin 12.

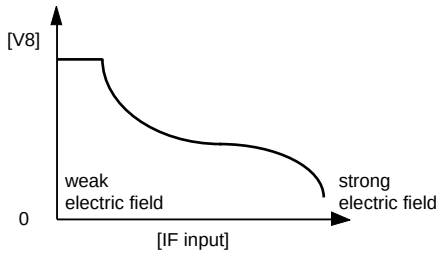


Connecting series resistor to the capacitor above, can reduce an audio output amplitude.

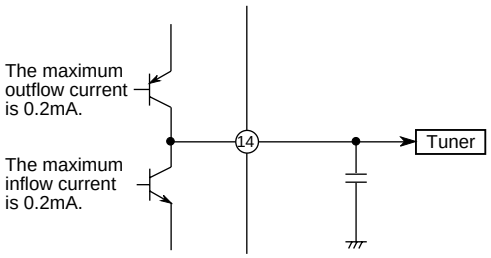
Pin 13 (IF AGC FILTER)



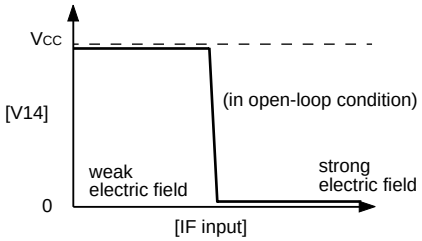
In spite of the 1-pin filter configuration, 2-pin filter characteristics are available by utilizing the dynamic AGC circuit.



Pin 14 (RF AGC OUTPUT)

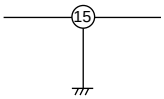


A current mode output is available in the reverse AGC operation.



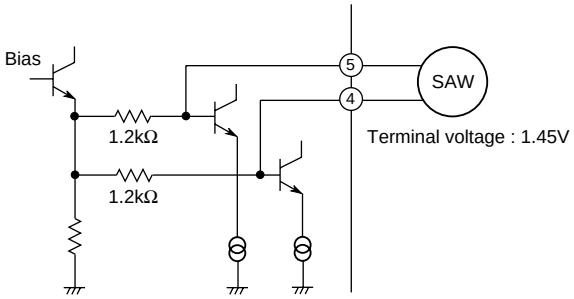
Note: Connecting a nonpolarity capacitor of 1μF between pin14 and pin 18 improves AGC operating speed.
In that case, the capacitors between pin14/pin18 and ground should be removed.

Pin 15 (GND)



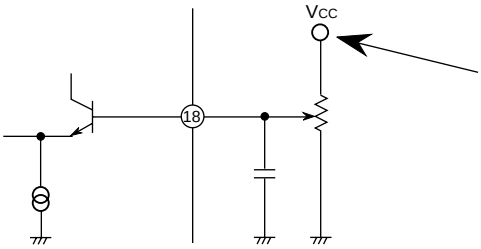
It is GND pin except for SIF.

Pin 16, Pin 17 (VIF INPUT)



It should be designed considering careful impedance matching with the SAW filter.

Pin 18 (RF AGC DELAY)

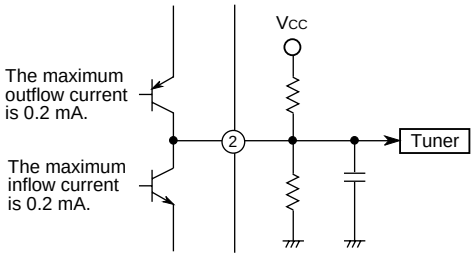


An applied voltage to the pin1 is for changing a RF AGC delay point.

In the 3-in-1 type∗ application, the regulated output from the regulator is suitable for a power supply (Vcc) to it, because there may be difference between the tuner and main board supply.

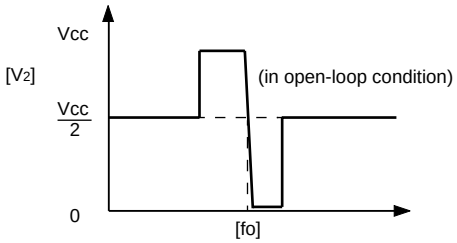
∗ TV tuner, VIF demodulator and RF modulator are togetherin one package.

Pin 19 (AFT OUTPUT)



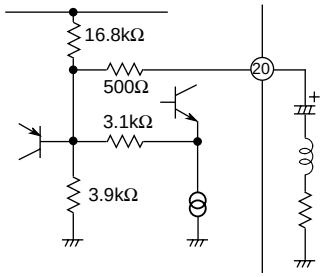
Since an AFT output is provided by a high impedance source, the detection sensitivity can be set by an external resistor.
The muting operation will be on in following two cases;

1) the APC is out of locking,
2) the video output becomes small enough in a weak electric field.



In the case of 5V supply, it should be considered that the maximum AFT and RF AGC output are less than 4.2V and 4.7V, respectively.

Pin 20 (EQ F/B)



Both the external coil and capacitor determine the frequency response of EQ output.
The series connected resistor is for damping.